

# Clocks Trust: An investigation of recent 500KV line operations

Galina S. Antonova and Tommy Jansson, Hitachi Energy  
Tom Roseburg and Steve Laslo, Bonneville Power Administration

## Abstract

The effect of sample synchronization on analog samples based differential protection is well known and understood. Sampling must be synchronized within an acceptable margin and samples taken at the same time, i.e., samples with equal timestamp values, are used in differential calculations. Given the importance of accurate synchronization, protective relays normally use supplementary information included with distributed time to determine time quality. But what if valid quality is sent with invalid time, and the relays are unaware of this ?

An analysis of two 500KV line operations on California Oregon Intertie (COI) lines, both of which occurred on February 5, 2021, 15 minutes apart, led to answering the above question in great level of details. These events were re-created in multiple laboratories for testing and detailed investigations to determine the exact cause and effect sequence and the true root cause.

Details of these investigations including field event records, synchronization and communication mechanisms, clock and relays behaviors, per the implemented algorithms are presented and explained in the paper. Thanks to the in-depth embedded debugging capabilities, root cause was conclusively determined for both events, using per message-based indicators and debugging data. Specifics of this detailed analysis, conclusions made, and corrective actions suggested are covered.

## 1. Introduction

Various conference papers are written about line protection philosophy and schemes deployed by Bonneville Power Administration (BPA), interested readers can refer to [1], [2]. A concise summary is provided below.

The current BPA 525kV line protection consists of a protection IED that includes single pole line differential protection operating in parallel with single pole phase distance protection. Protection communication to the remote terminal is relay to relay. The IEDs are configured with three fiber optic interfaces for communication to the remote terminals. Two of the interfaces have multimode transceivers and are operated at 64kbps using the IEEE C37.94 protocol [3]. They can be directly connected to an optical interface card in a channel bank. The two multi-mode interfaces allow the IED to operate on three terminal lines. The typical one-way delay of the communications channels is about 1 cycle. The third communications module has single mode transceivers and is setup for direct fiber communication to the remote terminal. The communications channels are setup for the differential protection. Four AC current quantities and eight digital bits are sent to the remote terminal. The digital bits are not used by the differential, so they are assigned as communications aided tripping bits for the distance relay. This allows the IED to provide complete protection on a single Digital Signal 0 (DS0) channel, which is the most common case in BPA.

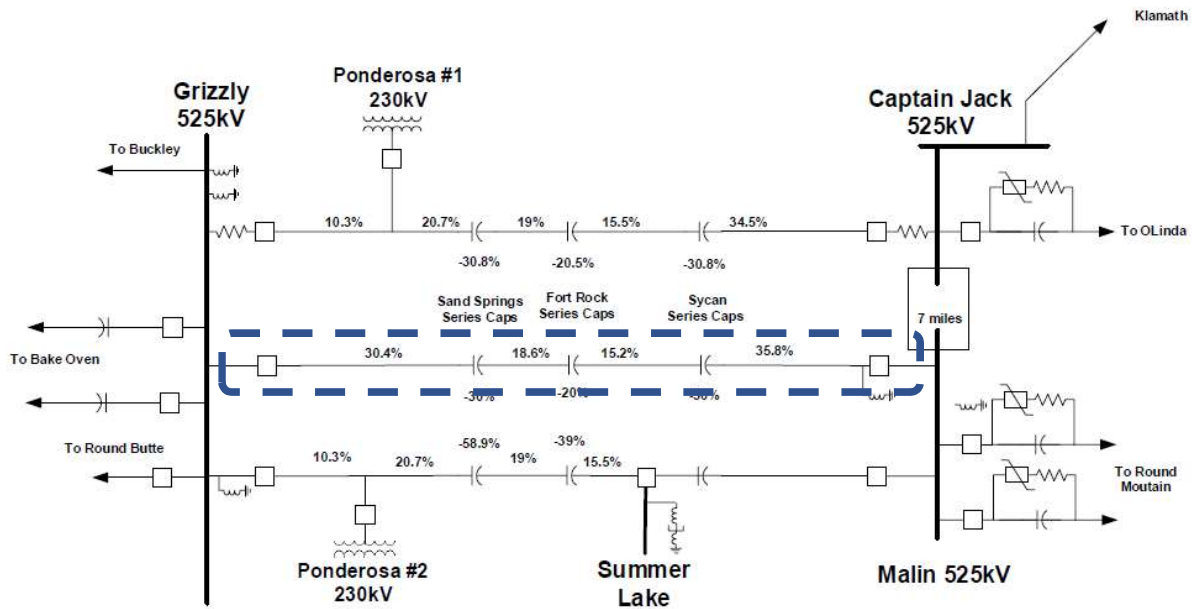
The line differential relays were included in the protection scheme because they can have more sensitive settings than phase distance relays. This gives the capability to operate single pole for much greater levels of ground fault resistance. Line differential relays operate on local and remote currents so all terminals, even terminals with weak sources, have the same operating quantities. Therefore, all terminals trip at about the same time. Line differential relays also do not have a problem with heavy line loads, series capacitors, three terminal lines, terminals with weak sources, sub-harmonic oscillations, system swings, mutual coupling, faults on parallel lines, and cross-country faults. A great advantage of line differential relays is they have fewer settings and are much easier to set.

Line differential relays do have a couple of limitations that must be addressed. Differential relays do not provide backup protection for equipment at the remote terminals. Also line differential relays are communications dependent. The differential will automatically disable itself on loss of time synchronization if a communications path switching event creates excessive asymmetrical delays between the transmit path and the receive path. BPA always install redundant relays, but loss of communication and loss of time synchronization can significantly impact the line differential protection.

These two main well-known dependencies of line current differential protection are reliable communication and precise samples synchronization. Dependencies of line protection on time synchronization are covered in [1], and overall challenges that time synchronization presents to any protection and control scheme are described in [4]. BPA power system events analyzed in this paper provide an opportunity to better understand the dependency on the samples synchronization, as well as consider methods for achieving a more reliable samples synchronization. Specifically, events described cover the situation when incorrect time was reported as good by a defective clock. How relays can defend against this, and what measures could be taken is the main focus on the paper.

## 2. Line current protection operation events

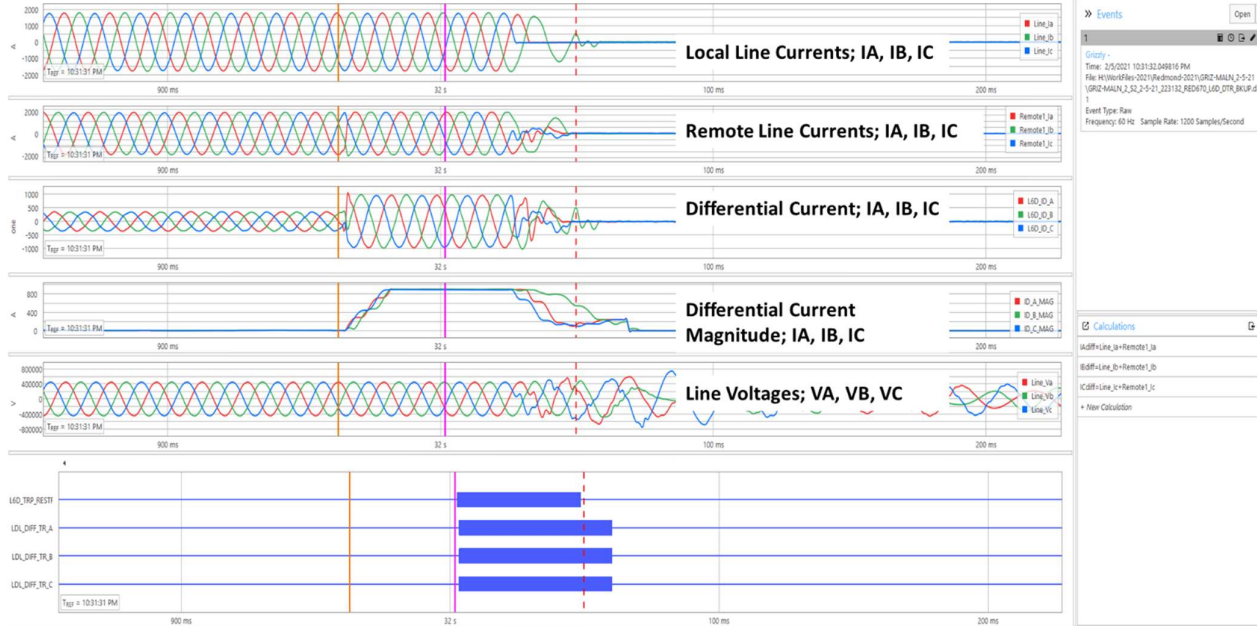
500kV intertie lines of BPA system are shown on Figure 1. Presence of series capacitors should be noted as well as long length of these lines: the line involved in the discussed events (center Grizzly-Malin) is 178.49 miles long.



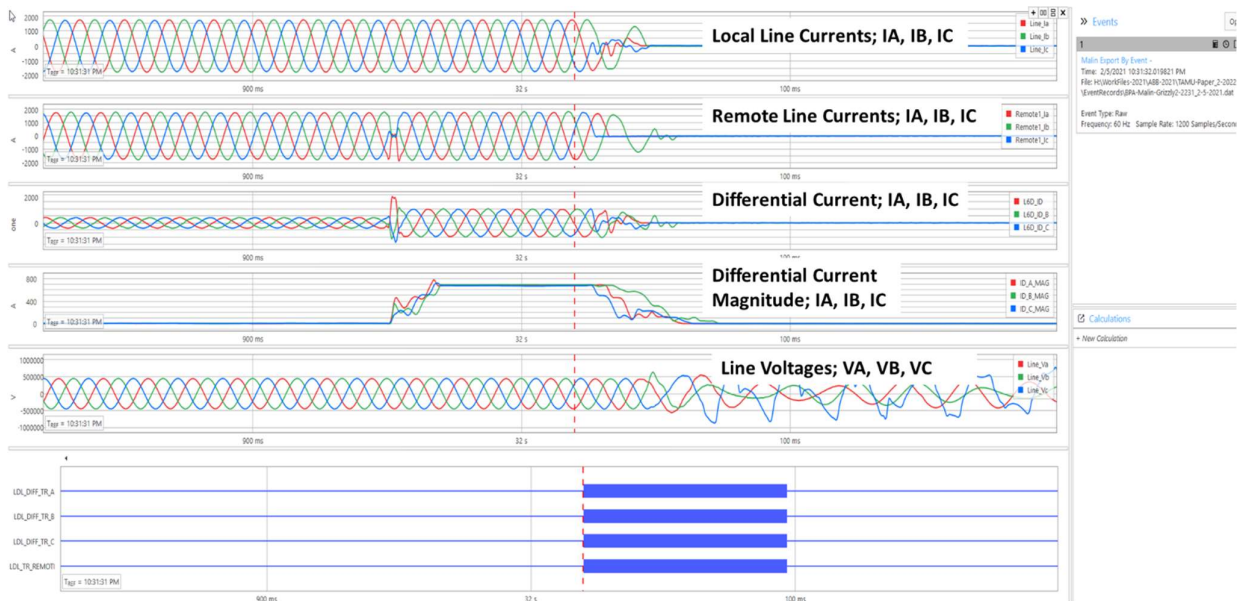
**Figure 1.** 500kV intertie lines, with Grizzly-Malin line shown in the middle.

In the late evening on February 5, 2021, BPA system experienced two 500KV line operations at California Oregon Intertie (COI) lines 15 minutes apart. Line current differential elements operated unexpectedly. At the time of these events, it was known that clock at one line terminal was experiencing some issues.

The first event had a time glitch that caused a slight time shift in the remote currents. Instead of blocking the differential the relay locked in the time error and appeared to unblock the differential allowing it to trip. Event records below show that both Grizzly and Malin terminals tripped on 87L element (Figure 2a). One can observe AC waveforms distortions, these are further analyzed in this paper.



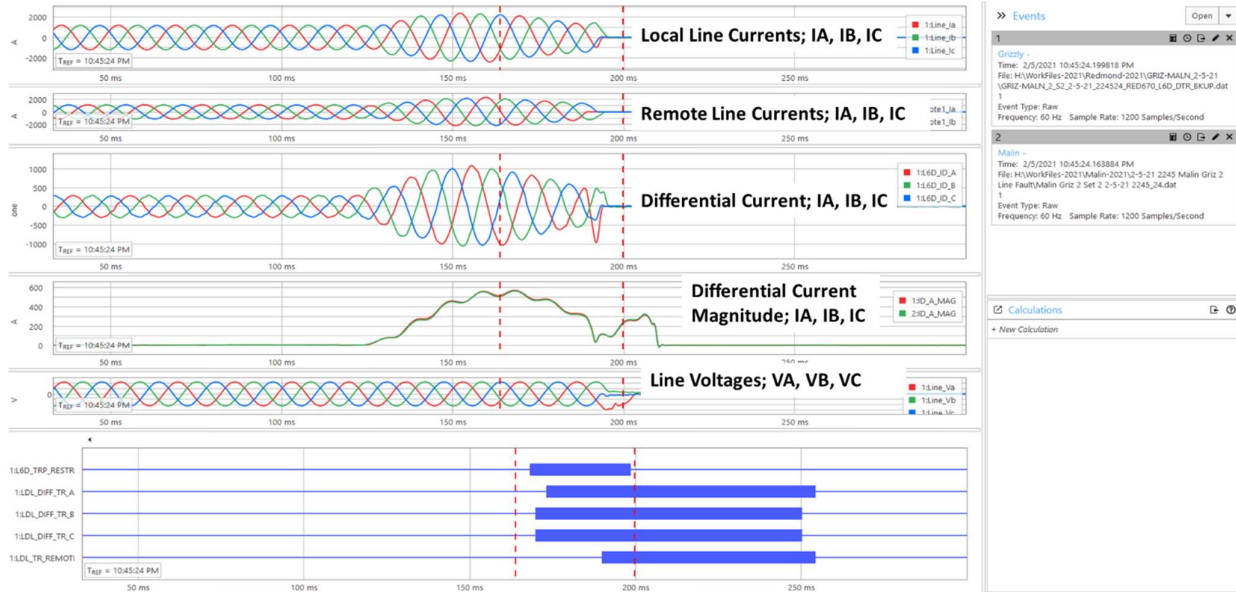
a) Grizzly terminal record



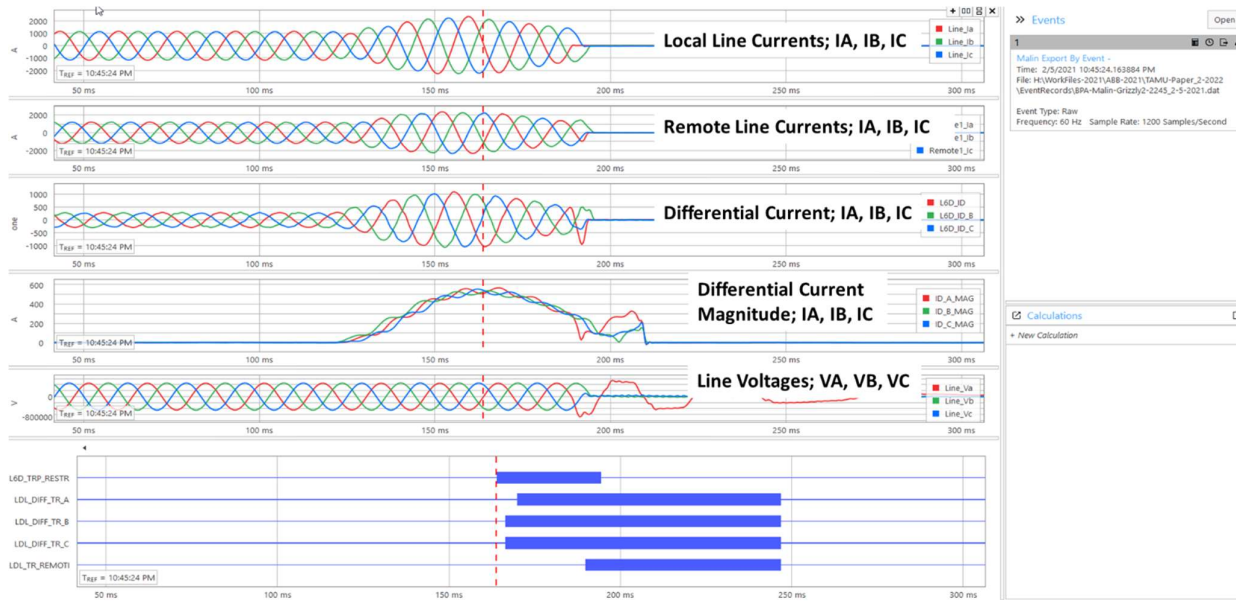
b) Malin terminal record

**Figure 2.** Event 1 records at Grizzly terminal (a) and Malin terminal (b)

The second event occurred 15 minutes later when the line was returned to service and one of the series capacitors was re-inserted. In this case the trip was caused by the increase in current when the capacitors were inserted, and the clock time was still in error. The clock was apparently stable after the first event and the differential remained in service with the time error. Both terminals tripped on 87L elements, as shown below for Grizzly terminal (Figure 3a) and Malin terminal (Figure 3b).



a) Grizzly terminal record



b) Malin terminal record

**Figure 3** Event 2 records at Grizzly terminal (a) and Malin terminal (b)

### 3. Event analysis

Detailed events analysis was performed at BPA laboratory, as well as relay vendor facilities at customer support and R&D levels. Details of these investigations are described below.

First, it should be noted that line current differential element uses relay to relay communication to obtain current samples from remote terminal. Line Data Communication Module (LDCM) performs this function. While exchanged data format is proprietary, IEEE C37.94 data framing specified in [3] is used.

Relay to relay communication occurs every 5ms and includes analog data samples (6 samples in one message) and supplementary information such as time synchronization mode, time accuracy and debugging information.

To synchronize local and remote currents BPA uses two methods: GPS mode (primary) and Echo mode (backup). If GPS mode fails, relays switch to Echo mode.

#### 3.1 Testing and event analysis at BPA laboratory

BPA has a universal Real Time Digital Simulator (RTDS) test setup for testing with both conventional copper and communication-based signals. Flexibility and benefits of this setup are described in detail in [5]. This setup has proven to be very useful for testing these events as well. Setup utilized included channel bank and communication channel emulator, refer to Figure 4. Firmware loaded to the relays during the events as well as the latest approved firmware were tested.

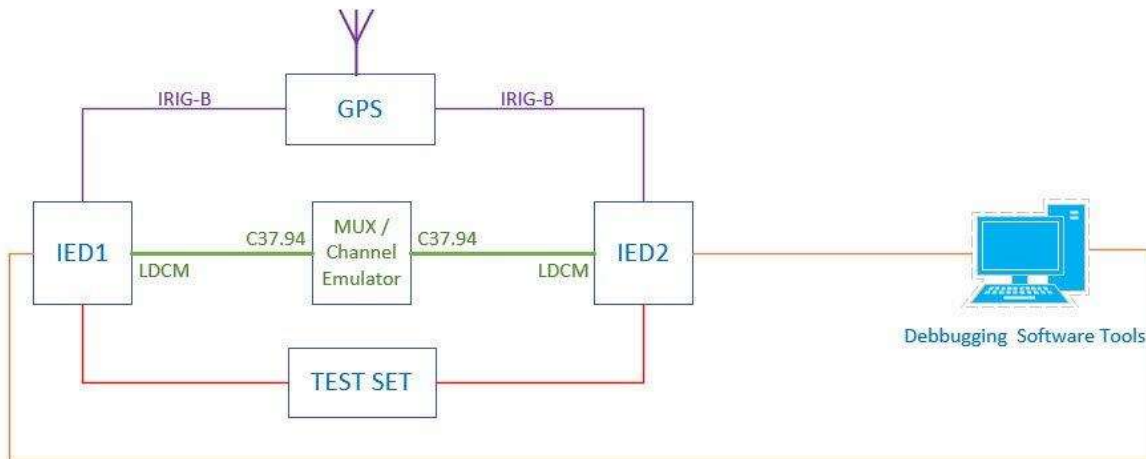


Figure 4. BPA test setup

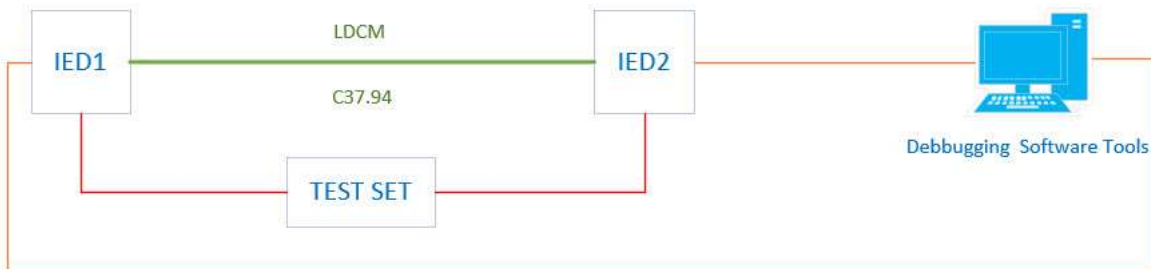
To emulate time difference between terminals, BPA creatively applied phase shift, to determine phase shift limits for a given Idmin setting.

Interestingly, during BPA tests similar to Event 1 behavior with similar oscillography signature was observed for other conditions, including a series capacitors bypass test and even an idle test with no injections. Ability to re-create such similar behavior assisted greatly in event analysis performed by both utility and relay vendor.

### 3.2 Testing and events analysis at the relay vendor

Relay vendor as well created a test setup at two different levels: product support and R&D to fully understand what happened and why. Presence of detailed internal relay logs and special debugging tools allowed to conduct a detailed and conclusive analysis.

Test setup at the product support site is shown on Figure 5.



**Figure 5.** Test setup by relay vendor product support team

Note that direct fiber connections for relay-to-relay communication were used. This setup was used to determine exactly what happened during BPA events, by looking inside specific relay to relay communication messages which carry analog samples and samples synchronization status. This was made possible by special debugging software tools used.

#### 3.2.1 Event 1 analysis

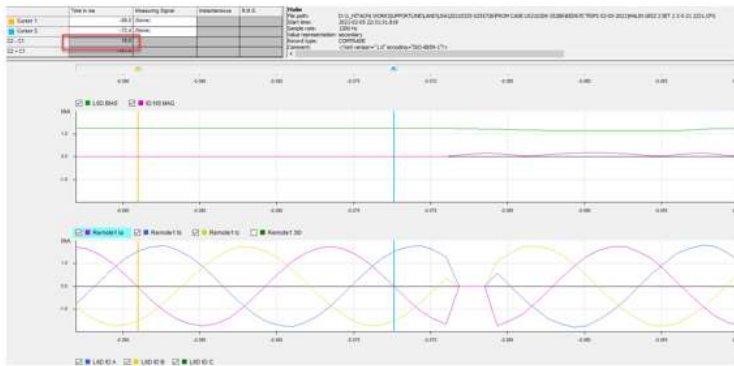
Event 1 occurred at 22:31 pacific time on 2/5/2021. To obtain an absolute local time reference, oscillography data was related to the relay's internal log data, as internal log data do not have complete time stamps including the date, only ms and  $\mu$ s. Figure 6 shows alignment between Event 1 records and internal relay log data that confirms correct log file selection.

Next, AC periods were examined. Before the event both records from both line terminal ends had steady 16.667ms period, as expected for a 60Hz system. During the event, AC period at Malin for the remote current from Grizzly extended to 18.7ms, and AC period at Grizzly for the remote current from Malin shrunk to 14.6ms. Refer to Figures 7a and 7b. Note that the actual time difference of the distorted remote current waveform at Malin is 3.3ms, while the duration of the zeroed current values is 2.1ms. After these distortions periods at both terminals returned to the nominal 16.667ms period duration.

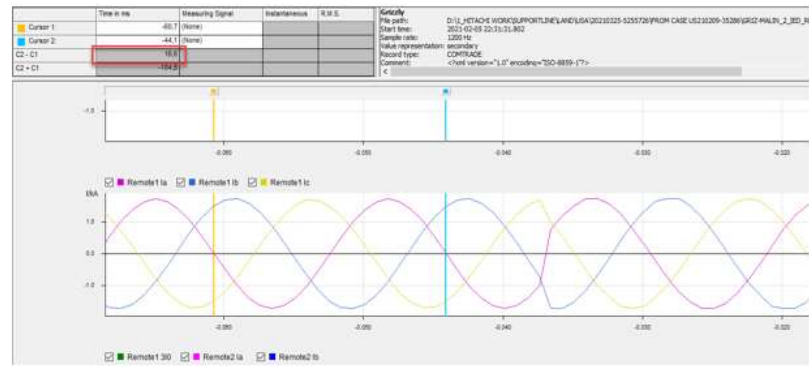
Figure 7b also shows that the time difference between COMTRADE records timestamps is 17ms (819-802) that includes 15ms communication channel delay and relay processing times. BPA's requirement for communication delay is within 1 power cycle delay for primary communication path, and within 1 ¼ power cycle for backup communication path.

Analysis at the relay-to-relay communication message level followed. Debugging software tools allow to look at each relay-to-relay communication data individually and examine its content for both analog data and status information.

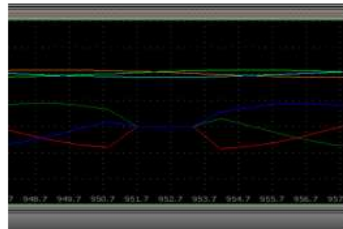
Current samples are communicated between line terminals every 5ms (6 samples per message) using IEEE C37.94 framing.



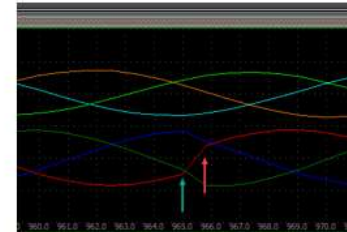
Malin Disturbance Record: remote Grizzly current



Grizzly Disturbance Record: remote Malin current

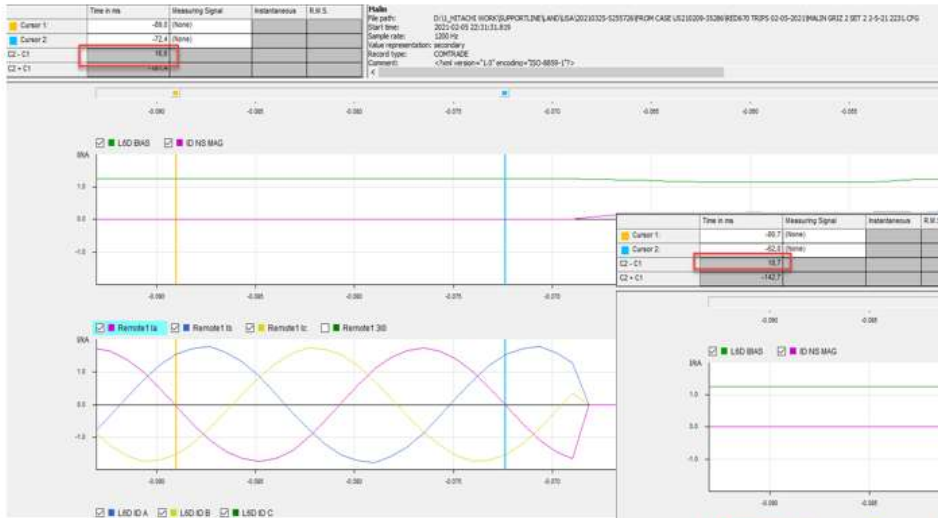


Malin internal log file data



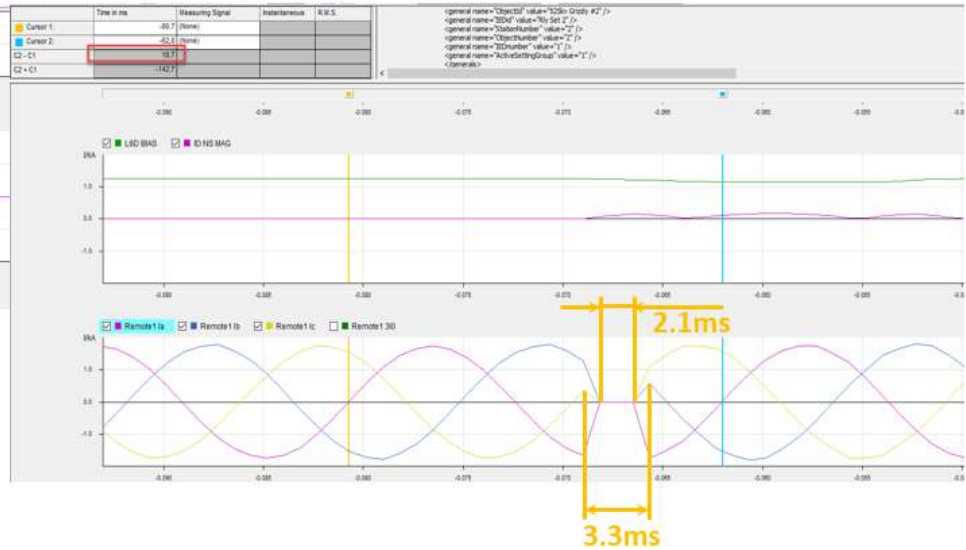
Grizzly internal log file data

Figure 6. Relating Event 1 record to internal relay log data for Malin and Grizzly relays



2021-02-05 22:31:31.819

During: period extended to **18.7ms !**

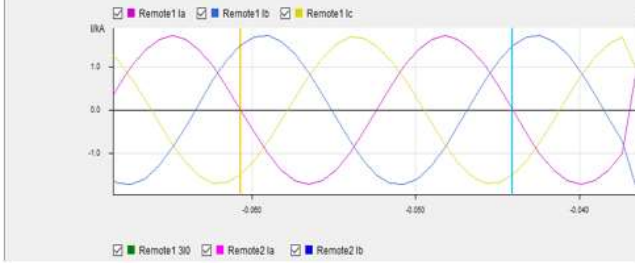


Before the event: period **16.6ms**

AC waveform discontinued for **3.3ms**  
 0 data recorded for **2.1ms**

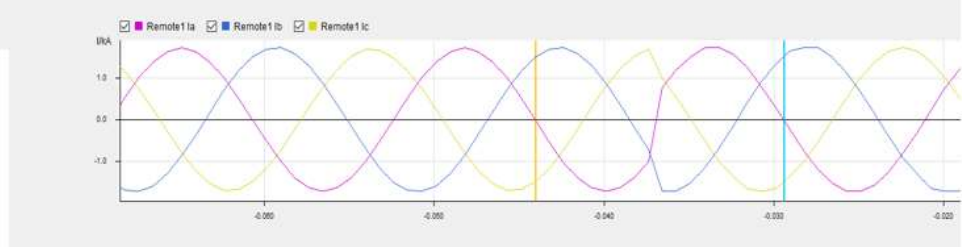
Figure 7a. Frequency/period checks for Malin relay for remote current from Grizzly

|           | Time in ms | Measuring Signal | Instantaneous | R.M.S. |
|-----------|------------|------------------|---------------|--------|
| Cursor 1: | -50.7      | (None)           |               |        |
| Cursor 2: | -44.1      | (None)           |               |        |
| C2 - C1   | 16.6       |                  |               |        |
| C2 + C1   | -164.8     |                  |               |        |



Before the event: period **16.6ms**

|           | Time in ms | Measuring Signal | Instantaneous | R.M.S. |
|-----------|------------|------------------|---------------|--------|
| Cursor 1: | -44.0      | (None)           |               |        |
| Cursor 2: | -29.4      | (None)           |               |        |
| C2 - C1   | 14.6       |                  |               |        |
| C2 + C1   | -73.4      |                  |               |        |



2021-02-05 22:31:31.802 Grizzly record

2021-02-05 22:31:31.819 Malin record

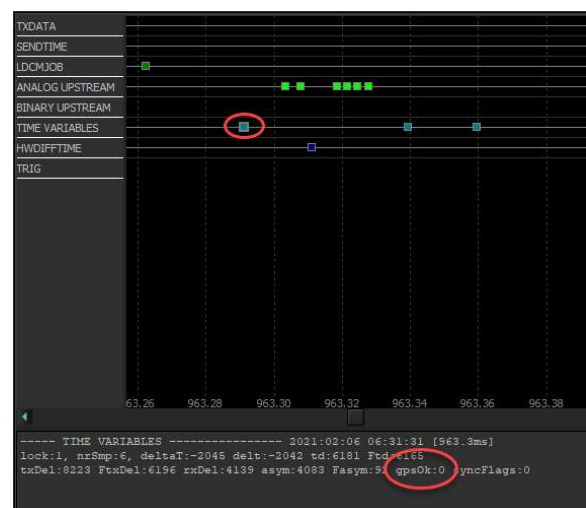
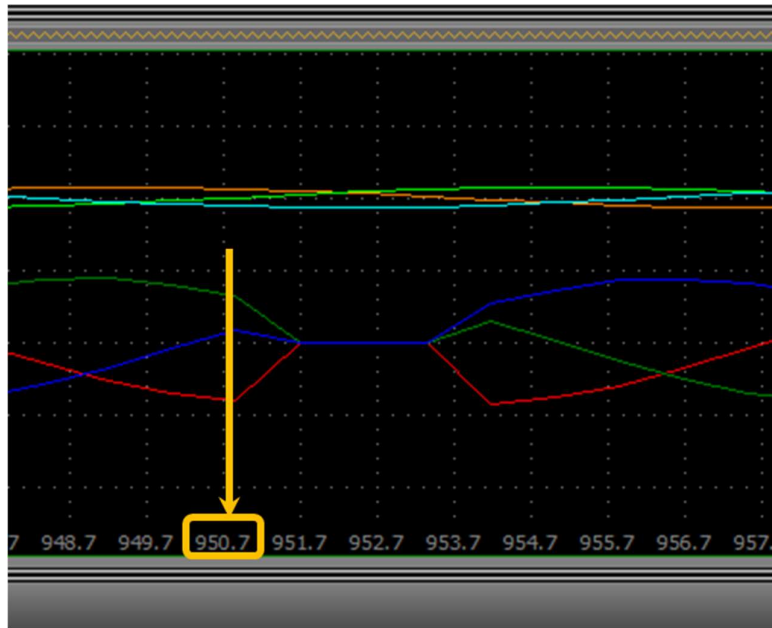
Delta: **15ms** com delay + processing

During: period shrunk to **14.6ms !**

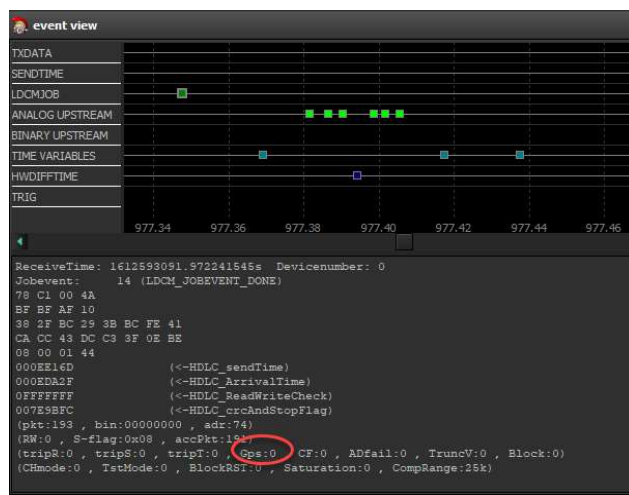
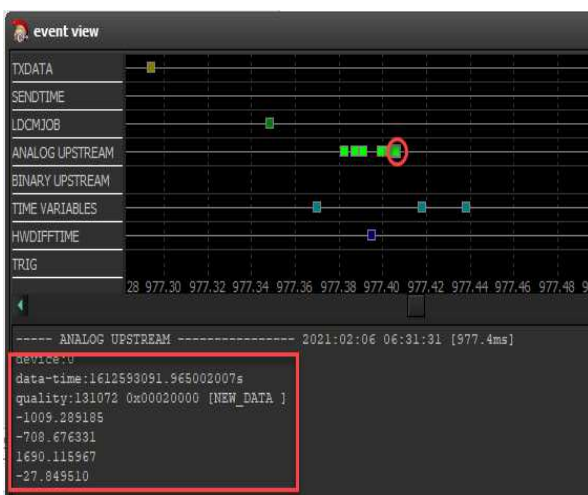
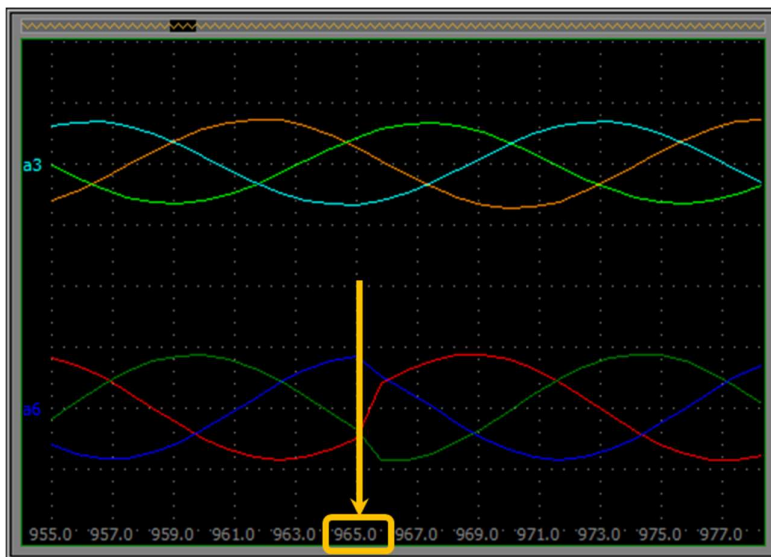
Figure 7b. Frequency/period checks for Grizzly relay for remote current from Malin

Examining the internal log in the Malin relay, it was concluded that at the start of the event its remote relay was operating in Echo mode. Figure 8 shows relay-to-relay communication message with 950.83ms time stamp received at Malin. Likewise, the associated message that arrived at Grizzly shown with 965.0ms timestamp also indicates that Malin relay sending it was in Echo mode. This is shown on Figure 9.

These timestamps are already adjusted for CPU processing in line current differential calculation and include end-to-end delay correction performed by the Echo method. 15ms channel delay is also included. It should also be noted that 50Hz systems use samples every 1ms, and 60Hz systems use samples every 0.83ms.



**Figure 8.** Details of relay-to-relay communication message received at Malin, 950.83ms

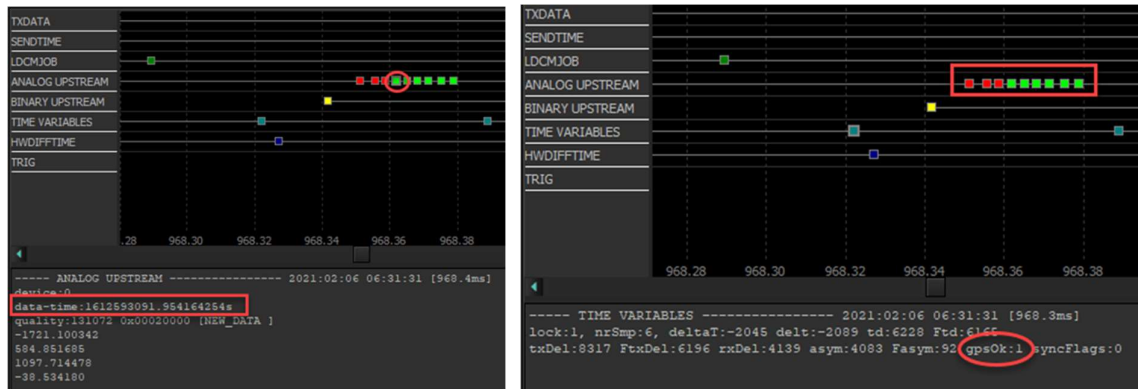


**Figure 9.** Details of relay-to-relay communication message received at Grizzly, 965.0ms

Thus, before Event 1 both relays were in Echo mode. An assumption was made that a clock issue experienced at Malin initiated a transition to Echo mode some time prior to the event. It should be noted that at the start of Echo mode operation a known good GPS time is frozen and used. Up until the times shown in Figure 8 and 9 regular and proper 16.667ms AC periods were observed.

The next relay-to-relay communication message that arrived at Malin from Grizzly end carried GPS=Ok flag, indicating that a transition back to GPS mode has occurred. Figure 10 shows details of this message. Note a 3.3ms timestamp jump from 950.83ms to 954.1ms.

This jump indicates that time at the (properly functioning) GPS clock at Grizzly end is around 3.3ms ahead of time at Malin terminal



**Figure 10.** Details of next message received at Malin, 954.1ms

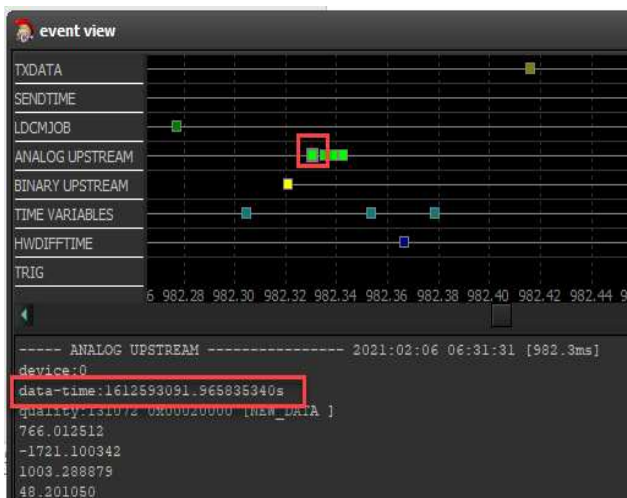
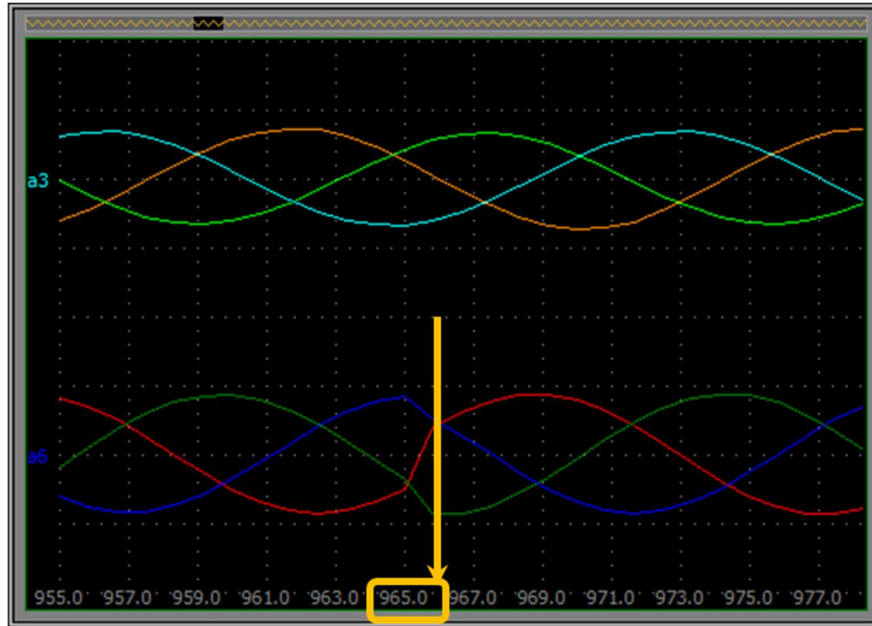
As explained earlier each relay-to-relay communication message carries 6 samples of analog data. Relays require analog samples every 0.83ms for 60Hz system (every 1ms for 50Hz system) to perform differential calculation.

This first message in GPS mode received at Malin terminal, was interpreted as 3.3ms of data was missing, i.e., no data was provided for times at approximately 951ms, 952ms and 953ms. As relay CPU needs samples every 0.83ms, zero values were provided for these samples. These are seen as red dots on Figure 10.

Per Figure 7a, the measured duration of the zeroed current is about 2.1ms, while the duration of the disturbed AC waveform is about 3.3ms.

Samples insertion with zero values explains period extension by about 2.1ms. These samples were inserted unnecessary, in addition to the correct AC data, because of the timestamps jump.

At Grizzly end, the next received message as well had GPS flag set to OK. Details of this message are shown on Figure 11. Note that the timestamp used is exactly the expected next time stamp value: 965.83ms. However, as seen on Figure 11, only 4 samples out of 6 were passed to CPU for processing. 2 samples were discarded for having timestamps in the past.



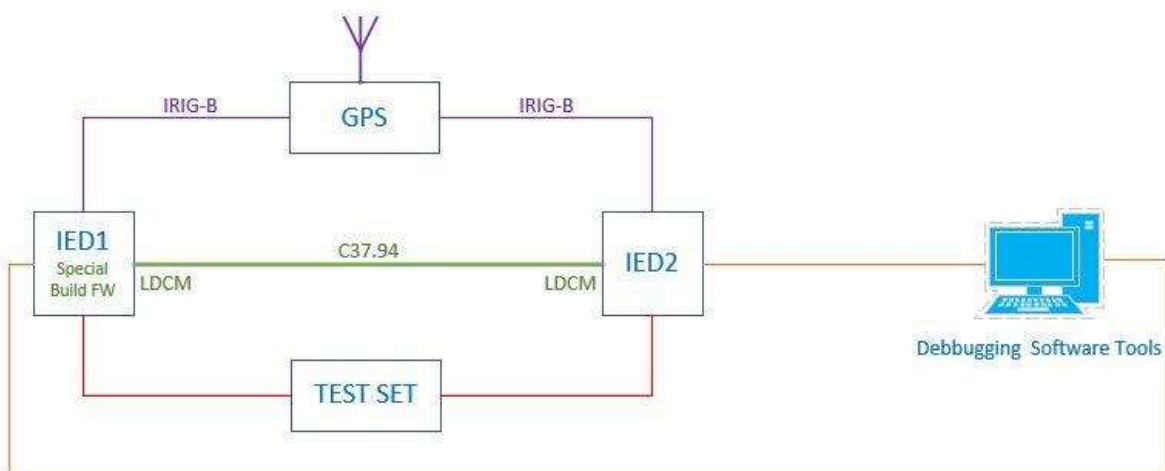
**Figure 11** Details of next message received at Grizzly, 965.83ms

Discarding two data samples with valid data with timestamps in the past explains the AC waveform period reduction by about 2.1ms in Grizzly record for the remote current.

The following overall understanding of the Event 1 was obtained.

1. GPS clock at Malin terminal experienced a sudden time jump backwards by approximately 2.1ms. The clock, however, continued to declare good time quality, despite of this change.
2. The 2.1ms time jump initiated a transition of both relays into Echo mode. Note that per relay logic its time needs to be within  $16\ \mu\text{s}$  of station clock to operate in GPS mode. A known good and frozen GPS time is used to initiate Echo mode operation.
3. As the station clock at Malin continued to report good time quality, Malin relay trusted it and started gradually adjusting its time to the (unknowingly incorrect) GPS time at the rate of  $50\ \mu\text{s}/\text{s}$ , per BPA setting. Note that it takes 41 seconds to adjust to for 2.1ms offset at the  $50\ \mu\text{s}/\text{s}$  rate.
4. When the difference between the adjusted local time and the (incorrect) GPS time became to be less than  $16\ \mu\text{s}$ , Malin relay changed back to GPS mode and locked to the unknowingly incorrect GPS time.
5. At this point time at Malin terminal was behind time at Grizzly terminal time by approximately 2.1ms. Timestamps for current samples were offset by the same amount. This time/phase shift resulted in calculated (false) differential current exceeding the  $I_{\text{admin}}$  setting and led to an 87L operation.

The above Event 1 behavior was reproduced by relay vendor R&D team, which confirmed same operation. For these tests complete relay copies called “clones” were used and a special relay firmware build that allows to emulate any time shift between relay terminals. Test setup is shown on Figure 12. Note that channel simulator or channel bank were not used for these tests, only direct fiber connections.



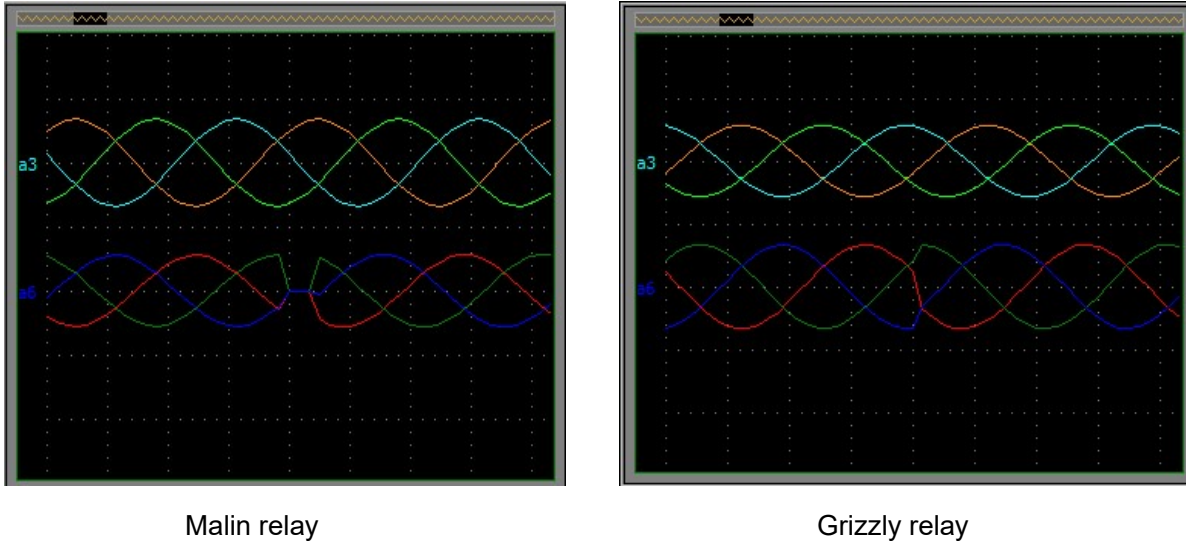
**Figure 12.** Test setup by relay vendor R&D team

To confirm achieved understanding first 2/5/2021 event was re-created by R&D tests

Initially both relays were operating in GPS mode. A negative - 2.1ms time offset was programmed to Malin relay. This corresponds to IRIG-B time being delayed by 2.1ms.

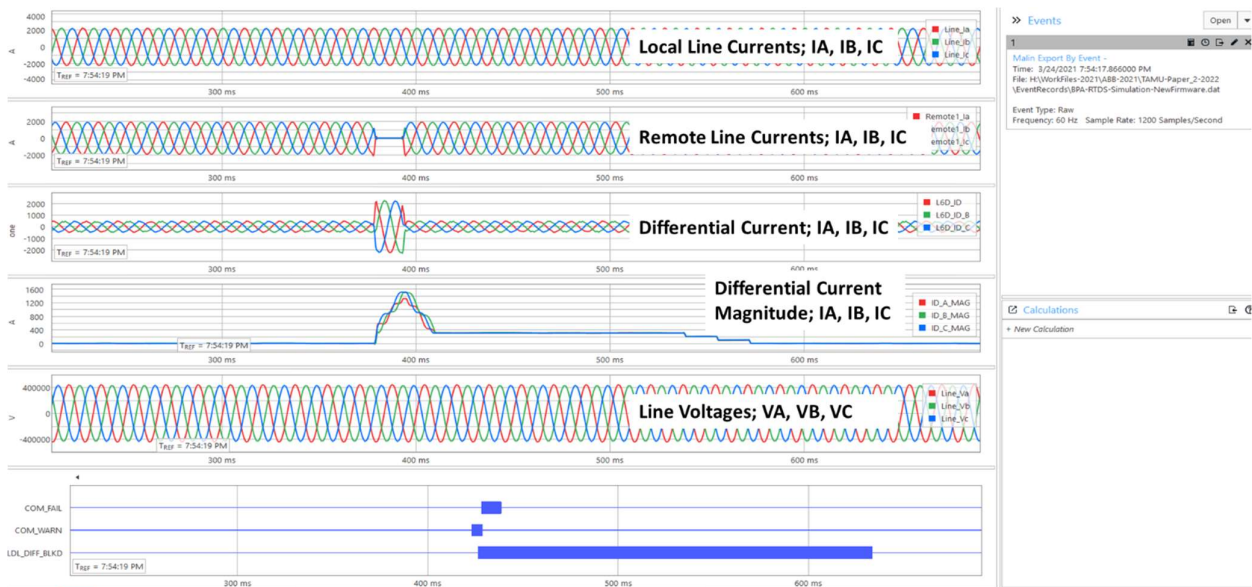
After activation of the simulated time error, both relays switched to Echo mode, as in Event 1. Malin relay also started adjusting its internal local time to the received from GPS at the rate of  $50\mu\text{s/s}$  per relay setting. When internal local time at Malin adjusted to be within  $16\mu\text{s}$  of its local GPS clock, both relays returned to GPS mode.

Malin terminal locked to GPS time with the configured negative  $-2.1\text{ms}$  time offset, current samples timestamps were also offset by  $2.1\text{ms}$ . Calculated using such timestamps differential current exceeded  $I_{\text{dmin}}$  setting and an 87T trip occurred, with nominal current injections. Figure 13 shows analog data captures from R&D tests, which are very similar to the actual event captures shown on Figure 6.



**Figure 13:** Relay vendor R&D test results, matching Event 1 data

An interesting anomaly that assisted with Event 1 analysis was also observed during BPA testing.

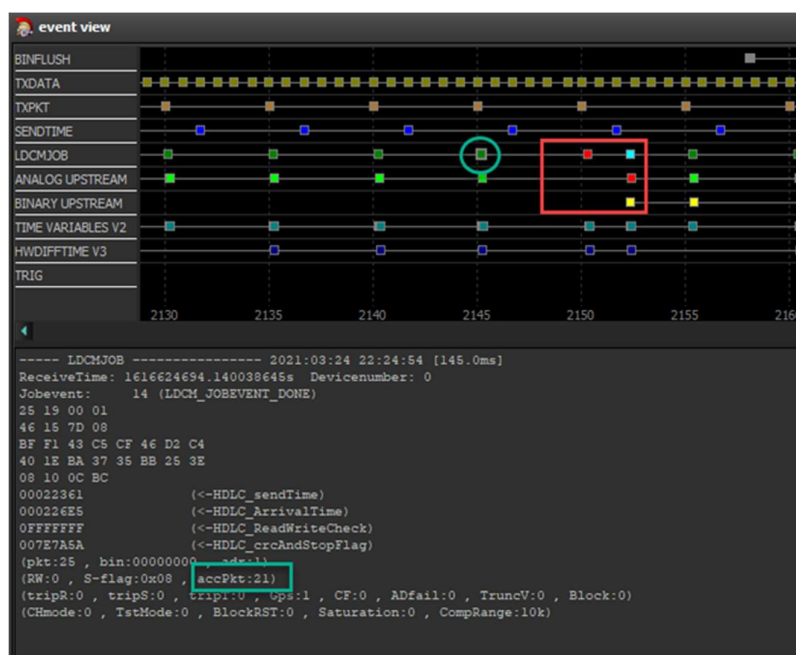


**Figure 14.** Record for series capacitor bypass test

It was noted that during series capacitor bypass test, a glitch in analog signals, similar to the one in Event 1 occurred. Its timing was also consistent and predictable: it happened about 1 second after capacitor bypass event. Figure 14 shows a record for such series capacitors bypass test. It should be noted that this test was performed with the latest approved by BPA firmware, which actually blocked differential in response to this glitch. More discussion on this is provided in Section 4.2. Relay vendor team analyzed this glitch in analog data as well.

First, it was verified that the glitch occurrence is unrelated to samples synchronization issue experienced in Event 1. This is because all AC waveforms in this event are proper and maintain 16.667ms period consistently.

Second, internal relay log files with details of relay-to-relay communication messages were examined. Figure 15 shows relay-to-relay communication messages 21, 22 and 23 sent during the glitch event.



**Figure 15.** Message details for the glitch in analog data: Messages 21, 22 and 23

Message 21 arrived with healthy flags and was received correctly. Message 22, however, colored in red had multiple issues. As shown on Figure 16 below, a Cyclic Redundancy Check (CRC) error was reported, as well as a lost/discarded message. Message 23 again had valid flags and was received correctly.

Following this analysis of received messages, message 22 was examined at the transmitting end. Figure 17 captures details of the healthy status of message 22 at the transmitting end.

Based on the above information it was concluded that the glitch in analog data was caused by lost data samples due to corrupted relay-to-relay communication message which had a CRC error. The source of the CRC error was concluded to be outside for the relays, inside BPA test setup which includes communication channel emulator and channel bank.

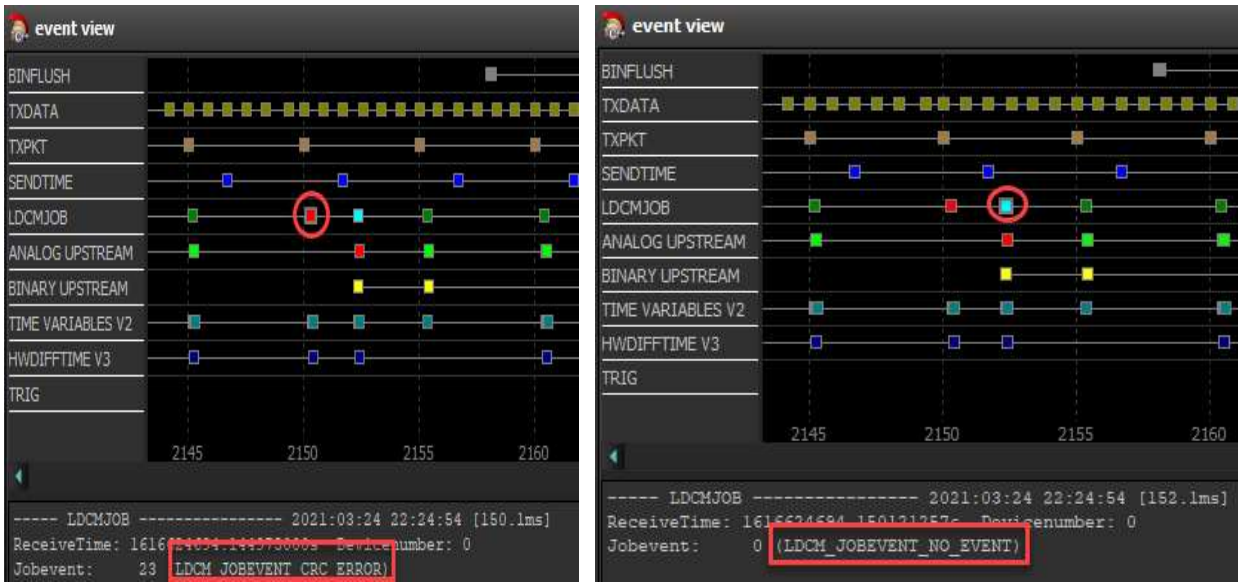


Figure 16. Details of message 22 details for the glitch in analog data

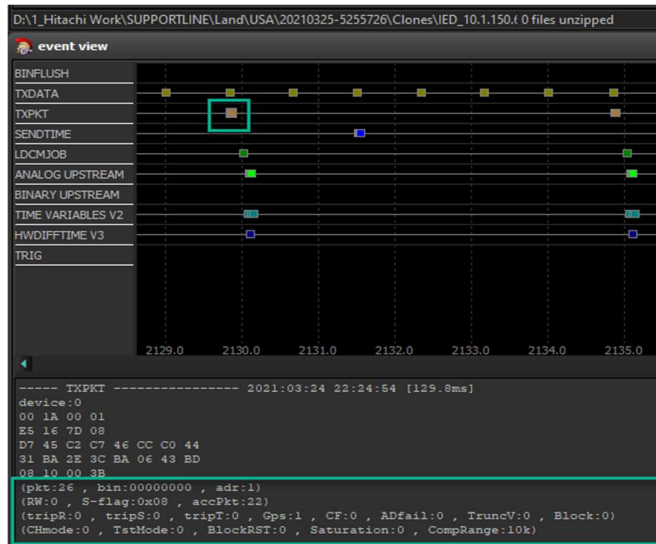
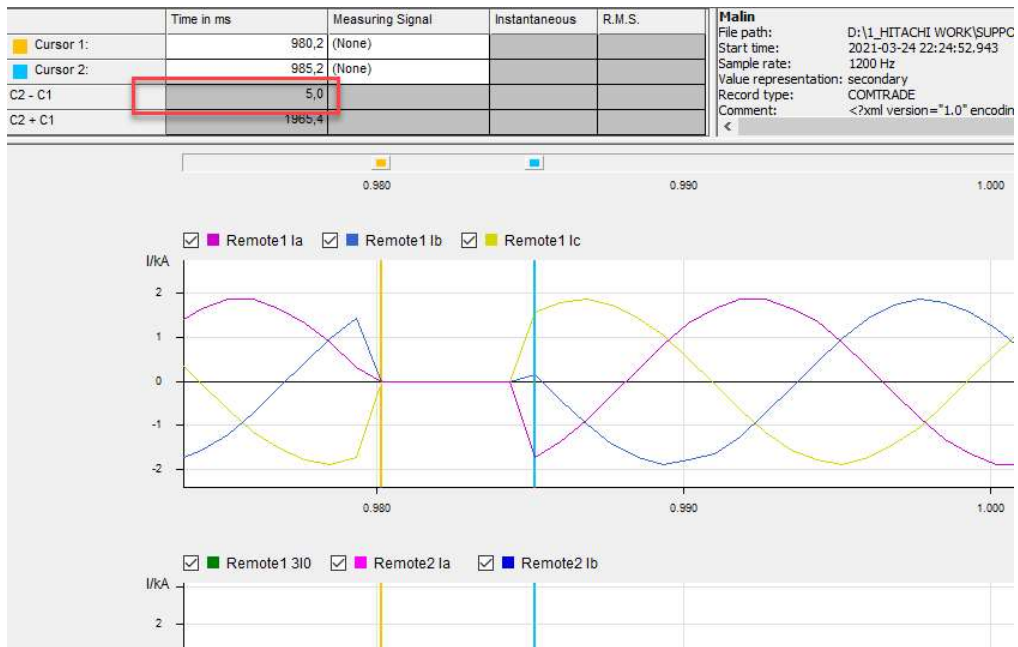


Figure 17. Details of message 22 at the transmitting end

Figure 18 as well show that analog samples are missing for exactly 5ms which corresponds to losing a single relay-to-relay communication message.

It is further interesting to note that a similar glitch was observed by BPA without any analog data injections, on a change of a test system state. These observations lead to following general conclusions:

1. A glitch in analog data is caused by loss or replacement by zero of analog samples data
2. Root causes loosing or replacing analog samples data vary and include
  - a. Sample synchronization error as observed in Event 1
  - b. Communication channel impairments resulting in CRC errors, as observed in 1<sup>st</sup> glitch
  - c. Com channel or test equipment influences, as observed in second glitch observed.



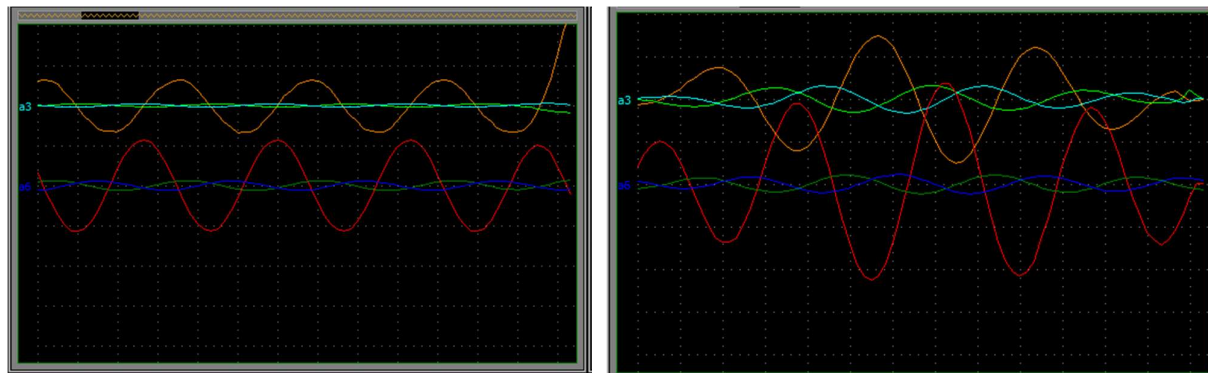
**Figure 18.** Data interruption for 5ms upon loss of a single message

### 3.2.2 Event 2 analysis

Event 2 occurred at 22:45 hours on 2/5/21 after Grizzly-Malin line was returned to service, and series capacitors were re-inserted.

This event analysis was significantly simpler than Event 1 analysis. The same method of using disturbance records and internal relay logs was used.

Right away it was identified that a phase shift was present prior and during the event. Figure 19 shows that the same phase difference was observed.



**Figure 19.** Phase difference observations before and during Event 2

Analysis of internal log messages identified that both relays were in GPS mode prior and during the event, as shown on Figures 20 and 21. It was also known that clock issue at Malin was not resolved.

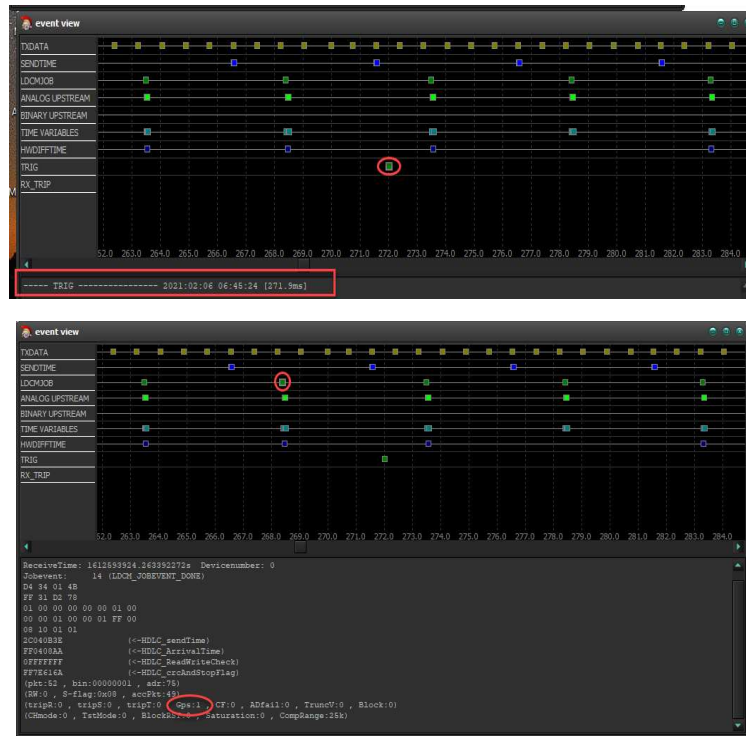


Figure 20. Malin relay log during Event 2

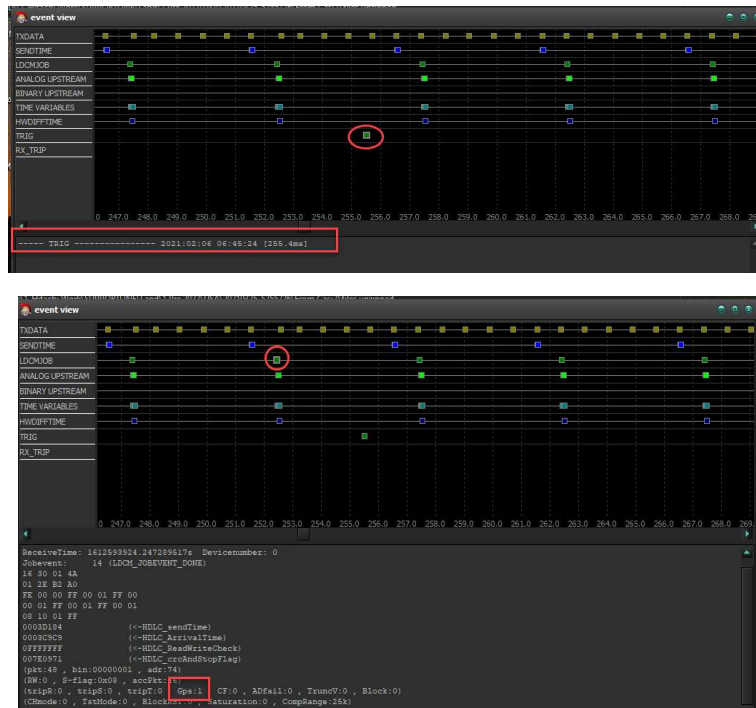


Figure 21. Grizzly relay log during Event 2

Per relay logic the  $16\mu\text{s}$  check tracks time change between internal relay clock and local GPS in sequential synchronization messages, and a constant and precise time offset of 2.1ms does not trigger a transition to Echo mode.

When Grizzly-Malin line was returned to service its terminals had a constant time offset of approximately 2.1ms. Differential calculation was summing current samples taken at different times, yet the false differential current did not exceed  $I_{\text{dmin}}$  setting, as the line load was light.

When series capacitors were re-inserted higher transient currents occurred and the resulting false differential current did exceed  $I_{\text{dmin}}$  setting and caused an 87L trip. These transients served as a saving grace that prevented lightly loaded line from being in service without adequate protection for longer, with a possibility of tripping on adjacent line events as well.

#### 4. Discussion on remedies

Various remedies were considered in response to 2/5/21 events to prevent such occurrences in the future. These include monitoring and replacement of specific clock types, upgrading to the latest approved relay firmware, modifying relay logic for increased resilience, and redesigning time distribution network to use redundant clocks, including consideration on using Echo mode only.

##### 4.1 Clock behavior analysis

Unfortunately, a detailed clock behavior analysis was not performed for the 2/5/21 events. After both events a site technician, however, observed that the value in Straight Binary Seconds (SBS) field did not align with the value in binary seconds field (SS) in the IRIG-B frame sent by the clock. This was described as an IRIG-B framing error. As various clock misbehaviors were noted before, field personnel power cycled the clock.

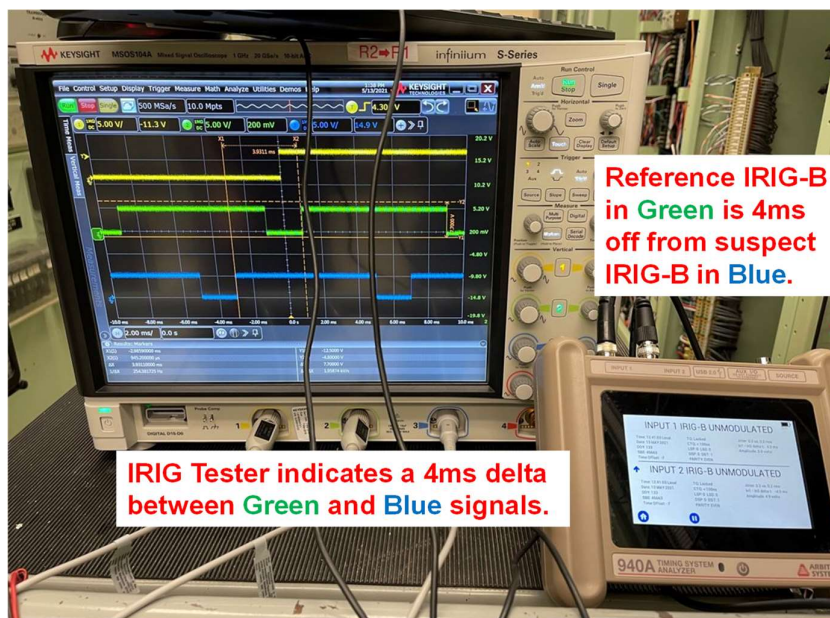
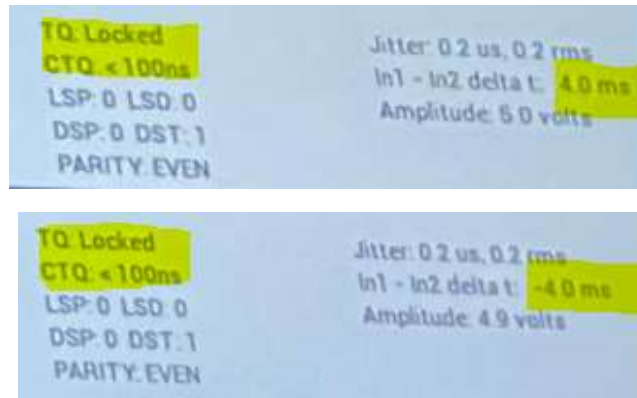


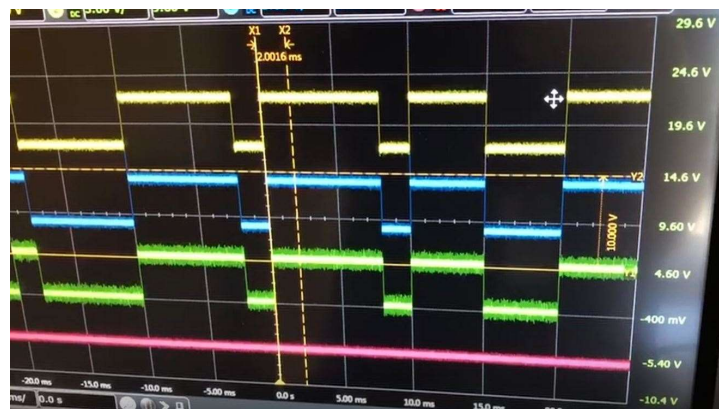
Figure 22. Oscilloscope and IRIG-B analyzer registration of 4ms clock jump

Similar behavior for a clock from the same vendor was observed after the described events. Figure 22 documents a clock jump to 4ms, as shown on an oscilloscope screen. Note that Time Quality (TQ) and

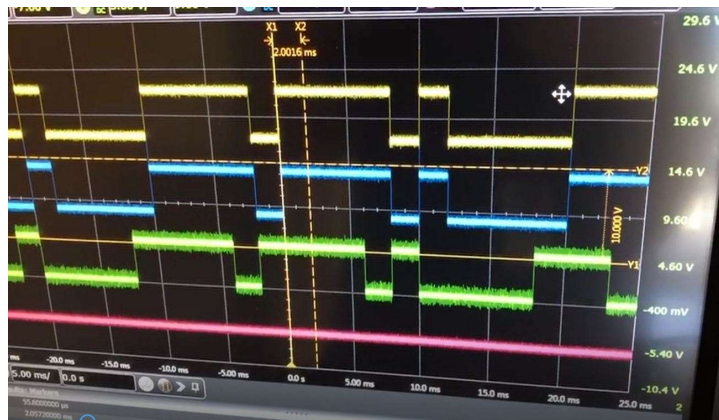
Continuous Time Quality (CTQ) fields in IRIG-B frame indicate that the clock is locked, and its accuracy is within 100ns, see Figure 23. At the same time a constant and precise time offset of 4ms is present.



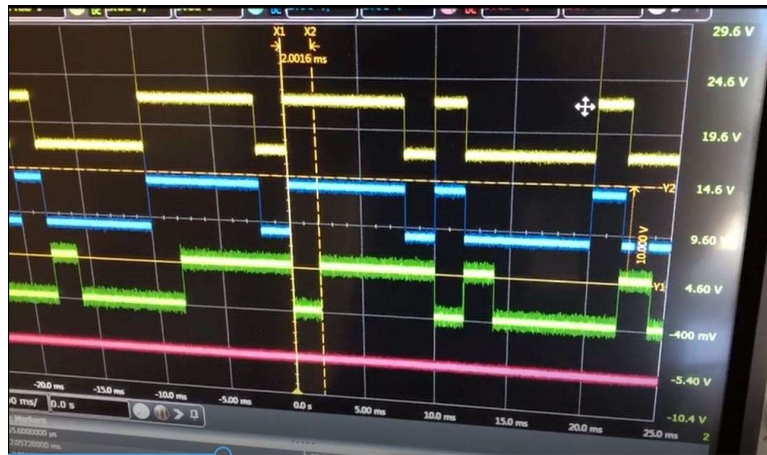
**Figure 23.** IRIG-B analyzer data showing 4ms offset while TQ and CTQ fields show good quality. Another strange behavior was experienced with the same vendor clock manifested itself in on-going variations in  $\pm 2$ ms range. This was captured in a video; snapshots are provided on Figure 24.



a) Initial state



b) State with negative 2ms difference

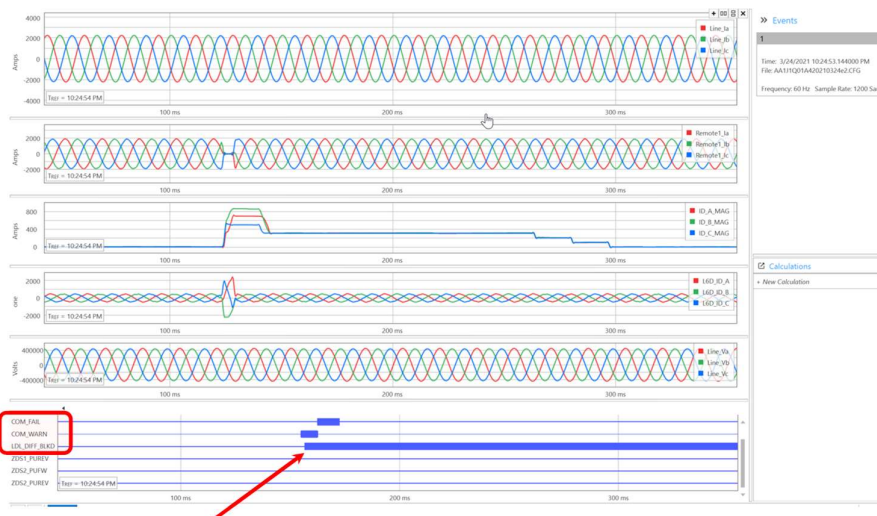


c) State with positive 2ms difference

**Figure 24.** Snapshots of clock variations in  $\pm 2$ ms range

#### 4.2 Latest approved relay firmware

The 2/5/21 events occurred before the relays were upgraded to the latest approved firmware. Testing was performed with relay firmware used during the events, as well as the latest approved firmware. As a way to create a similar to Event 1 behavior was found, it was used to test both firmware versions. Figure 25 shows the same test performed with the latest approved firmware.



**Com Warning, Com Fail and Diff Blocked (LDL\_DIFF\_BLKD)** issued for signature *similar* to Event 1

**Figure 25.** Event record captured with latest approved relay firmware

One can note the presence of Com Warning, Con Fail and Diff Blocked signals when latest approved relay firmware was used. Differential protection got blocked. Based on this test one can conclude that the use of latest approved firmware could have prevented 87L in similar to Event 1 case.

### 4.3 Relay settings

Relay settings were reviewed to identify if any changes could have prevented the 2/5/2021 events.

The first thing BPA considered was to desensitize 87L function by increasing Idmin setting. While it is not desirable to reduce sensitivity this allowed the relays to ride through various system conditions. It should be noted that BPA uses charging current compensation, so the known and set value of charging current is subtracted from differential calculation.

BPA relays are set to use GPS mode as the first choice for time synchronization, and Echo mode as a backup mode, Echo mode is activated if GPS mode fails. These settings are depicted on Figure 26.

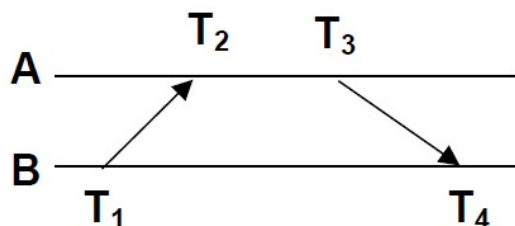
Another option for these settings is to block differential protection on GPS mode failure, instead of changing to Echo mode. While it appeared initially that it could have helped, it was concluded that it would not. This is because the blocking would happen instead of transitioning to Echo mode (Echo mode actually worked fine), while there would be no blocking on transitioning back to GPS mode, exactly when the undesired trip in Event 1 happened.

An alternative to these options is not to use GPS mode at all. In this case channel delay measurements and channel delay asymmetry measurements need to be known and set. As BPA's communication system performance varies, using Echo mode only (without initial GPS mode) is not deemed as a viable option.

| RED670-V12-AppConfig_3-2-2021-Rev2 - Application Configuration |                        | RED670-V12-AppConfig_3-2-2021-Rev2 - Parameter Settings |      |        |               |  |
|--|------------------------|---|------|--------|---------------|--|
| Group / Parameter Name   | IED Value [SG1/Common] | PC Value [SG1/Common]                                   | Unit | Min    | Max           |  |
| ✓ LDCMAnalog1_302  |                        |   |      |        |               |  |
| ✓ NAMEECH1   |                        | LDCM302-CH1   |      |        | 13 characters |  |
| ✓ NAMEECH2   |                        | LDCM302-CH2   |      |        | 13 characters |  |
| ✓ NAMEECH3   |                        | LDCM302-CH3   |      |        | 13 characters |  |
| ✓ NAMEECH4   |                        | LDCM302-CH4   |      |        | 13 characters |  |
| ✓ ChannelMode  |                        | Enabled   |      |        |               |  |
| ✓ TerminalNo   |                        | 1   |      | 0      | 255           |  |
| ✓ RemoteTermNo   |                        | 2   |      | 0      | 255           |  |
| ✓ DiffSync   |                        | GPS   |      |        |               |  |
| ✓ GPSSyncErr   |                        | Echo  |      |        |               |  |
| ✓ CommSync   |                        | Slave   |      |        |               |  |
| ✓ OptoPower  |                        | LowPower  |      |        |               |  |
| ✓ TransmCurr   |                        | CT-SUM  |      |        |               |  |
| ✓ ComFailAlrmDel   |                        | 100   | ms   | 5      | 500           |  |
| ✓ ComFailResDel  |                        | 100   | ms   | 5      | 500           |  |
| ✓ RedChSwTime  |                        | 5   | ms   | 5      | 500           |  |
| ✓ RedChRturnTime   |                        | 100   | ms   | 5      | 500           |  |
| ✓ AsymDelay  |                        | 0.00  | ms   | -20.00 | 20.00         |  |
| ✓ AnalogLatency  |                        | 2   |      | 2      | 20            |  |
| ✓ remAinLatency  |                        | 2   |      | 2      | 20            |  |
| ✓ MaxTransmDelay   |                        | 20  | ms   | 0      | 40            |  |
| ✓ CompRange  |                        | 0-25kA  |      |        |               |  |
| ✓ MaxtDiffLevel  |                        | 600   | us   | 200    | 2000          |  |
| ✓ DeadbandDiff   |                        | 300   | us   | 200    | 1000          |  |
| ✓ InvertPolX21   |                        | Disabled  |      |        |               |  |

Figure 26. Time synchronization modes settings

In Echo mode relays can only measure two-way communication delay. With an assumption of delay symmetry, relays can calculate their clock offset in relation to each other using 4 timestamps, refer to Figure 27 borrowed from [9]. Timestamps  $T_1$  and  $T_4$  are generated using clock at Terminal B, while timestamps  $T_2$  and  $T_3$  are generated using clock at Terminal A.



**Figure 27.** Echo mode operation

While Terminal A and Terminal B clocks are not exactly in sync, with an assumption of delay symmetry in A to B and B to A direction their clock offset can be calculated and accounted for. Delay asymmetry itself is simply the difference in delay in two directions. i.e.,  $Delay\ asymmetry = (T_2 - T_1) - (T_4 - T_3)$ .

First, calculating one way delay, with an assumption of delay symmetry can be done as

$$One\ way\ delay = \frac{(T_2 - T_1) + (T_4 - T_3)}{2}$$

Assuming delay symmetry, clock offset can be calculated as

$$Clock\ Offset = \frac{(T_1 + T_4) - (T_2 + T_3)}{2}$$

Clock offset (or time difference) calculation occurs every time a message with current samples arrives (every 5ms). Current samples timestamps are adjusted per calculated clock offset prior to their use by current differential calculation. Thus, clocks at each terminal can be drifting in relation to each other and still provide correctly calculate differential current.

The communication channel is expected to have a symmetrical delay or known and deterministic delay asymmetry (a settable parameter) for successful operation in Echo mode. Delay and delay asymmetry are measured dynamically in GPS mode and become “frozen” when GPS mode fails. These “frozen” measurements are used when relay transitions to Echo mode.

Two settings are provided to track communication channel performance in Echo mode: a dead band time difference variation and max time difference. The first setting allows the system to continue operation if the calculated time difference between line terminal clocks is within the set dead band value. This value is set to  $300\mu s$ . The second setting leads to blocking current differential protection if the time difference between line terminals reaches or exceeds the set maximum. This value is set to  $600\mu s$ . It should be noted that if time difference is calculated to be above the dead band value but is below the max time difference for 4 times consequently, no differential protection blocking occurs. The fifth calculation in the same range will block differential protection. This is in addition to blocking differential protection if the calculated time difference exceeds the set max time difference.

As noted, if GPS mode is not used at all, the relays can't measure the reference two-way delay and delay asymmetry. These values need to be pre-measured and set for operation in Echo mode. With varying communication system performance this does not appear as a viable option for BPA.

Another relevant setting is the adjustment rate prior to transitioning back to GPS mode: a slow adjustment rate was set which corresponds to the  $50\mu\text{s/s}$  adjustments, refer to Figure 28. Review of this setting confirmed this to be a good and recommended choice. Fast adjustment at  $1\text{ms/s}$  is another option that is not recommended for Echo modes. It is understandable, as  $1\text{ms/s}$  adjustment will in a second exceed the maximum allowed time difference between terminal clocks, which is set to  $600\mu\text{s}$ .

| Group / Parameter Name | IED Value [SG1/Common] | PC Value [SG1/Common] | Unit | Min | Max |
|------------------------|------------------------|-----------------------|------|-----|-----|
| Time                   |                        |                       |      |     |     |
| Synchronisation        |                        |                       |      |     |     |
| TIMESYNCHGEN: 1        |                        |                       |      |     |     |
| General                |                        |                       |      |     |     |
| CoarseSyncSrc          |                        | Disabled              |      |     |     |
| FineSyncSource         |                        | IRIG-B                |      |     |     |
| SyncMaster             |                        | Disabled              |      |     |     |
| TimeAdjustRate         |                        | Slow                  |      |     |     |
| IEC61850-9-2           |                        |                       |      |     |     |

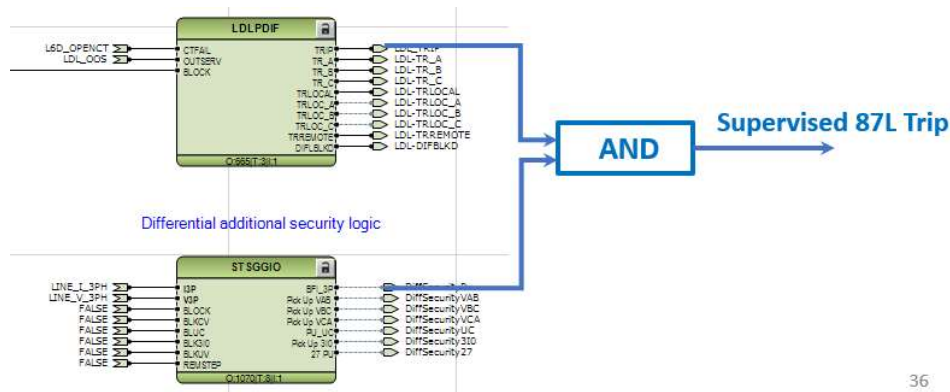
Description: Adjust rate for time synchronization

**Figure 28.** Relay time synchronization settings

Thus, review of relay settings confirmed their validity and that no settings changes would have prevented 2/5/2021 events.

#### 4.4 Additional relay logic

Additional relay logic was also considered to improve relay's defense against clock related issues. An overall time sync status is available as an internal relay signal, and as a part of relay-to-relay communication status. Both signals could be considered for implementing additional block logic for 87L function.



**Figure 29.** 87L function supervision

Another thought is supervising 87L element by a function that is based on completely different principles. A relay function with additional security logic, operating on phase-to-phase current variation is being considered, refer to Figure 29. Theoretical evaluations of this method led to an expectation that such supervision could have prevented Event 1. This will be verified by testing.

#### 4.5 Additional IRIG-B validity checks

IRIG-B frame structure is shown on Figure 30, for reader's reference. These frames are sent every second, using DC shift. Amplitude modulation (AM) or Modified Manchester coding.

*<sync> SS:MM:HH:DDD <control> <straight binary seconds>*

*<sync> is the on-time sync marker*

*SS is the second of the minute [00 to 59 (60 during leap seconds)]*

*MM is the minute of the hour (00 to 59)*

*HH is the hour of day in 24 h format (00 to 23)*

*DDD is the day of year (001 to 366)*

*<control> is a block of 27 binary control characters*

*<straight binary seconds> is a 17-bit second of day in binary*

**Figure 30.**IRIG-B frame structure

Enhanced IRIG-B validity checking is another avenue to explore as potential remedies. Currently, most IRIG-B devices support 4-bit Time Quality (TQ) check per older specification, defined in Synchrophasor standard dated 2005 [6]. TQ field per those definitions is set to 0 when clock is locked to GPS. This also means that no time accuracy information is provided in this case other than that clock is locked. TQ is transmitted in IRIG-B control positions P 71 to P 74.

Newer Synchrophasor standard dated 2011 [7] added definition of 3-bit Continuous Time Quality (CTQ) to communicate time accuracy when clock is locked to GPS and when it lost its GPS connection. This field helps to determine time accuracy in the locked state but does not help with detecting a constant and precise time offset. For example, it did not detect 4ms time offset as shown on Figure 9. So, while it is useful for devices to support and check CTQ field, it will not help with time offset challenge, however. CTQ is transmitted in IRIG-B control positions P 76 to P 78.

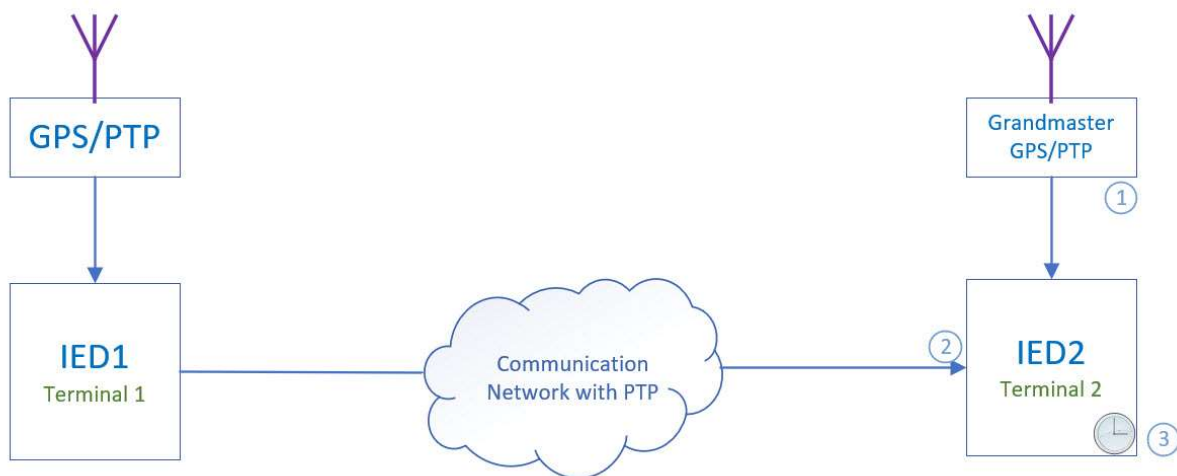
The 2/5/21 events showed that IRIG-B signal from the clock had a framing error. Specifically, 17-bit straight binary seconds (SBS) value did not align with 2-byte second value in SS field. One could consider SBS vs SS check to detect such framing error.

It should be noted that the latest IRIG-B specification is captured in the normative Annex A of IEEE C37.237 standard [8]. It includes the use of 17-bit SBS field for supplementary time information in a time division multiplexed (TDM) manner. For example, frames 11 and 12 are used for communication latest leap second information per International Earth Rotation and Reference Systems Service (IERS). SBS data is transmitted in IRIG-B positions P80 to P96. This new purpose of SBS field prevents implementation of SBS vs SS check for devices compliant to IEEE C37.237-2018 standard.

#### 4.6 Redundancy and time synchronization architectures

Another direction of improvements deals with architecture of time distribution itself. Firstly, the use of Echo mode only, without (GPS mode) was discussed and considered. Possibilities of using this approach depend on changing network characteristics. Secondly, installation of redundant clocks was discussed and is being pursued. Redundant clocks could include remote clocks with Ethernet-based Precision Time Protocol (PTP). It should be noted that if redundant clocks are used in a majority

scheme, a minimum of three clocks would be required. Refer to Figure 31 for an example of 3 possible time sources, GPS, PTP and internal oscillator.



**Figure 31.** Time synchronization architecture with redundant clocks

It should also be noted that while typically Global Navigation Satellite Systems (GNSS) such as GPS require minimum of 4 satellites to determine location and time, if location is known, only one satellite can be used to obtain time. In this case time source redundancy would not be achieved, refer to [1].

Lastly, discussions on implementing an atomic clock inside IEDs/relays was considered. While this is not in line with commonly accepted time distribution architectures, it could provide a reliable clock backup if other sources fail, including station clock and remote clock.

## 5. Conclusions

The 5/2/2021 Events that took place in BPA system provided numerous learning opportunities. The root cause for both events was conclusively identified as a clock misbehavior and appropriate corrective actions were put in place. What presented an interesting challenge is that misbehaving clock was sending good time quality indications with incorrect time. This triggered discussions on how could relays and overall protection systems defend against such clock misbehavior. A few methods discussed in this paper will be further evaluated and tested. Temporary desensitizing differential protection by increasing Idmin setting has been implemented in the meantime.

## References

- [1] A. Martin, R. Cooke, G. S. Antonova "Effect of communication channel and time synchronization quality on protection", Western Protective Relaying Conference 2016.
- [2] M. Kockott, S. Zubic, Z. Liu, H. Jernberg, T. Roseburg, W. Rees "A POTT scheme, using transient directional elements, for a complex 525kV transmission corridor comprising long, heavily loaded and heavily series compensated parallel lines", Western Protective Relaying Conference 2019.
- [3] IEEE Std. C37.94-2017 IEEE Standard for N times 64 kbps Optical Fiber Interfaces between Teleprotection and Multiplexer Equipment.
- [4] G. S. Antonova, M. A. Weiss and D. P. Erwin "Protection and Control dependencies on Time", Western Protective Relaying Conference 2018.

- [5] T. Roseburg, W. Rees, G.S. Antonova “Benefits of using IEC 61850 messages for testing conventional protection schemes”, Western Protective Relaying Conference 2020.
- [6] IEEE Std. C37.118-2005 IEEE Standard for Synchrophasors for Power Systems.
- [7] IEEE Std. C37.118.1-2011 IEEE Standard for Synchrophasor Measurements for Power Systems.
- [8] IEEE Std. C37.237 IEEE Standard for Requirements for Time Tags Created by Intelligent Electronic Devices—COMTAG.
- [9] Line differential protection RED670 Technical reference manual