Maximizing Line Protection Reliability, Speed, and Security

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***Abstract*—This paper describes several commonly applied line protection schemes, including distance schemes, directional comparison schemes using distance and directional elements, and line current differential schemes. Using analysis tools like fault trees, power system studies, and event analysis, we evaluate and compare these protection schemes in terms of speed, sensitivity, dependability, security, and selectivity. The paper considers the use of various communications channels, including direct relay-to-relay fiber-optic channels and multiplexed digital fiber-optic networks. The paper also discusses some practical considerations for evaluating line protection schemes when faced with complications like series compensation, mutual coupling, single-pole tripping and reclosing, three-terminal lines, and short lines.**

I. Introduction

Traditional protection systems consisted of a number of single-function electromechanical relays that provided good service for many years. However, providing redundancy required duplicating many devices. In addition, increased maintenance costs, lack of support by manufacturers, and incorrect operation data led many utilities to replace electromechanical relays with microprocessor-based relays, which provide better protection and control functions at lower cost and with higher reliability. They also have monitoring and communications abilities. Redundant protection systems are more economical with multifunction microprocessor-based relays. On the other hand, microprocessor-based relays have shifted complexity from panel designs and wiring to settings, logic, and documentation.

Modern power systems demand that transmission line protection schemes be reliable (dependable and secure), fast, sensitive, and selective. However, these protection system characteristics are frequently at odds with each other. For example, in a dual-redundant system, we need to connect the relay output contacts in parallel to achieve dependability but connect them in series to achieve security. A very fast and highly sensitive protection system may not be very secure or selective. For this reason, engineers have traditionally needed to make design choices to prioritize some protection system characteristics at the expense of others. With today's technology, is it possible to simultaneously maximize all of these critical protection characteristics?

References [1] and [2] discuss the application of fault tree analysis to determine factors that influence overall protection system reliability and provide comprehensive data of reliability indices. In particular, [1] evaluates line protection redundancy and reliability. Analyzing protection system speed, sensitivity, and selectivity not covered in [1] and [2] requires a different set of tools, such as computer-based power system studies and event information analysis.

This paper briefly describes several commonly applied line protection schemes. Using analysis tools like fault trees, power system studies, and event analysis, we evaluate these schemes in terms of speed, sensitivity, dependability, security, and selectivity and provide a comparison of the schemes' performance. The paper mainly considers the use of fiber-optic communications channels, but it also provides data on the speed of other channels, such as power line carrier (PLC) and digital radios. The paper also discusses some practical considerations for evaluating line protection schemes in complex applications.

II. Basic Concepts

A. Protection System Functional Characteristics

Protection system functional characteristics must meet the stringent requirements of modern power systems, which lack redundancy and operate near their security limits. The most important characteristics are reliability, selectivity, speed of operation, and sensitivity.

- Reliability is a measure of the certainty that the protection system will trip when required (dependability) and not trip when not required (security). We can obtain dependability through relays that try to trip the same circuit breaker (parallel connection of the relay contacts or its equivalent logic function [OR logic]). We can obtain security through series connection of the relay contacts or the equivalent logic function (AND logic). There is a bias among protection engineers toward dependability in protection system design. This bias reflects the fact that power systems are redundant to a certain extent. In modern power systems, however, this concept is changing. For example, some wide-area protection systems, where security is very important, use two-out-of-three voting schemes.
- Selectivity is the ability of a protection system to eliminate a fault in the shortest time possible with the least disconnection of system components. We also use the term coordination for selectivity. Protection coordination implies that primary protection eliminates faults and that backup protection operates only when primary protection fails.

- Speed of operation is the ability of the protection system to operate in a short time after fault inception. Fast operation is important in preserving system stability, reducing equipment damage, and improving power quality. Protection system operation time includes relay operating time, communications system delay (if any), and circuit breaker fault-clearing time.
- Sensitivity is the ability of the protection system to detect even the smallest faults within the protected zone. It is important to ensure the detection of high-impedance faults or the reduced contribution to faults from small, distributed generators.

B. Basic Reliability Concepts

We often use the following measures to describe product reliability performance, assuming constant failure and repair rates [1] [2] [3]:

- Failure: Termination of the ability of an item to perform its required or specified function.
- Failure rate (λ): Total number of failures divided by the total unit operating time or uptime.
- Repair rate (μ): Total number of repairs divided by the total unit operating time or uptime.
- Mean time to failure (MTTF): Average time between the start of operation (or return after repair) and failure. For a constant failure rate, MTTF = λ^{-1}.
- Mean time to repair (MTTR): Average time to correct a failure and restore a unit to operating condition. For a constant repair rate, MTTR = μ^{-1}.
- Mean time between failures (MTBF): Average time between failures for units repaired and returned to use.

MTBF is the sum of MTTF and MTTR. Because MTTR is usually small compared to MTTF, we assume that MTBF is approximately equal to MTTF and that MTBF = λ^{-1}.

Availability, a measure that considers repeated cycles of failure and repair, is the probability or fraction of time that a device or system is able to operate. Equation (1) defines availability *A* for constant failure and repair rates.

$$A = \frac{\mu}{\lambda + \mu} = \frac{MTTF}{MTTF + MTTR} \approx \frac{MTBF}{MTBF + MTTR} \quad (1)$$

Unavailability is the probability or fraction of time a device or system is unable to perform its intended function. Equation (2) defines unavailability *U* for constant failure and repair rates.

$$U = 1 - A = \frac{\lambda}{\lambda + \mu} = \frac{MTTR}{MTBF} \approx \lambda MTTR \quad (2)$$

Availability and unavailability are dimensionless numbers from 0 to 1. We can convert them to minutes or seconds per year by multiplying by the appropriate factors.

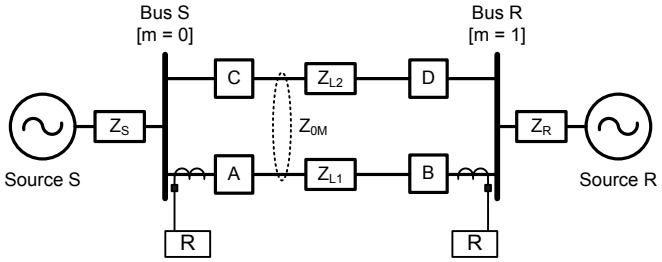
Fault tree analysis is a tool for evaluating how a component failure contributes to a specific failure event [3] [4]. Fault tree analysis is useful for comparing the relative reliability of protection schemes. The failure event of interest is called the top event. The failure rate for the top event is a combination of the failure rates of the basic events that contribute to the top event. Basic events are individual component failures with identified failure rates. We use AND, OR, and other gates to represent combinations of failure rates. OR gates express the idea that any of several failures can cause the protection system to fail. The OR gate output is the sum of the failure rates of the input events. AND gates express the idea that failures must occur simultaneously to cause the protection system to fail. The AND gate output is the product of the failure rates of the input events. We can also use availability, unavailability, or MTBF figures instead of failure rates in fault tree analysis.

Analyzing the dependability and security of a protection system requires different fault trees [1] [2]. To construct each tree, we identify which component failures may cause a failure to trip (a dependability problem) or an undesired trip (a security problem). This analysis leads to different tree topologies and different failure rate (or unavailability) values. For example, nearly any relay failure could cause a failure to trip. However, not all relay failures cause an undesired trip. Hence, the relay failure rate or unavailability value to use for dependability analysis is higher than the value to use for security analysis. In this paper, we use unavailability for dependability fault trees because failures to clear faults depend on component downtime per failure. We use failure rate for security fault trees because undesired trips typically occur at the instant a component fails [5].

III. Example Systems

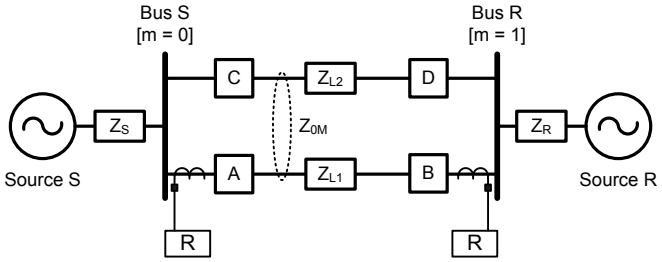
A. Example Power Systems

We performed computer-based steady-state power system studies to evaluate the sensitivity, speed, and selectivity of various line protection schemes. We selected three two-source example systems with two parallel transmission lines with magnetic mutual coupling. Fig. 1(a) shows a system with two strong sources and two long lines. Fig. 1(b) depicts a system with two strong sources and two short lines. Fig. 1(c) shows a system with a strong source, a weak source, and two long lines.



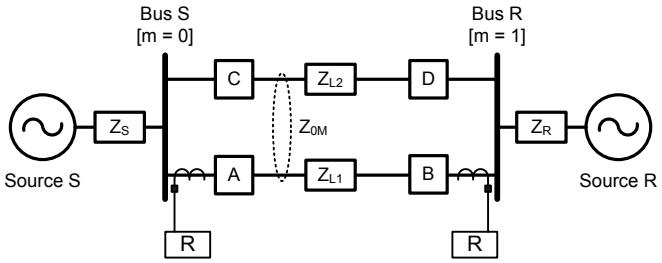
$Z_{1S} = 2\angle 88° \Omega$ $Z_{1L1} = Z_{1L2} = 8\angle 84° \Omega$ $Z_{1R} = 2\angle 88° \Omega$
$Z_{0S} = 2\angle 88° \Omega$ $Z_{0L1} = Z_{0L2} = 24\angle 80° \Omega$ $Z_{0R} = 2\angle 88° \Omega$
$Z_{0M} = 16\angle 78° \Omega$

(a)



$Z_{1S} = 2\angle 88° \Omega$ $Z_{1L1} = Z_{1L2} = 0.4\angle 84° \Omega$ $Z_{1R} = 2\angle 88° \Omega$
$Z_{0S} = 2\angle 88° \Omega$ $Z_{0L1} = Z_{0L2} = 1.2\angle 80° \Omega$ $Z_{0R} = 2\angle 88° \Omega$
$Z_{0M} = 0.8\angle 78° \Omega$

(b)



$Z_{1S} = 2\angle 88° \Omega$ $Z_{1L1} = Z_{1L2} = 8\angle 84° \Omega$ $Z_{1R} = 40\angle 60° \Omega$
$Z_{0S} = 2\angle 88° \Omega$ $Z_{0L1} = Z_{0L2} = 24\angle 80° \Omega$ $Z_{0R} = 40\angle 60° \Omega$
$Z_{0M} = 16\angle 78° \Omega$

(c)

Fig. 1. Example power systems: (a) two long lines and strong sources; (b) two short lines and strong sources; and (c) a strong source at S, a weak source at R, and two long lines.

B. Example Protection Systems

Reference [1] describes a reliability study of several directional comparison line protection schemes using fault trees. This study covered permissive overreaching transfer trip (POTT) and directional comparison blocking (DCB) schemes with PLC, microwave, and fiber-optic communications channels. The study evaluated the effect of protection system redundancy; comprehensive commissioning testing; using relays from the same or different manufacturers; and common-mode failures in relays. Table V of the Appendix summarizes the results.

In this paper, we extend the study in [1] to include line current differential (87L) schemes. We compare the reliability of POTT and 87L schemes protecting a transmission line with single circuit breakers at both ends. All schemes use multifunction relays and fiber-optic communications channels. Fig. 2(a) shows the basic line protection scheme, which consists of a communications-based protection scheme (Relay R1) complemented with a separate distance protection scheme (Relay R2) at each line end. The scheme includes one set of instrument transformers, one dc power system, and a circuit breaker with a single trip coil at each line end. In this scheme, the Zone 1 elements of the distance protection scheme provide redundant protection, independent from the communications channel. The scheme lacks high-speed tripping redundancy for faults that fall outside the reach of Zone 1 elements.

Fig. 2(b) shows a dual-redundant protection scheme, which includes two communications-based schemes with separate fiber-optic communications channels, two relays, two sets of instrument transformers, two dc power systems, and a circuit breaker with redundant trip coils at each line end. To create a triple-redundant scheme, we add a third communications-based scheme to the Fig. 2(b) scheme. In redundant schemes, we assume that all of the redundant components are of similar quality and that relays have the same reliability indices.

Fig. 2 represents the communications channel as a digital multiplexed fiber-optic network. We can replace the multiplexers and the network with an optical fiber providing direct relay-to-relay communication.

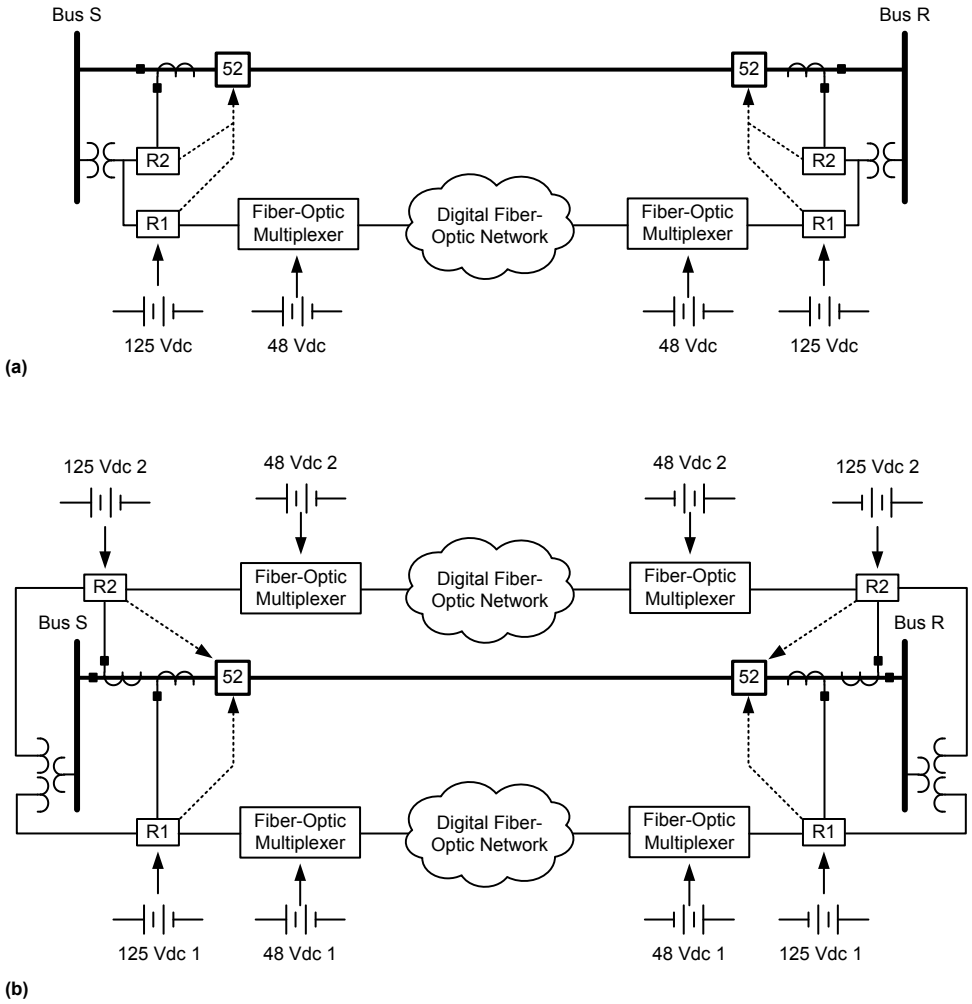


Fig. 2. Single- and dual-redundant transmission line protection schemes. An optical fiber providing direct relay-to-relay communication can replace the multiplexer and digital fiber-optic network.

IV. Protection Scheme Speed Analysis

Power system stability continues to drive the quest for faster protection. Faults must be cleared faster than critical clearing times or systems may lose transient stability. Faster protection also allows increased power transfer capability, reduces equipment damage, and improves power quality.

The fault-clearing time has the following components:

- Protection scheme tripping time (PSTT): The time elapsed between fault inception and the instant when the protection scheme issues a circuit breaker tripping signal.
- Circuit breaker fault-clearing time.

PSTT consists of the sum of the delays of all devices that must operate in order for the protection scheme to produce a circuit breaker tripping signal. PSTT includes:

- Relay operating time: Includes the protective relay and auxiliary relay (if used) delays.
- Communications system delay (for communications-based protection schemes).

A. Protective Relay Operating Time

Today's line protection schemes typically use microprocessor-based relay elements with phasor-based protection algorithms: directional overcurrent, distance, and current differential. For example, Fig. 3 shows the functional block diagram of a typical microprocessor-based mho relay element. The analog low-pass filters reject the high-frequency signal components to avoid aliasing errors in the sampling process. The digital band-pass filters extract the fundamental frequency components of the sampled and digitized voltage and current signals. In Fig. 3, V_{RE}, V_{IM}, I_{RE}, and I_{IM} designate the real and imaginary components of the voltage and current phasors, respectively. The relay performs a phase comparison between an operating signal derived from the voltage and current phasors and a polarizing signal (typically the memorized positive-sequence voltage) to create the mho characteristic shown in Fig. 3. Directional overcurrent and current differential elements also process phasors obtained as in Fig. 3.

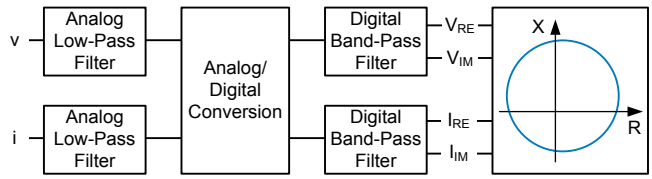


Fig. 3. Functional block diagram of a phasor-based mho element.

Fig. 4 shows the different components of the operating time of a microprocessor-based relay with phasor-based protection algorithms. Analog low-pass filter delay and sampling latency determine how fast the signal samples are available for processing by the digital filter. The analog filter delay depends on the filter type and its cutoff frequency, which depends on the sampling rate. For a 16 samples per cycle rate, the analog filter delay is around 0.04 cycles. After the delay introduced by the analog filter, the digital band-pass filter still needs to wait for the next sample to be available for processing. This is the sampling latency, whose value is between zero (when the fault occurs just before the next sampling instant) and the sampling period (for faults occurring just after the last sampling instant). For a 16 samples per cycle rate, the sampling period is 0.063 cycles. The digital band-pass filter typically introduces the longest delay. Reducing this delay is instrumental to achieving high-speed relay operation. The digital filter delay is determined by the data window length and the input signal magnitude as compared to the pickup setting. The digital filter delay approaches the data window length for faults representing an operation condition close to the relay pickup setting. For higher fault currents, the digital filter delay is smaller than the data window length. Relay protection algorithms process the phasors estimated by the digital filter to make tripping decisions. This processing introduces a delay, as shown in Fig. 4. Finally, the relay output system requires time to process the tripping signal and close the output relay contact. This is the output device delay.

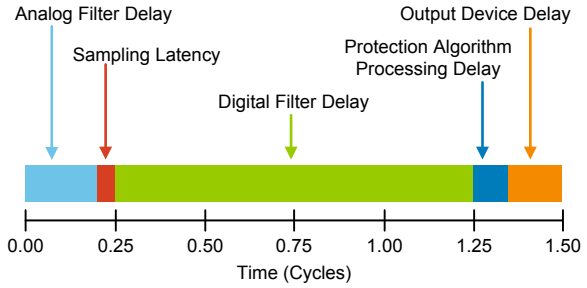


Fig. 4. Components of the operating time of a microprocessor-based relay with phasor-based protection algorithms.

As mentioned before, filtering delays relay operation. Most of this delay comes from the digital band-pass filter. The choice of the digital filter data window length (half cycle, one cycle, and so on) directly impacts relay operating speed and transient performance [6]. The longer the filter window, the longer the delay, but the lower the transient overreach. The shorter the window, the shorter the delay, but the greater the transient overreach. In order to maximize the performance, we can combine long- and short-window filters to achieve faster speeds for close-in faults and good transient performance for zone-boundary faults. Fig. 5 shows a dual-filter scheme that uses a full-cycle mho element in parallel with a high-speed, half-cycle element. In order to ensure high-speed element security, the relay reduces the reach of the high-speed element to compensate for the increased transient overreach [7] [8]. A better approach to improve speed is to apply time-domain protection principles. For example, the traveling wave principle allows reducing the relay operating time to a quarter of a cycle or less [9].

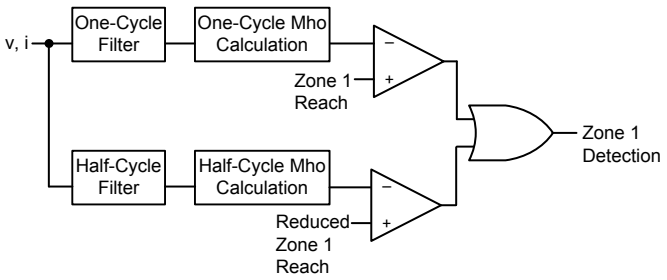


Fig. 5. Zone 1 mho distance element using dual-filter scheme.

The relay output system produces the contact closing operation that completes the circuit breaker tripping coil circuit. Conventional output systems with electromechanical relays typically add a 4 to 6 ms delay. We can use high-speed output systems with solid-state circuits that operate in about 10 µs to substitute conventional output systems.

Fig. 6 and Fig. 7 depict the typical operating times of two types of phase and ground mho elements, one that uses the Fig. 5 dual-filter scheme and another that uses only one-cycle filters. These elements have high-speed output systems; adding 4 to 6 ms to these times gives the typical operating times for mho elements with conventional output systems. Fig. 6 and Fig. 7 show the operating time as a function of fault distance (in percent of reach setting) for different values of source-impedance ratio (SIR). Fig. 6 and Fig. 7 show that the high-speed mho elements consistently trip in less than one cycle.

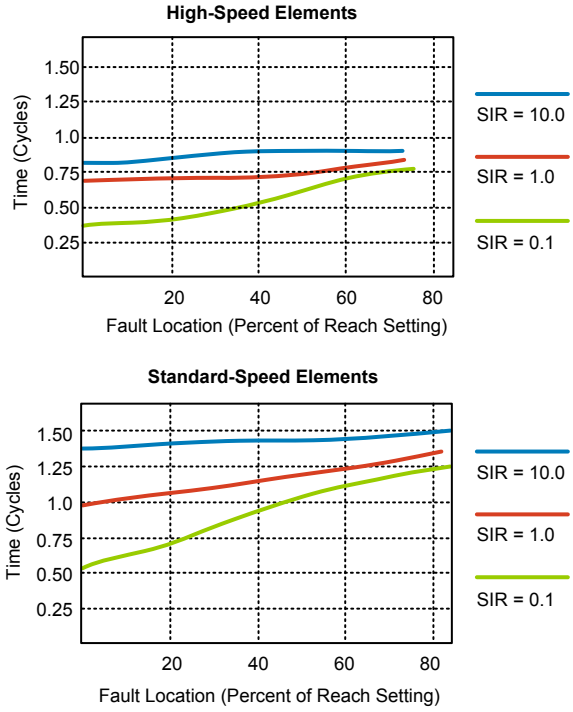


Fig. 6. Typical operating time of phase mho elements with high-speed, dual-filter schemes and with standard-speed, one-cycle filters.

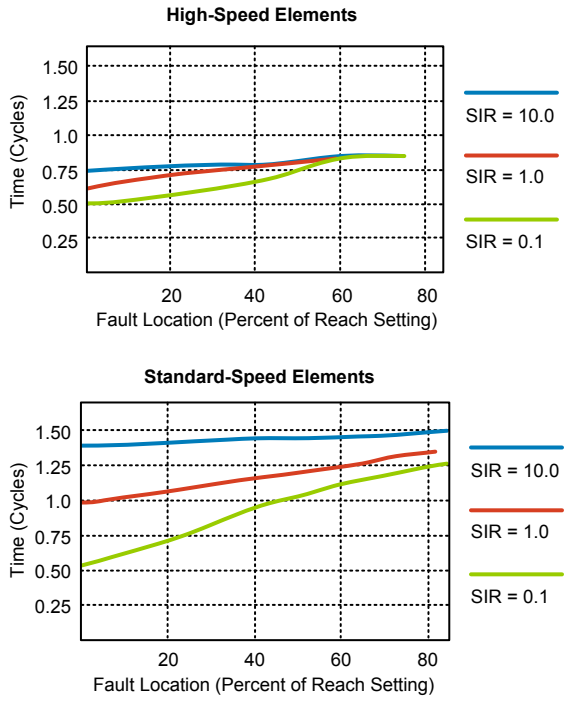


Fig. 7. Typical operating time of ground mho elements with high-speed, dual-filter schemes and with standard-speed, one-cycle filters.

Microprocessor-based 87L schemes perform the differential comparison of digitized current samples or current phasor values from all line terminals. Fig. 8 depicts the typical operating time of phase (87LP), negative-sequence (87LQ), and zero-sequence (87LG) differential elements. The 87LP elements trip in less than one cycle for differential currents above three times pickup current.

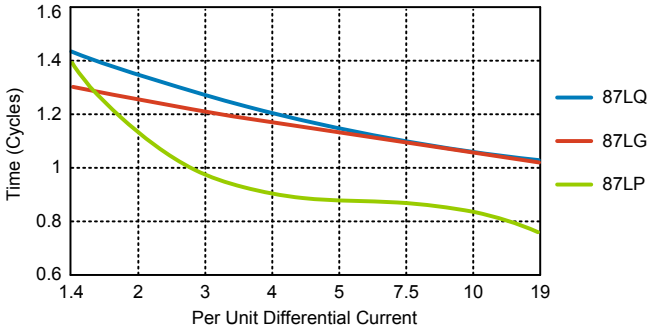


Fig. 8. Typical operating time of phase (87LP), negative-sequence (87LQ), and zero-sequence (87LG) differential elements.

The PSTT of the 87L scheme includes the differential element operating time and the communications system delay (the time it takes for the remote end current information to reach the local differential element). Section D covers communications system delay.

B. Pilot Protection Schemes

Pilot protection uses a communications channel to compare information from the line terminals and provide high-speed fault clearing for 100 percent of the protected line. Pilot protection includes directional comparison schemes and current-based schemes (phase comparison and 87L schemes).

In a directional comparison scheme, instantaneous directional overcurrent or distance elements provide fault direction information for the scheme logic at each line terminal. Directional comparison does not require a high-bandwidth channel because the relays exchange information on the status of their directional or distance elements. Typical bandwidth requirements are 0.5 to 1.5 kHz for analog channels and 9.6 kbps for digital channels. Directional comparison schemes include:

- Direct underreaching transfer trip (DUTT).
- Permissive underreaching transfer trip (PUTT).
- Permissive overreaching transfer trip (POTT).
- Directional comparison blocking (DCB).
- Directional comparison unblocking (DCUB).

Microprocessor-based 87L schemes perform the differential comparison of the protected line terminal currents. The relays can exchange digitized current samples or current phasor values. 87L protection requires a digital microwave or fiber-optic channel with a bandwidth of 56 kbps or higher. The communications system delay causes a fictitious phase shift between the local current and the received remote current(s). 87L schemes align (synchronize) current samples or phasors to prevent the errors caused by this phase shift. Typical communications system delay requirements for 87L schemes are in the range of 5 to 10 ms.

C. Components of PSTT in Pilot Protection Schemes

The pilot protection schemes of all line terminals must operate to achieve high-speed fault clearing. Hence, PSTT is the time it takes the slowest scheme to issue the circuit breaker tripping signal.

Fig. 9(a) shows the components of PSTT in a traditional directional comparison tripping scheme (PUTT, POTT, or DCUB) with analog relays and an analog PLC or microwave channel. PSTT includes the local relay operating time, local and remote communications equipment delays, communications channel delay, processing delay at the remote relay, and remote relay output device delay. Microprocessor-based relays start the signal transmission process when the output of a protection element asserts, as shown in Fig. 9(b). There is no need to wait for the relay output contact to close. Direct relay-to-relay communication over optical fiber practically eliminates the communications equipment delay (the fiber-optic transceiver is very fast), as shown in Fig. 9(c).

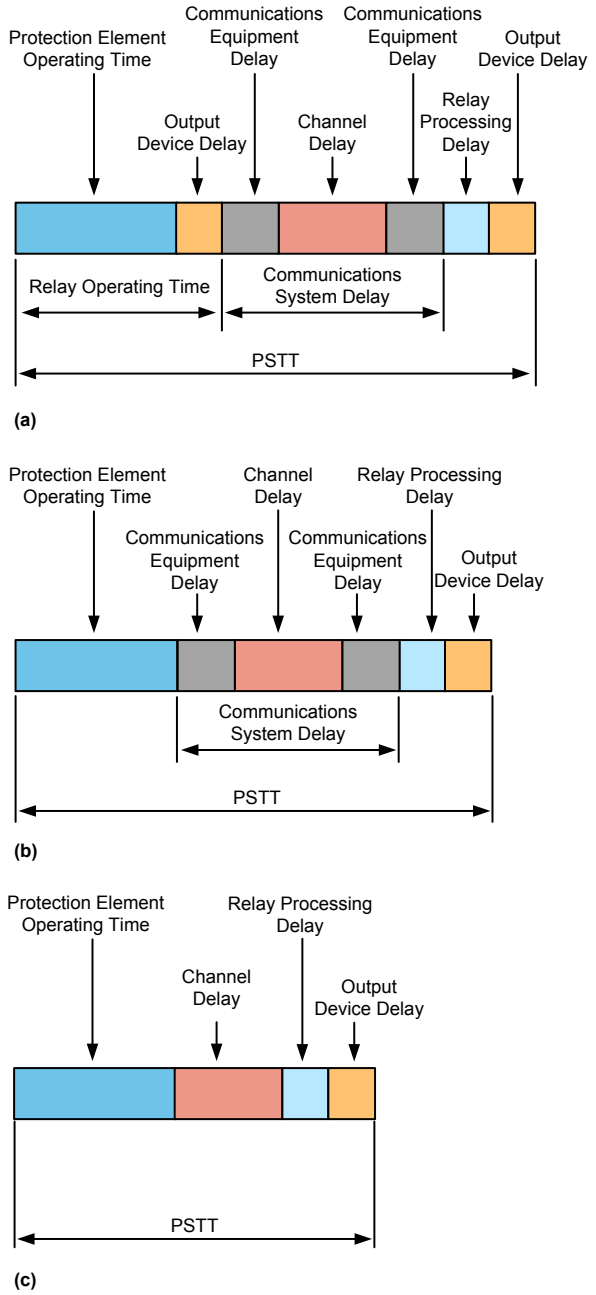


Fig. 9. Components of PSTT in line pilot protection schemes: (a) directional comparison tripping scheme (PUTT, POTT, or DCUB) with analog relays and analog PLC or microwave channel; (b) pilot protection scheme with microprocessor-based relays and digital microwave channel, digital radio channel, or digital fiber-optic network; and (c) pilot protection scheme with direct relay-to-relay communication over optical fiber.

The relay processing delay in Fig. 9 includes the hardware and firmware delays (approximately 3 ms), plus the processing latency. This latency equals zero when an input is processed just before a change of state, and it equals the processing period when the input is processed just after a change of state. The longest processing latency is 4 ms for a 4 sample/cycle processing rate and 2 ms for an 8 sample/cycle rate. A slow channel further increases relay processing latency. Modern communications equipment uses high-speed, solid-state outputs. However, some legacy systems require interposing relays that add 2 to 4 ms of delay and are also susceptible to contact bounce, for which an additional delay may be necessary to "debounce" inputs [10].

As an example, Table I, taken from [11], lists typical processing delays for relays using a proprietary relay-to-relay communications protocol for different processing rates and channel speeds.

TABLE I
TYPICAL PROCESSING DELAYS FOR RELAYS USING A RELAY-TO-RELAY COMMUNICATIONS PROTOCOL [11]

Channel Speed (kbps)	Relay Processing Delay (ms)	
	8 Samples per Cycle	4 Samples per Cycle
38.4	4.2	8.3
19.2	6.3	10.5
9.6	8.3	12.5
4.8	12.5	16.7

Fig. 10 shows the typical time chart for a POTT scheme with overreaching distance elements, excluding Zone 1 direct tripping. DCB schemes require an additional coordinating time delay to wait for the blocking signal to arrive from the remote terminal(s). For this reason, DCB schemes are slightly slower than PUTT, POTT, or DCUB schemes.

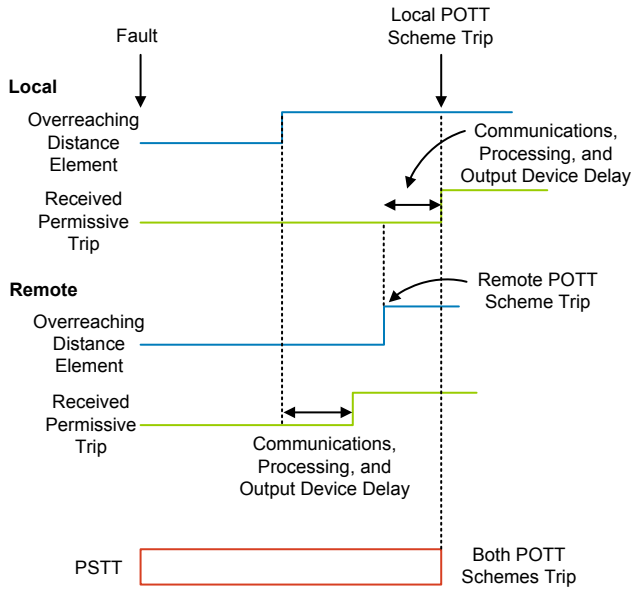


Fig. 10. Time chart for a POTT scheme with overreaching distance elements (excluding Zone 1 direct tripping).

D. Communications System Delay

Fig. 9(a) and Fig. 9(b) show that the communications system delay (also called communications system latency) includes the equipment and channel delays.

PLC systems, typically used for DCB schemes, transmit information over the line conductors. PLC frequencies are usually in the 30 to 500 kHz range. Table II shows typical delays for traditional on-off and frequency-shift PLC systems. Always check manufacturer published specifications when determining operating times for any given scheme. Wide-band PLC systems are faster than narrow-band systems, but the wider band channel allows more noise into the receiver filter, which introduces a greater chance for a false assertion.

TABLE II
TYPICAL DELAYS FOR TRADITIONAL PLC SYSTEMS

Communications Equipment	Delay (ms)
PLC (wide or narrow band)	4 to 8 [10]
PLC (on/off DCB)	2 to 4

Pilot protection schemes using digital communications technology have been in use for over 20 years. These schemes use direct or multiplexed optical fiber, digital radios, and digital microwave channels.

Considering a direct relay-to-relay connection over optical fiber, the communications delay depends on the time required for light to travel over the optical fiber (0.8 ms per 100 miles). In multiplexed fiber-optic networks, multiplexers and repeaters introduce additional delays. For protection multiplexers, the delay is only 0.5 ms plus approximately 24 µs for each repeater in the path. Some multiplexers designed for telecommunications applications over Ethernet do not perform to protection expectations. These multiplexers may introduce 6 to 8 ms delays. Table III shows typical delays for direct relay-to-relay communication over optical fiber and multiplexed fiber-optic networks.

TABLE III
TYPICAL DELAYS FOR DIRECT RELAY-TO-RELAY COMMUNICATION OVER OPTICAL FIBER AND MULTIPLEXED FIBER-OPTIC NETWORKS

Communications System Component	Delay
Optical fiber	0.8 ms per 100 miles
Protection-class multiplexer	0.5 ms
Nonprotection-class multiplexer	6 to 8 ms
Repeater	24 µs/repeater

For example, for direct relay-to-relay communication systems, the delay is nearly zero for a short line since the optical fiber delay is less than 0.8 ms. For multiplexed fiber-optic networks, the communications system delay depends on the line length and the fiber-optic network delay. Using protection multiplexers, the communications system delay is typically under 2 ms. For a 100-mile line, the delay would be about 1.3 ms, based on 0.8 ms (optical fiber delay), plus approximately 0.5 ms (multiplexer delay), plus approximately 24 µs per repeater [12].

In some applications, such as subtransmission line protection, where fault-clearing speed is not as critical, digital point-to-point serial radios are an acceptable and economical alternative. These radios typically operate in the unlicensed 900 MHz range and are limited to line of sight. Under favorable conditions, the radios can work on lines up to about 20 miles. Table IV shows typical communications delays for digital relay-to-relay communications systems using point-to-point radios. The use of AES-256 encryption introduces some additional delay.

TABLE IV
TYPICAL DELAYS FOR DIGITAL RELAY-TO-RELAY COMMUNICATIONS SYSTEMS USING POINT-TO-POINT RADIOS

Channel Speed (kbps)	Delay (ms)	
	No Encryption	With AES-256 Encryption
38.4	4.8	N/A
19.2	5.6	7.4

E. Evaluation of PSTT by Computer Simulations

In order to evaluate the operating speed of different protection schemes, we simulated faults at different locations on one line of each of the three example systems shown in Fig. 1. We determined the average PSTT values for POTT and 87L schemes. We considered the following pilot schemes:

- POTT scheme with distance Zone 1 direct tripping:
  - POTT scheme using Zone 1 and Zone 2 phase and ground high-speed distance elements (the Zone 1 element also provides direct circuit breaker tripping).
  - Zone 1 reach set to 80 percent of the line length for long lines and 60 percent for short lines.
  - Zone 2 reach set to 200 percent of the line length.
  - Communication at 38.4 kbps over fiber-optic network with multiplexers (for long lines).
  - Relay-to-relay communication at 38.4 kbps over direct optical fiber (for short lines).
  - Fast (<10 µs) output devices.
- 87L scheme with distance Zone 1 direct tripping:
  - 87L scheme using phase (87LP), negative-sequence (87LQ), and zero-sequence (87LG) elements. 87LP pickup current set to 1.2 per unit. 87LQ and 87LG pickup current set to 0.2 per unit.
  - Zone 1 reach set to 80 percent of the line length for long lines and 60 percent for short lines.
  - Communication at 56 kbps over fiber-optic network with multiplexers (for long lines).
  - Relay-to-relay communication at 56 kbps over direct optical fiber (for short lines).
  - Fast (<10 µs) output devices.

Fig. 11 through Fig. 16 show the average PSTT values resulting from computer simulations.

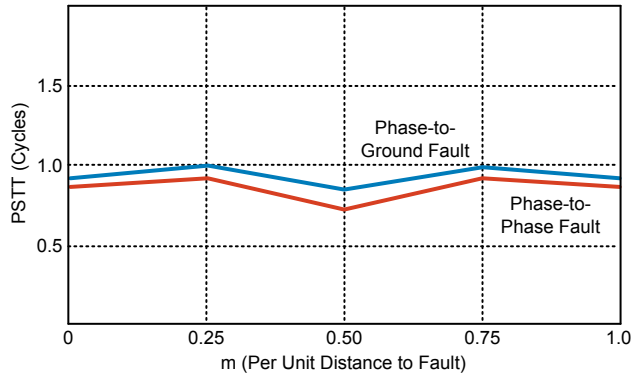


Fig. 11. Average PSTT values for POTT scheme and 80 percent distance Zone 1 direct tripping. System with two long lines and strong sources.

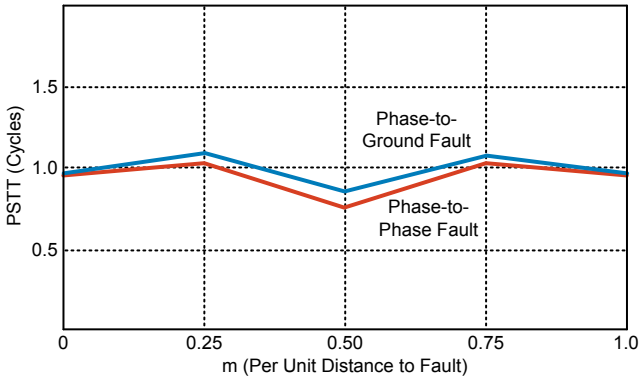


Fig. 12. Average PSTT values for 87L scheme and 80 percent distance Zone 1 direct tripping. System with two long lines and strong sources.

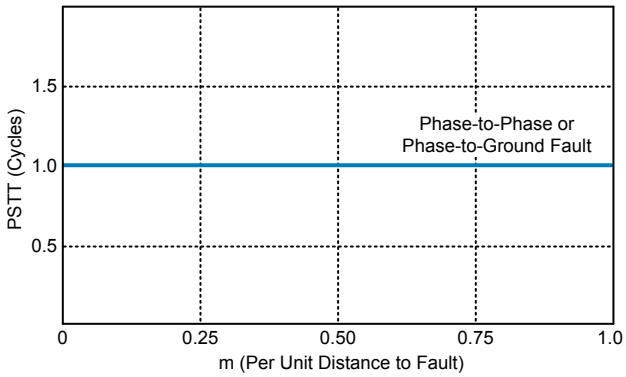


Fig. 13. Average PSTT values for POTT scheme and 60 percent distance Zone 1 direct tripping. System with two short lines and strong sources.

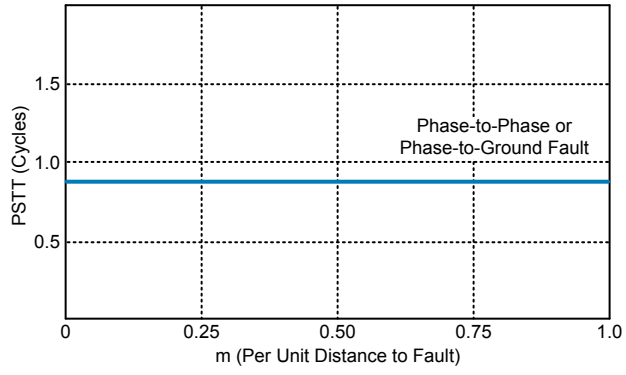


Fig. 14. Average PSTT values for 87L scheme and 60 percent distance Zone 1 direct tripping. System with two short lines and strong sources.

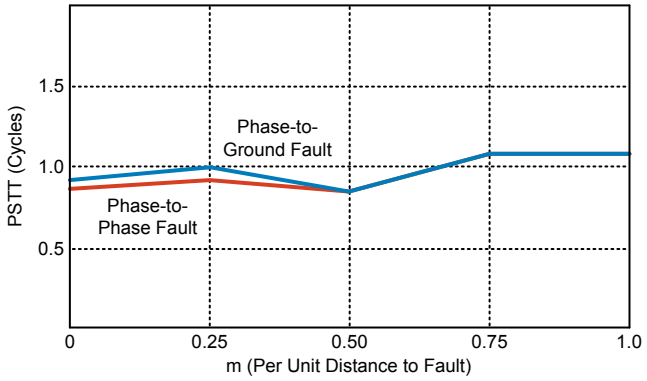


Fig. 15. Average PSTT values for POTT scheme and 80 percent distance Zone 1 direct tripping. System with two long lines, a strong source at the local end, and a weak source at the remote end.

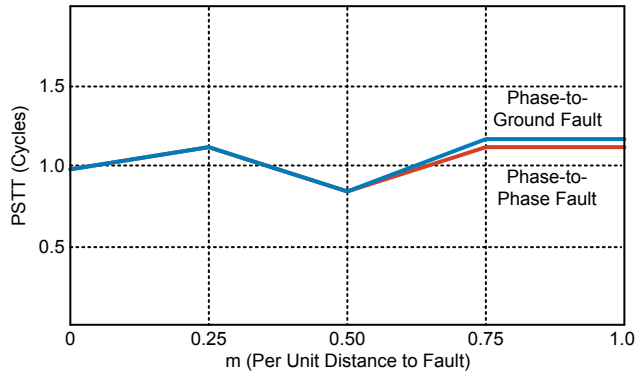


Fig. 16. Average PSTT values for 87L scheme and 80 percent distance Zone 1 direct tripping. System with two long lines, a strong source at the local end, and a weak source at the remote end.

Fig. 11 through Fig. 16 show that modern protection schemes using high-speed elements and fast communications channels produce low and consistent PSTT values for various line lengths and source strengths.

F. Actual Fault Case

Many power system events demonstrate the speed of modern directional comparison and 87L protection schemes. For example, [13] reports multiple relay operations that show PSTT values close to one cycle, including one event in which the 87L scheme detects two consecutive single-phase-to-ground faults in 0.75 cycles, as shown in Fig. 17.

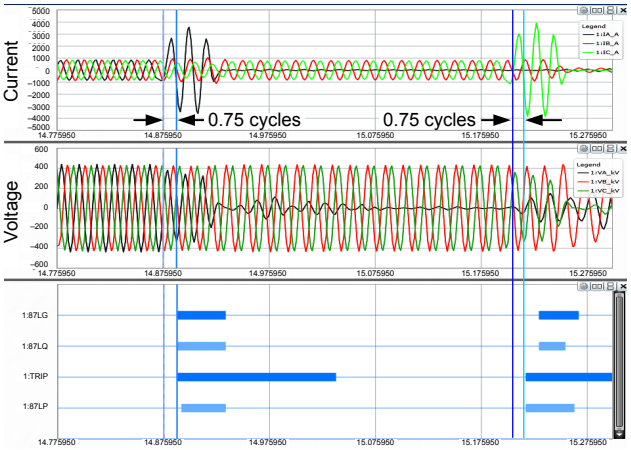


Fig. 17. 87L scheme detects two consecutive faults in 0.75 cycles.

V. Protection System Sensitivity Analysis

Measuring fault resistance (R_F) coverage is an excellent way to evaluate the sensitivity of a protection system. References [14], [15], and [16] evaluate the sensitivity of ground directional and distance elements and ground pilot protection schemes based on R_F coverage. In this paper, we expand this discussion by including an evaluation of 87L element sensitivity and comparing it to distance and directional element sensitivity.

A. Protection Element R_F Coverage

In order to evaluate sensitivity, we simulated single-phase-to-ground faults at different locations on one line of each of the three example systems shown in Fig. 1. We determined the maximum value of R_F detected by each protection element for each fault location. We used the following settings for the studied protection elements:

- Ground mho distance element (21N): Reach setting of $2Z_{1L}$.
- Ground quadrilateral distance element (21X):
  - Reactance reach setting of $2Z_{1L}$.
  - Resistance reach setting of 50 ohms secondary.
- Zero-sequence directional overcurrent element (67N): Pickup current setting of $3I_0 = 0.5$ A.
- Negative-sequence directional overcurrent element (67Q): Pickup current setting of $3I_2 = 0.5$ A.
- Zero-sequence differential element (87LG): Differential current pickup setting of $3I_0 = 0.5$ A.
- Negative-sequence differential element (87LQ): Differential current pickup setting of $3I_2 = 0.5$ A.

Fig. 18 through Fig. 20 depict the R_F coverage of 21N, 21X, 67N, 67Q, 87LG, and 87LQ elements as a function of fault distance. These figures show that the value of R_F detected by the ground distance and directional elements decreases as the fault moves away from the relay location because these elements measure only the local current, which diminishes as the fault moves away. However, 87LG and 87LQ elements measure the total fault current (the sum of the local and remote currents), which maximizes their R_F coverage and makes it independent of the fault location.

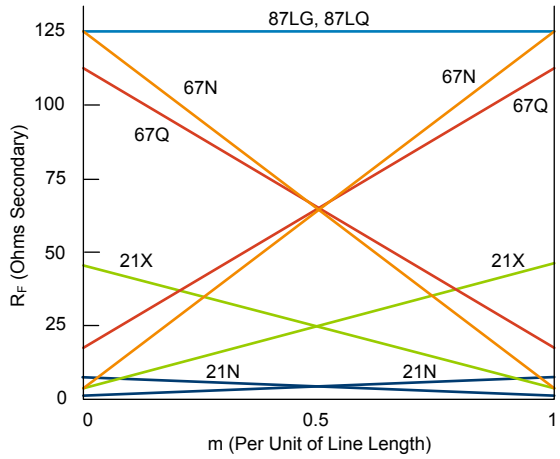


Fig. 18. R_F coverage of 21N, 21X, 67N, 67Q, 87LG, and 87LQ elements. System with two long lines and strong sources.

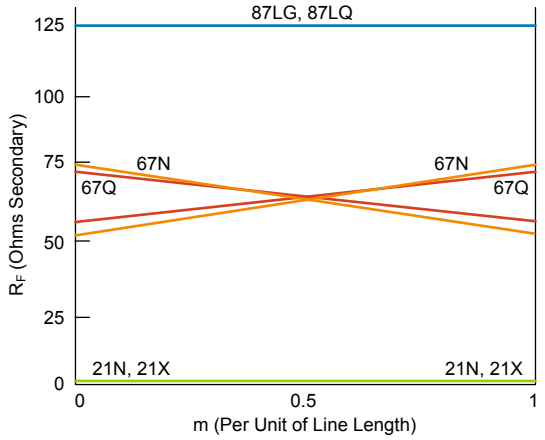


Fig. 19. R_F coverage of 21N, 21X, 67N, 67Q, 87LG, and 87LQ elements. System with two short lines and strong sources.

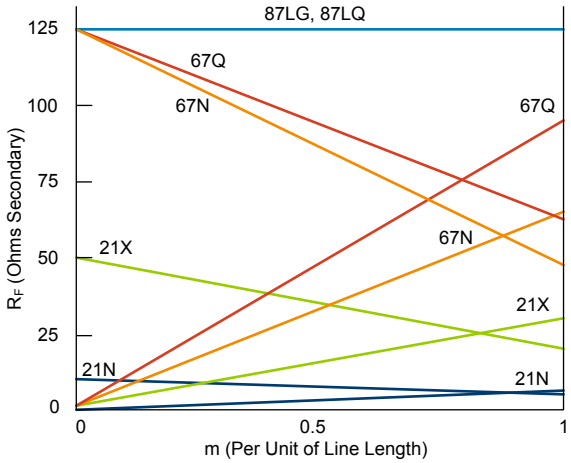


Fig. 20. R_F coverage of 21N, 21X, 67N, 67Q, 87LG, and 87LQ elements. System with two long lines, a strong source at the local end, and a weak source at the remote end.

B. Combining Speed and Sensitivity

Reference [16] compares various pilot protection schemes, including an evaluation of speed and sensitivity together. To add to this work, we also considered 87L schemes. For which faults can we maximize both speed and sensitivity?

Fig. 21 shows the R_F coverage regions of a POTT scheme using instantaneous overreaching 67N elements for the system with two long lines and strong sources shown in Fig. 1(a). Fig. 21 does not show the effect of the directly tripping underreaching instantaneous 67N elements or the time-delayed overreaching 67N elements. The POTT scheme trips in less than 1.5 cycles when the overreaching 67N elements of both line terminals detect the ground fault (Region A in Fig. 21). When only one overreaching 67N element detects the fault, the POTT scheme does not trip immediately because it does not receive the permissive tripping signal from the other terminal. If an instantaneous underreaching 67N element trips the circuit breaker, the fault current redistribution with that terminal open allows the overreaching 67N element of the other terminal to detect the fault and send the permissive signal. This sequential operation introduces some fault-clearing delay (Region B in Fig. 21). If no underreaching 67N element detects the fault, no current redistribution occurs, and the POTT scheme does not operate. Fault clearing occurs when the time-delayed overreaching 67N elements trip the circuit breakers. This time-delayed fault clearing defeats the POTT scheme purpose.

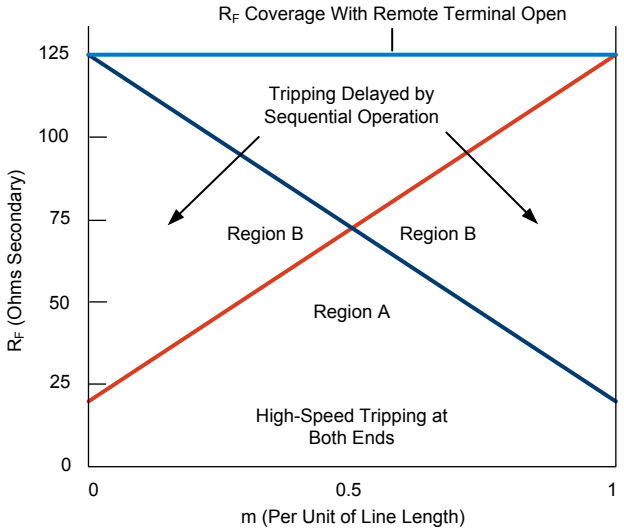


Fig. 21. R_F coverage regions of a POTT scheme using instantaneous overreaching 67N elements for the system with two long lines and strong sources.

Fig. 22 through Fig. 24 show the high-speed R_F coverage regions (corresponding to Region A in Fig. 21) for the different line protection schemes studied in this paper and for the different power systems of Fig. 1. These figures show the higher sensitivity and speed of 87L schemes using 87LG and 87LQ elements as compared with POTT schemes using either 67N or 21N (or 21X) elements. Fig. 22 through Fig. 24 also show that 67N elements provide higher sensitivity and speed than 21N (or 21X) elements.

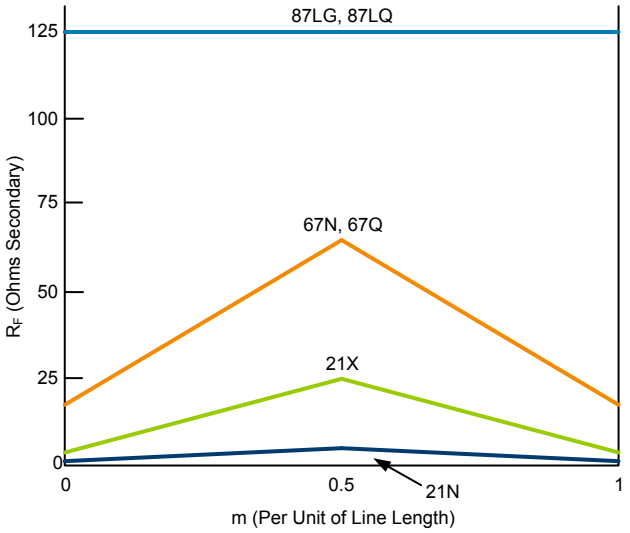


Fig. 22. High-speed R_F coverage regions of POTT schemes with 21N, 21X, 67N, or 67Q elements and of 87L schemes with 87LG or 87LQ elements. System with two long lines and strong sources.

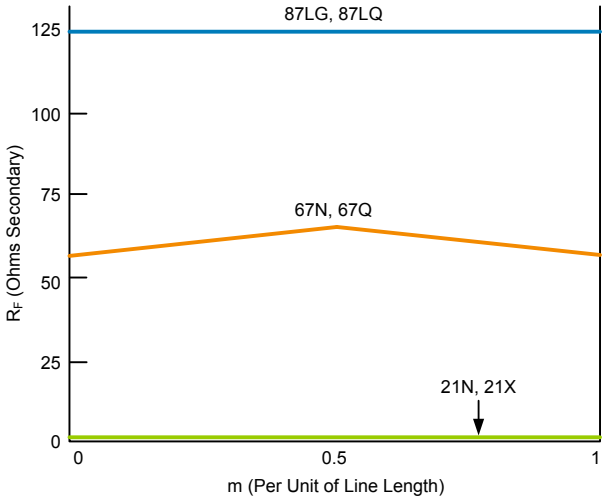


Fig. 23. High-speed R_F coverage regions of POTT schemes with 21N, 21X, 67N, or 67Q elements and of 87L schemes with 87LG or 87LQ elements. System with two short lines and strong sources.

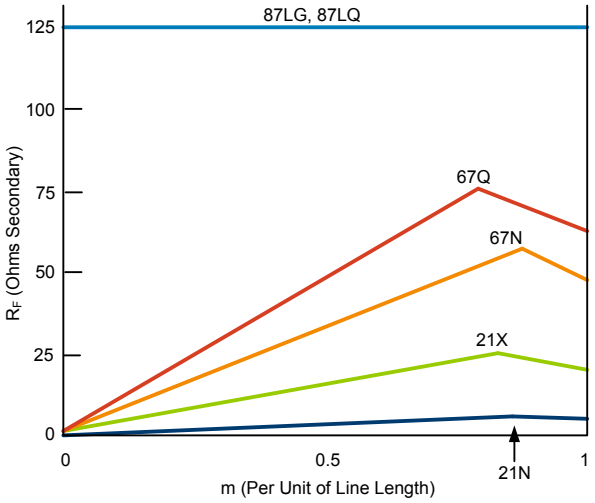


Fig. 24. High-speed R_F coverage regions of POTT schemes with 21N, 21X, 67N, or 67Q elements and of 87L schemes with 87LG or 87LQ elements. System with two long lines, a strong source at the local end, and a weak source at the remote end.

C. Actual Fault Case

One actual system fault on a 525 kV transmission line with 500 ohms primary (or 44 ohms secondary) of fault resistance was cleared by a pilot protection scheme using 67N elements [17]. Fig. 25 shows the phasors measured by the relay of one line terminal. If an 87L scheme had been applied on this line, the relays at both terminals would have measured approximately 190 A of negative-sequence and zero-sequence differential current. These primary current values yield $3I_0 = 3I_2 = 1.425$ A secondary, well above the minimum pickup current of modern 87LG and 87LQ elements.

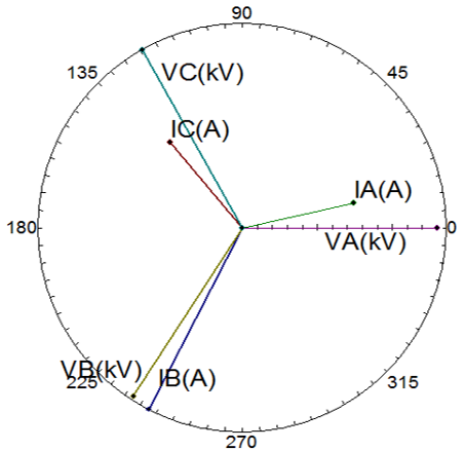


Fig. 25. Currents and voltages measured by the relay during a ground fault on a 525 kV line with $R_F = 500$ ohm primary.

VI. Protection System Reliability Analysis

When applying fault trees to analyze protection system reliability, the power system performance requirements determine the top event of the fault tree. If, for example, the power system requires high-speed fault clearing to preserve transient stability, the top event should only consider high-speed protection. However, if the power system remains stable after a breaker failure protection operation, the top event should also consider breaker failure protection.

We created 20 fault trees (10 for dependability analysis and 10 for security analysis) for the following protection schemes (all with fiber-optic channels):

- Combination of POTT scheme with direct Zone 1 tripping (POTT/21) in one relay and distance protection (21) scheme in another relay [Fig. 2(a)].
- Combination of 87L scheme with direct Zone 1 tripping (87L/21) in one relay and 21 scheme in another relay [Fig. 2(a)].
- Dual-redundant POTT/21 scheme [Fig. 2(b)]. Each relay performs POTT and 21 scheme functions.
- Dual-redundant POTT scheme [Fig. 2(b)]. Each relay performs POTT scheme functions (no direct Zone 1 tripping).
- Dual-redundant POTT/21 and 87L/21 scheme [Fig. 2(b)]. One relay performs POTT and 21 scheme functions and the other performs 87L and 21 scheme functions.
- Dual-redundant POTT and 87L scheme [Fig. 2(b)]. One relay performs POTT scheme functions and the other performs 87L scheme functions (no direct Zone 1 tripping).
- Dual-redundant 87L/21 scheme [Fig. 2(b)]. Each relay performs 87L and 21 scheme functions.
- Dual-redundant 87L scheme [Fig. 2(b)]. Each relay performs 87L scheme functions (no direct Zone 1 tripping).
- Triple-redundant two-out-of-three voting 87L/21 scheme. Each relay performs 87L and 21 scheme functions.
- Triple-redundant two-out-of-three voting 87L scheme. Each relay performs 87L scheme functions (no direct Zone 1 tripping).

Table VI of the Appendix shows the reliability indices used in the fault trees.

In this section, we describe several fault trees and summarize the results obtained from all of the fault trees.

A. Single Schemes

Fig. 26 shows the dependability fault tree for the combination of POTT/21 and 21 schemes in separate relays [Fig. 2(a)] with a fiber-optic channel. The top event is "protection fails to clear in-section fault in the prescribed time." In our analysis, the prescribed time is 6 cycles, which means that this fault tree considers only high-speed protection. We assume that the power system requires high-speed fault clearing to preserve transient stability. We should change the prescribed time to breaker failure time if the power system remains stable after a breaker failure protection operation.

The left side of the fault tree in Fig. 26 expresses the likelihood for the 21 scheme not to provide channel-independent, high-speed tripping for faults in Zone 1 coverage of both line ends [5]. We assume that both Zone 1 elements detect around 45 percent of all line faults to accommodate the effect of fault resistance. The right side of the fault tree represents POTT/21 scheme contribution to a failure to trip (for the remaining 55 percent of all faults). OR Gate 5 indicates that any failure to trip of the 21 scheme or of the POTT/21 scheme causes a protection scheme failure to trip. We can modify the fault tree as required to consider other scheme configurations, include other events of interest, or use other unavailability values.

In Fig. 26 and in all of the other dependability fault trees, we show the unavailability values multiplied by 10^6.

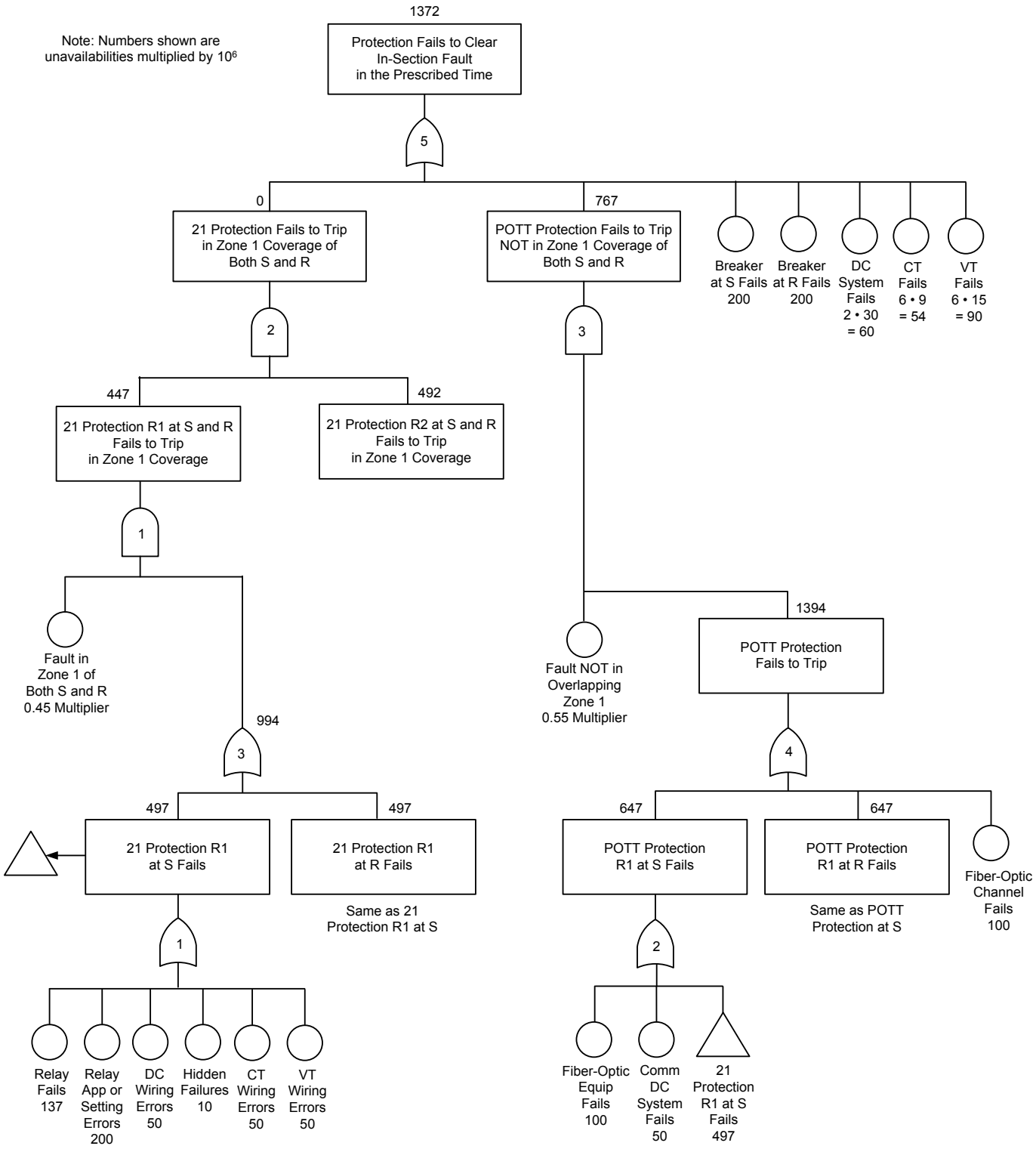


Fig. 26. Dependability fault tree for the combination of POTT/21 and 21 schemes in separate relays [Fig. 2(a)] with a fiber-optic channel.

Fig. 27 shows the security fault tree for the combination of POTT/21 and 21 schemes in separate relays [Fig. 2(a)] with a fiber-optic channel. The top event is "protection produces an undesired trip." This security fault tree includes the same basic events as the dependability fault tree (Fig. 26) but uses the security failure rates shown in Table VI of the Appendix. The left side of the fault tree expresses the likelihood for the 21 scheme to cause an undesired trip. The right side of the fault tree represents the POTT/21 scheme contribution to an undesired trip, which occurs when the directly tripping Zone 1 undesirably trips or the communications system generates an undesired permissive trip signal and also an overreaching POTT element operates for an external fault. We assume that 20 percent of external faults fall within the overreaching element zone.

In Fig. 27 and all of the other security fault trees, we show the failure rate values multiplied by 10^6.

Fig. 28 shows the dependability fault tree for the combination of 87L/21 and 21 schemes in separate relays [Fig. 2(a)] with a fiber-optic channel. The left side of the fault tree in Fig. 28 expresses the likelihood for the 21 scheme to cause a failure to trip. The right side of the fault tree represents the POTT/21 scheme contribution to a failure to trip. OR Gate 6 indicates that any failure to trip of the 21 scheme or of the POTT/21 scheme causes a protection scheme failure to trip.

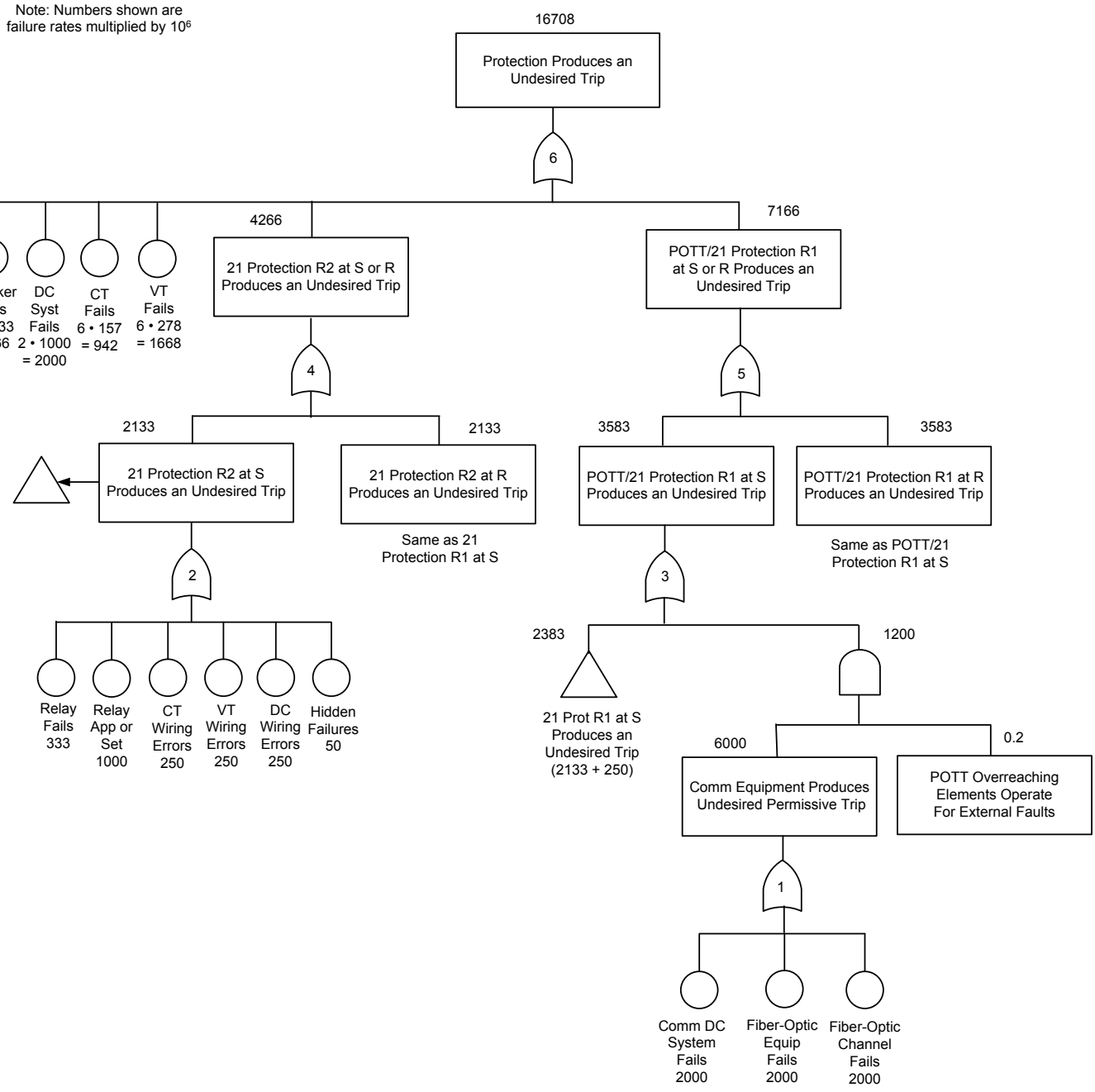


Fig. 27. Security fault tree for the combination of POTT/21 and 21 schemes in separate relays [Fig. 2(a)] with a fiber-optic channel.

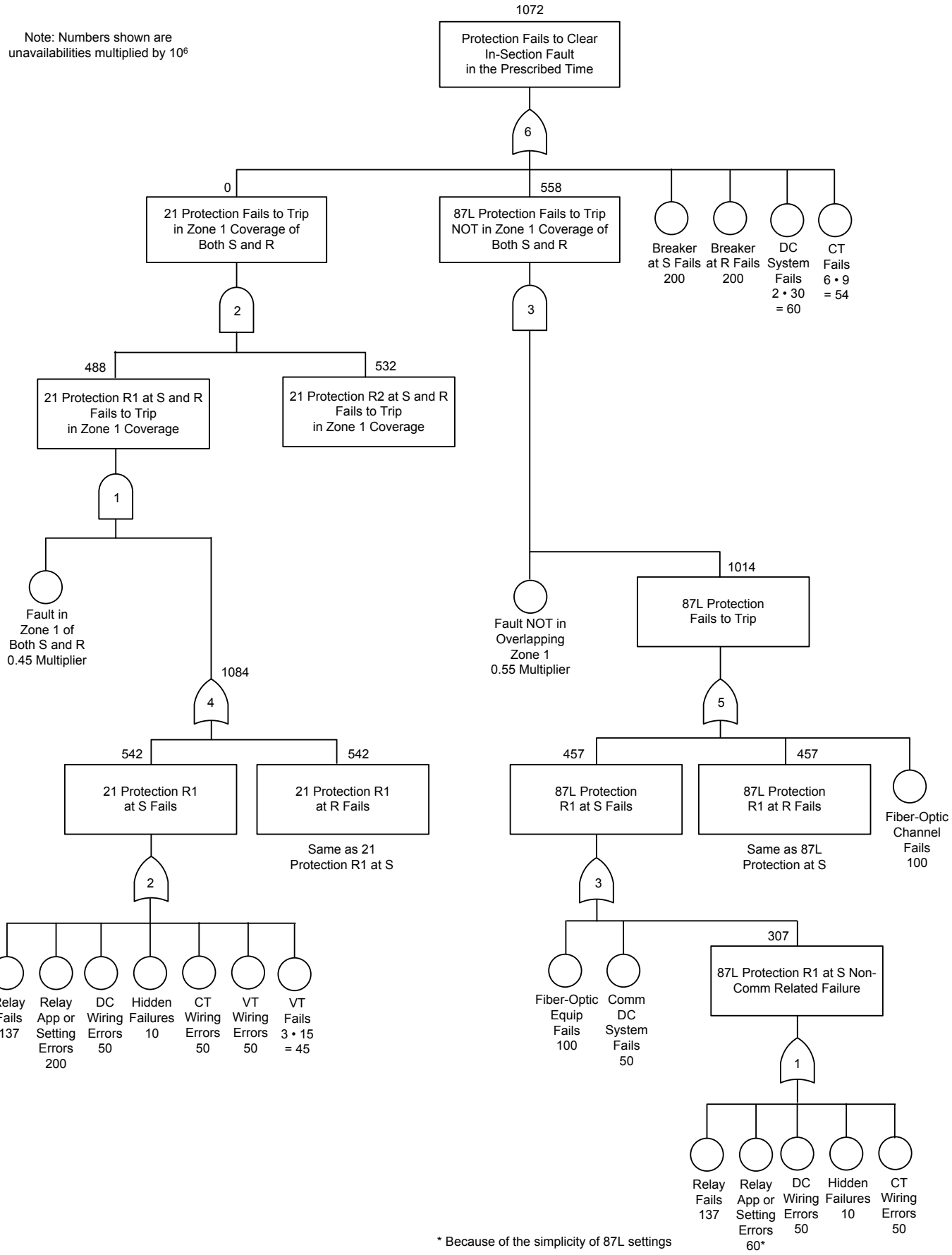


Fig. 28. Dependability fault tree for the combination of 87L/21 and 21 schemes in separate relays [Fig. 2(a)] with a fiber-optic channel.

Fig. 29 shows the security fault tree for the combination of 87L/21 and 21 schemes in separate relays [Fig. 2(a)] with a fiber-optic channel. The left side of the fault tree expresses the likelihood for the 21 scheme to cause an undesired trip. The right side of the fault tree represents the 87L/21 scheme contribution to an undesired trip, which occurs when the directly tripping Zone 1 undesirably trips or the communications system generates an undesired 87L trip.

B. Redundant Schemes

In the redundant schemes analyzed in this paper, either Main 1 or Main 2 protection schemes may consist of a POTT/21, POTT, 87L/21, or 87L scheme. We first created the fault trees for these schemes (each residing in one relay) and then used them as building blocks for the fault trees of the dual- and triple-redundant schemes. As an example, Fig. 30 shows the dependability fault tree for the POTT/21 scheme in one relay (Relay R1 in this example).

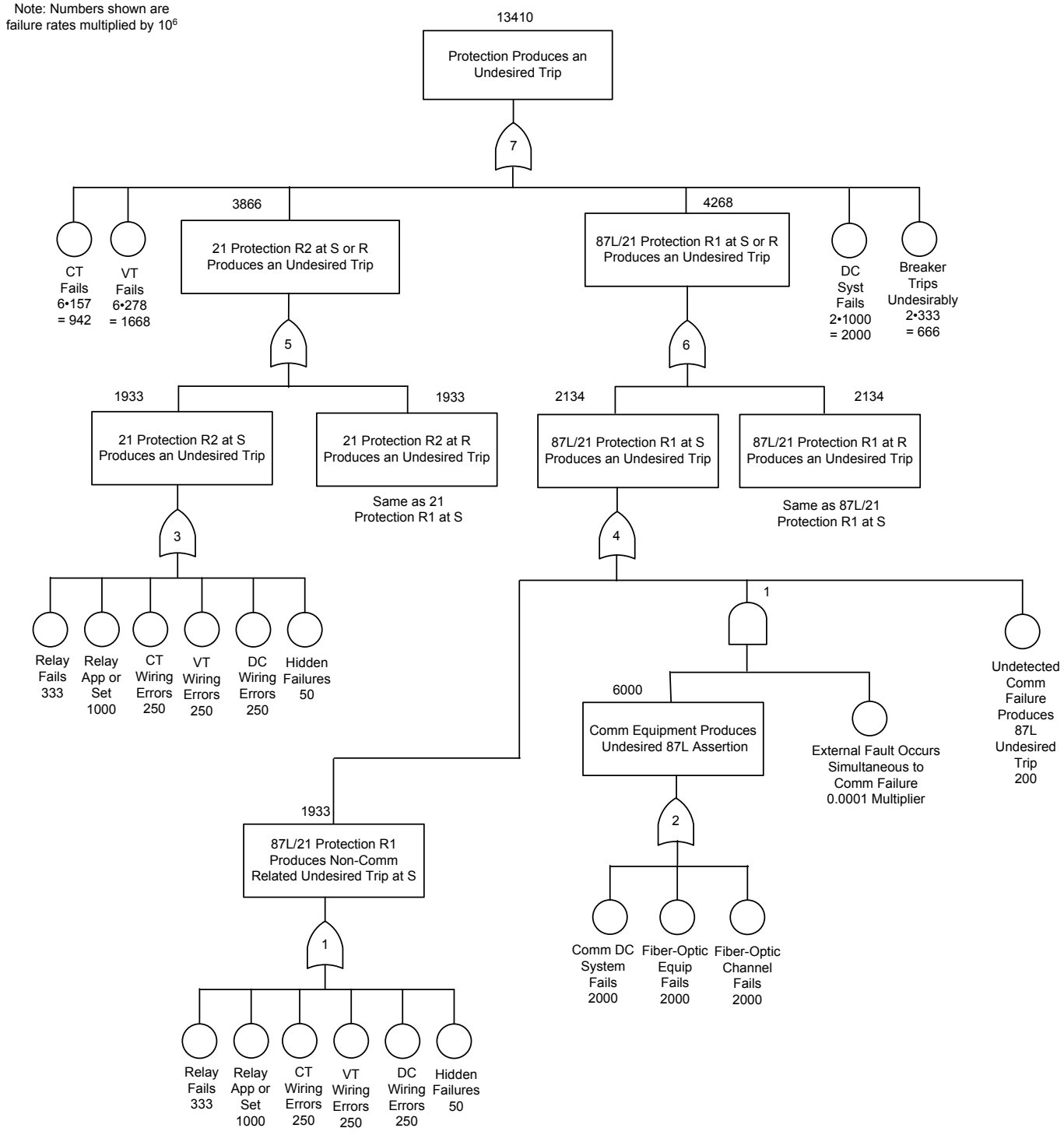


Fig. 29. Security fault tree for the combination of 87L/21 and 21 schemes in separate relays [Fig. 2(a)] with a fiber-optic channel.

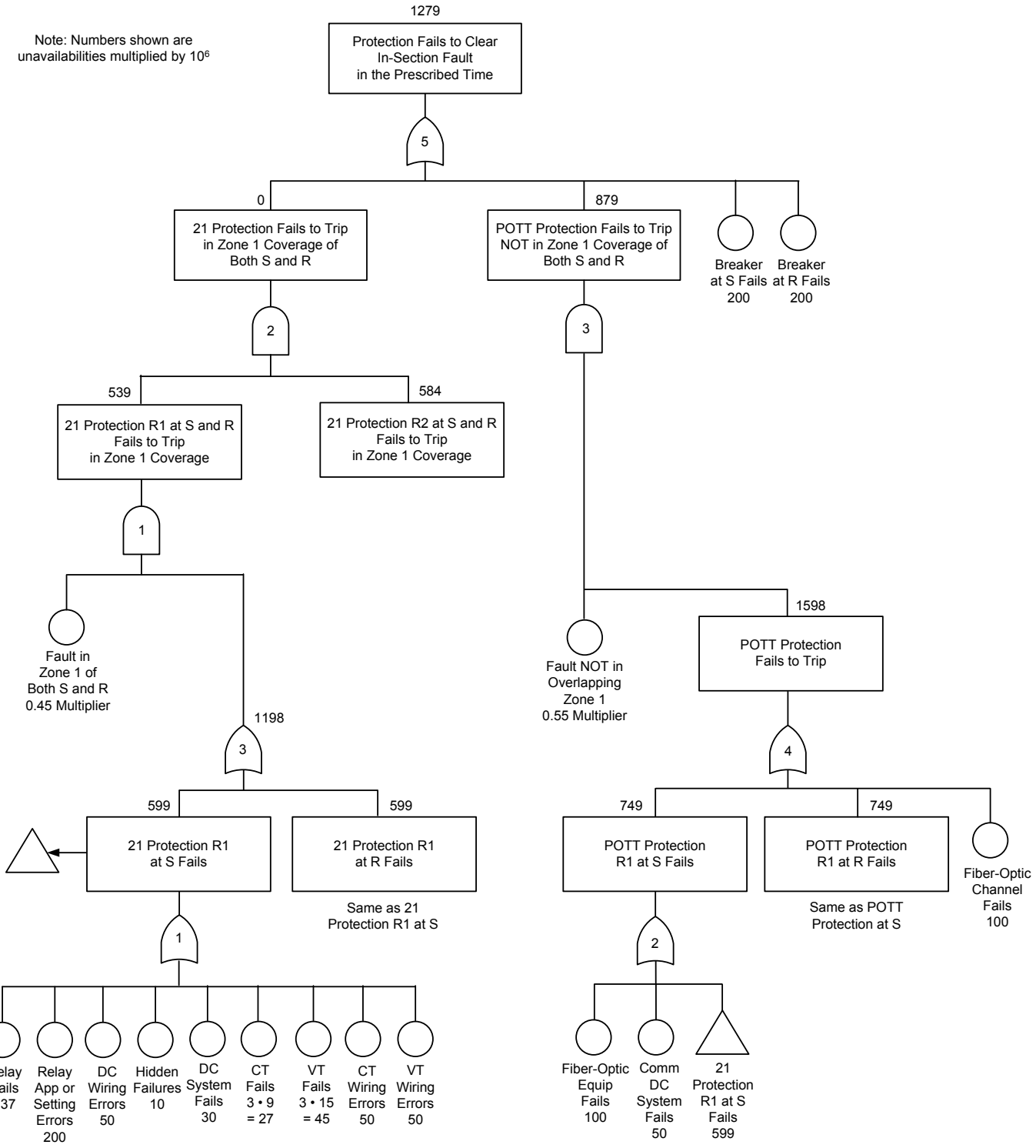


Fig. 30. Dependability fault tree for one of the POTT/21 schemes (Main 1 or Main 2) in one relay in a dual-redundant POTT/21 scheme with a fiber-optic channel.

Fig. 31 shows how redundancy improves the POTT/21 scheme dependability. The AND gate indicates that the failure of one scheme does not cause a failure to trip. The multiplication of unavailabilities reduces the output of the AND gate to a value close to zero. We represent full redundancy in Fig. 31: redundant relays, instrument transformers, dc power systems, communications channels, and circuit breaker trip coils. We can modify this fault tree as required to represent systems with lower redundancy (for example, single dc power systems or circuit breaker trip coils).

In the fault tree shown in Fig. 31, we assume that the circuit breaker has redundant trip coils, so we split the circuit breaker into two parts. We represent circuit breaker trip coil failures or dc circuit fuse operations at the basic level (below AND Gate 1). Their contribution to a failure to clear the fault is practically eliminated by the AND gate. If the trip coils

operate correctly, a breaker failure to interrupt current (a stuck contact mechanism or a failure of the contacts to extinguish the arc) will cause a failure to clear the fault, no matter the redundancy of the scheme. Hence, we represent breaker failures to interrupt current above the AND gate as an input to OR Gate 1. Because the other input to this OR gate has a very low unavailability value (because of redundancy), the breaker failures to interrupt current become the dominant factor in the scheme dependability. This fact emphasizes the importance of good circuit breaker maintenance. It also shows the need for breaker failure protection that will clear faults in more than 6 cycles but that could be fast enough to prevent the power system from losing transient stability.

Fig. 32 shows the security fault tree for the dual-redundant POTT/21 scheme with fiber-optic channels. OR Gate 1 reflects the effect of redundancy: any of the two POTT/21 schemes may cause an undesired trip. The result is lower security (a higher failure rate) than that of the combination of POTT/21 and 21 schemes in separate relays (Fig. 27).

Fig. 33 shows how redundancy improves the 87L/21 scheme dependability. The AND gate reflects the fact that the failure of one scheme does not cause a failure to trip. The multiplication of unavailabilities reduces the output of the AND gate to a value close to zero. We represent full redundancy in Fig. 33: redundant relays, instrument transformers, dc power systems, communications channels, and circuit breaker trip coils. We can modify this fault tree as required to represent systems with lower redundancy (for example, single dc power systems or circuit breaker trip coils).

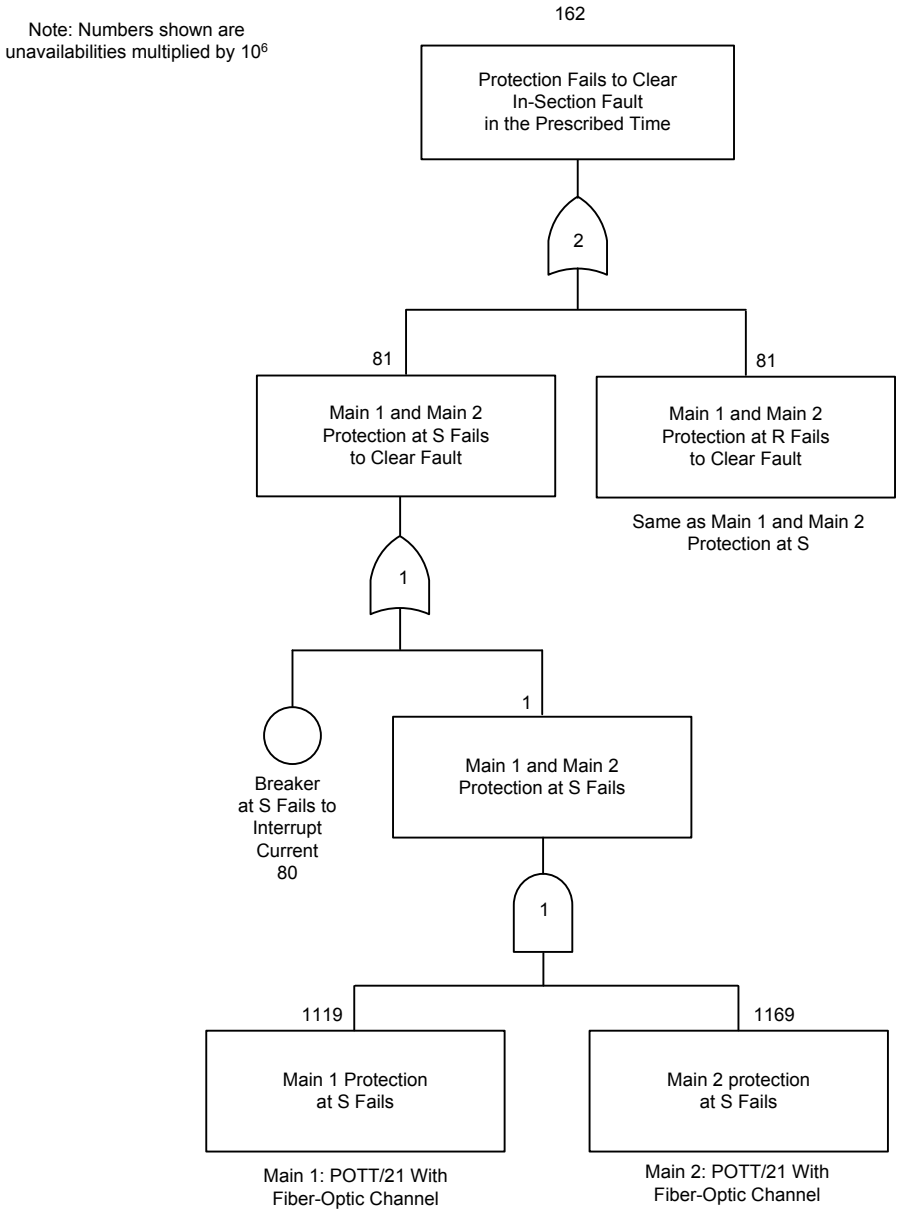


Fig. 31. Dependability fault tree for the dual-redundant POTT/21 scheme with fiber-optic channels.

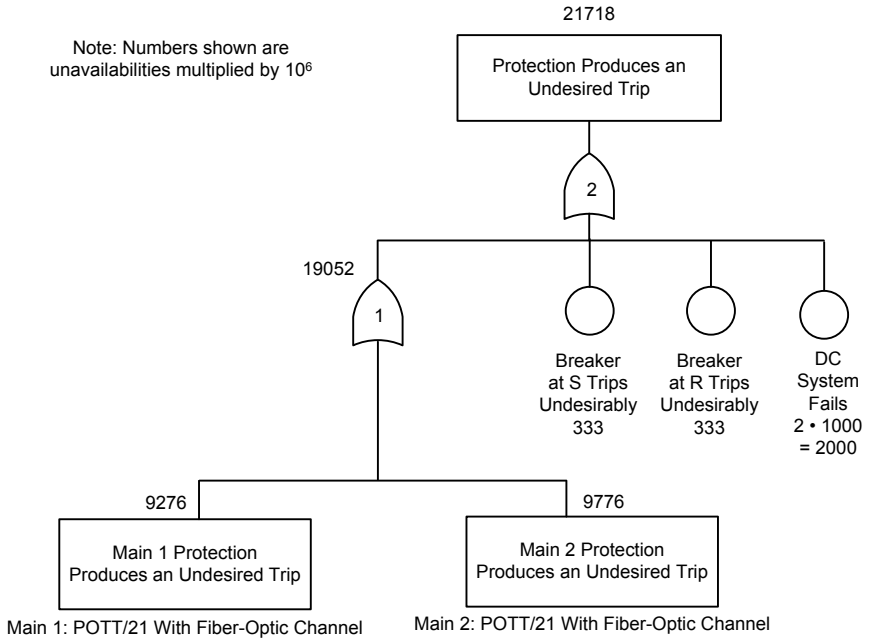


Fig. 32. Security fault tree for the dual-redundant POTT/21 scheme with fiber-optic channels.

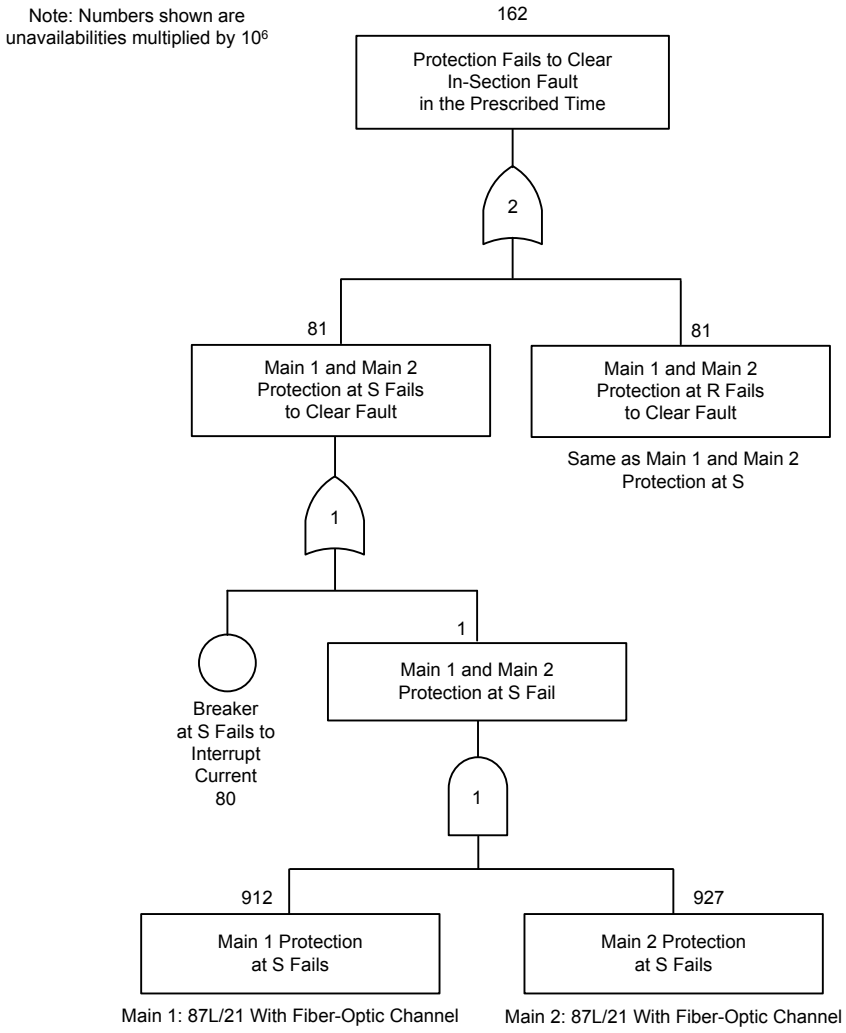


Fig. 33. Dependability fault tree for the dual-redundant 87L/21 scheme with fiber-optic channels.

Fig. 34 shows the security fault tree for the dual-redundant 87L/21 scheme with fiber-optic channels. OR Gate 1 reflects the effect of redundancy: any of the two 87L/21 schemes may cause an undesired trip. The result is lower security (a higher failure rate) than that of the 87L/21 and 21 schemes in separate relays (Fig. 29).

Fig. 35 shows the dependability fault tree for a triple-redundant two-out-of-three voting 87L/21 scheme with fiber-optic channels. The scheme has three independent 87L/21 schemes (three relays, three communications channels, three sets of instrument transformers, three dc power systems, and circuit breakers with three trip coils). Actually, circuit breakers have only two trip coils. However, if the voting scheme sends the tripping signal to both trip coils, the fault tree is slightly different from that of Fig. 35 but the scheme reliability is practically the same. Tripping occurs when at least two of the schemes operate. The effect of the voting logic is that the output of AND Gate 2 is practically zero (very high dependability). Hence, breaker failures to interrupt current determine the scheme dependability. In this analysis, we assume that the three schemes have the same R_F coverage. If the schemes had different R_F coverages (because of different settings, principles of operation, or manufacturers) and two of the schemes did not detect a high-resistance in-section fault, the two-out-of-three voting scheme would fail to clear the fault. Such a combination of schemes may consist, for example, of two 87L schemes using only 87LP elements with a third 87L scheme that includes 87LP and 87LQ elements. For this reason, we recommend that voting schemes use relays with the same R_F coverage.

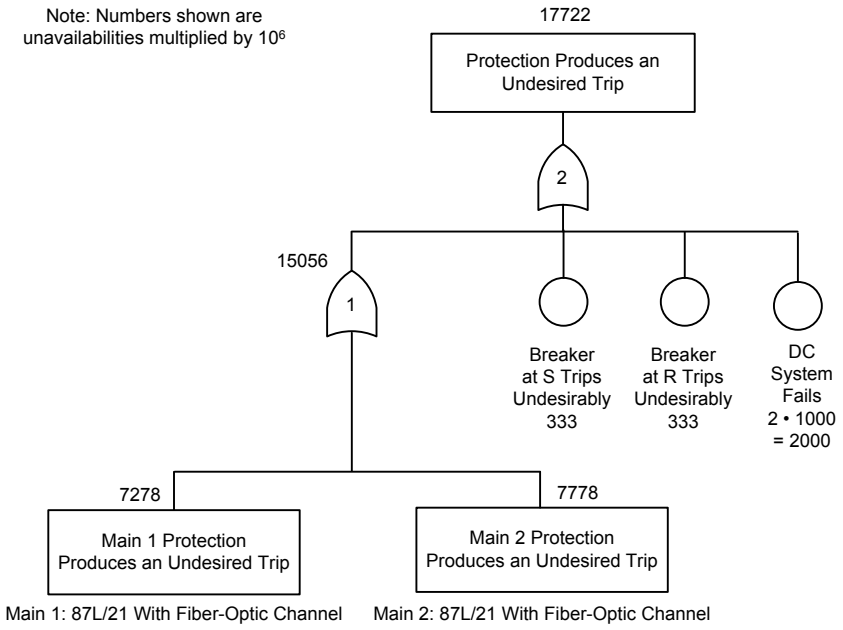


Fig. 34. Security fault tree for the dual-redundant 87L/21 scheme with fiber-optic channels.

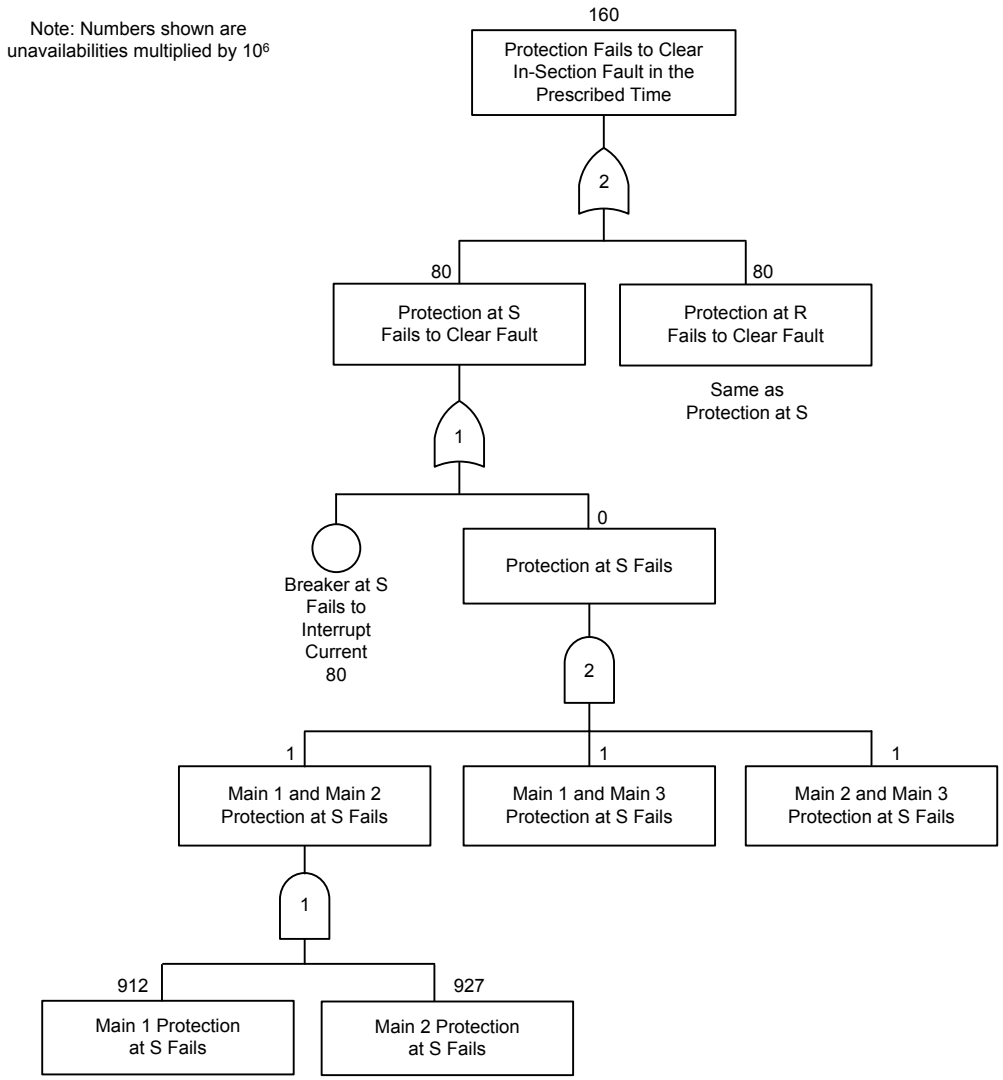


Fig. 35. Dependability fault tree for the triple-redundant two-out-of-three voting 87L/21 scheme with fiber-optic channels.

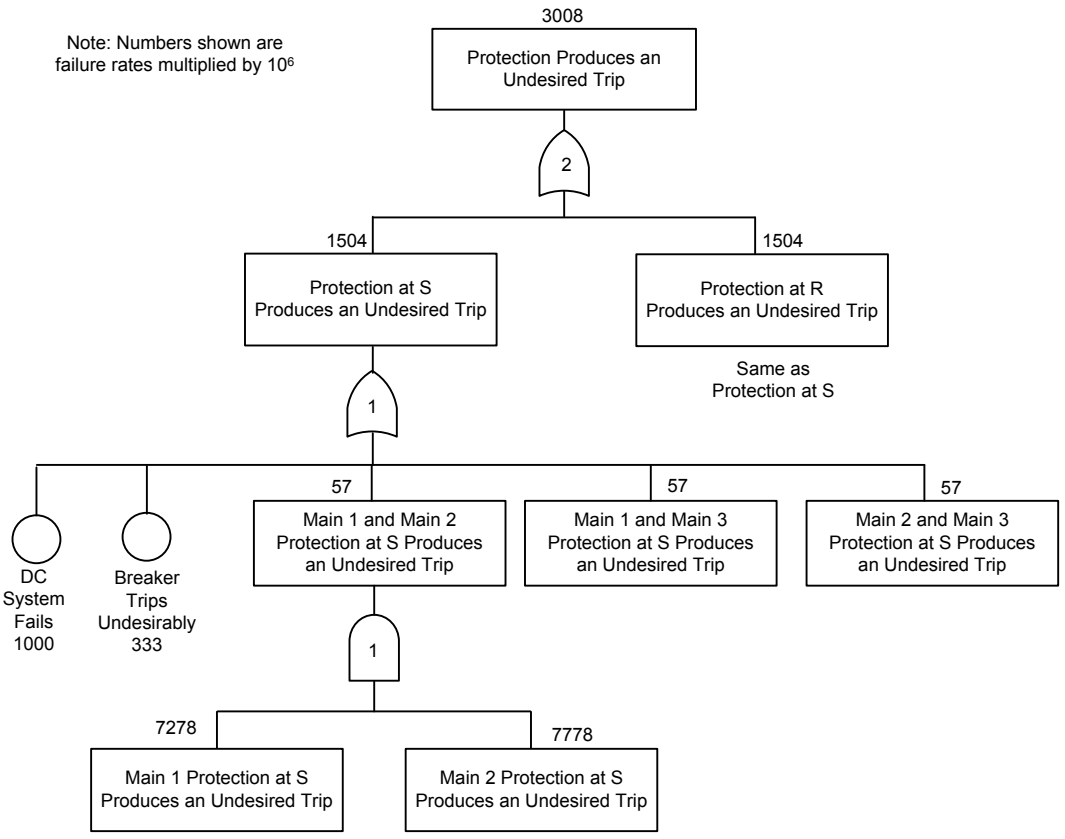


Fig. 36. Security fault tree for the triple-redundant two-out-of-three voting 87L/21 scheme with fiber-optic channels.

Fig. 36 shows the security fault tree for the triple-redundant two-out-of-three voting 87L/21 scheme with fiber-optic channels. AND Gate 1 reflects the fact that two schemes need to misoperate to cause an undesired trip. The result is very high security (a low failure rate).

Table VII of the Appendix summarizes the results obtained from the fault tree analysis. Fig. 37 and Fig. 38 present these results in a graphical form. Lower values in these figures mean higher reliability.

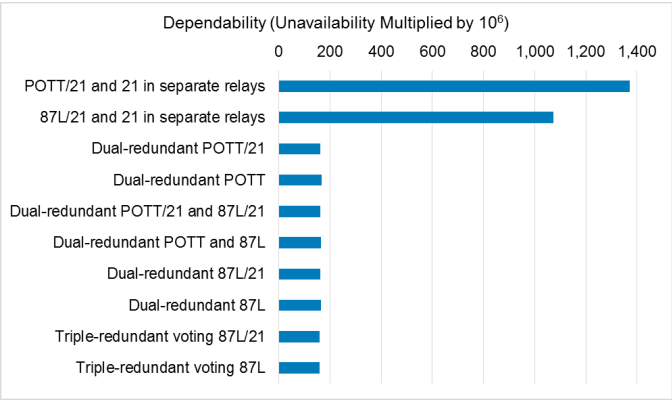


Fig. 37. Fault tree analysis results: Line protection dependability comparison.

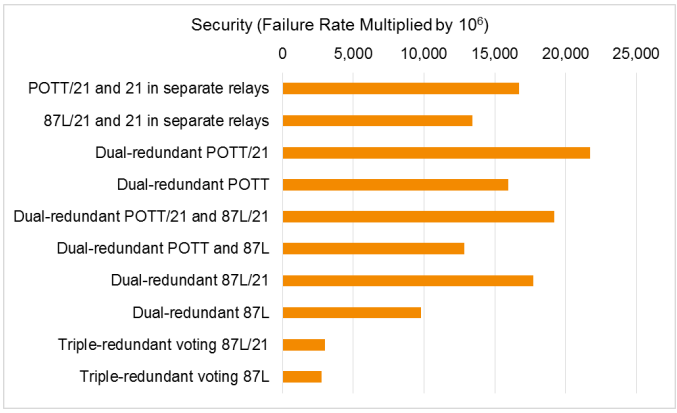


Fig. 38. Fault tree analysis results: Line protection security comparison.

VII. Protection System Selectivity Analysis

As mentioned before, selectivity is the ability of a protection system to eliminate a fault in the shortest time possible with the least disconnection of system components. By striving for high-speed tripping on all line terminals while ensuring high levels of security and dependability, we essentially achieve selectivity.

VIII. Practical Considerations

In this section we discuss the line protection challenges presented by series-compensated, mutually coupled, multiterminal, and short lines. We also discuss distance element problems when applied to extra-high-voltage (EHV) lines that require single-pole tripping and reclosing. In addition, we describe the advantages of 87L protection in dealing with these complex transmission line protection applications.

A. Series Compensation [18] [19]

Series-compensated lines present unique challenges for directional, distance, and 87L elements because the transient response of the series capacitor is not readily predictable. Series compensation introduces errors in the impedance that distance elements estimate. The series capacitor modifies the line impedance that the relay measures. Furthermore, subharmonic frequency oscillations cause the impedance estimation to oscillate. The basic problem is that the impedance estimation depends on the state of the capacitor protection.

A voltage inversion is a change of approximately 180 degrees in the voltage phase angle. For elements responding to phase quantities, voltage inversion can occur for a fault near a series capacitor if the impedance from the relay to the fault is capacitive rather than inductive. Voltage inversion can cause directional and distance elements to operate incorrectly. Close-in, three-phase, bolted faults present an additional problem to directional and distance elements responding to phase voltages because these elements lose their polarizing voltage. In series-compensated lines, the voltage at the fault side of the series capacitor collapses and voltage reverses on the other side. In particular, external faults may appear to be internal, and internal faults may appear to be external. Memory polarization and offset characteristics in directional elements can make distance and directional elements secure for voltage inversions.

A current inversion occurs on a series-compensated line when, for an internal fault, the equivalent system at one side of the fault is capacitive and the equivalent system at the other side of the fault is inductive. The current flows out of the line at one terminal, which is referred to as current outfeed. For high-resistance faults, the low fault current prevents capacitor bypassing and creates conditions for a current inversion. Current inversion can also occur in negative- or zero-sequence networks. Current inversion affects directional, distance, phase comparison, and differential elements responding to phase or sequence-component quantities. Current inversions are unlikely, but they may occur under certain conditions.

87L protection is an excellent choice for series-compensated lines. 87L elements are immune to voltage inversions and more tolerant of current inversions than are directional or distance elements. In particular, the Alpha Plane 87L elements described in [20] are very tolerant of current inversion and subharmonic frequency transients.

B. Mutual Coupling [21]

Magnetic mutual coupling affects ground directional overcurrent elements responding to zero-sequence quantities, which compromises directional comparison scheme security. Mutual coupling may cause zero-sequence polarizing quantity inversion when this coupling is strong enough to dominate over the electrical connection between lines. An extreme case is when the zero-sequence network of the protected line is electrically isolated from the zero-sequence network of the faulted line. Zero-sequence polarized directional elements can misoperate for reverse faults under certain system configurations and circuit breaker switching conditions. A solution to this problem is to use 67Q elements.

Magnetic mutual coupling affects ground distance elements and compromises distance and directional comparison scheme security and dependability. Ground distance elements overreach (a concern for Zone 1) when the zero-sequence currents in the protected line and the coupled line flow in opposite directions and underreach (a concern for Zone 2) when these currents flow in the same direction. Solutions to this problem include applying reach or zero-sequence compensation settings that consider the mutual coupling effect.

87L protection is not affected by mutual coupling and is an excellent solution for mutually coupled lines.

Because of mutual coupling, operating a double-circuit transmission line as a single circuit with jumpers placed across similar phases along the line causes phase and ground distance element underreaching [21]. Applying 87L schemes solves this problem.

C. Single-Pole Tripping [22] [23]

Single-pole tripping and reclosing protection schemes are designed to trip only the faulted phase on single-phase-to-ground faults and all three phases on multiphase faults. When a single-phase-to-ground fault occurs on a transmission line, the faulted phase is tripped and automatically reclosed after a suitable dead time, which should be long enough for the secondary arc caused by the coupling with the unfaulted phases to extinguish. If the fault is cleared and of transient nature, the scheme resets. If the fault is still present when the pole is reclosed, all three poles are tripped and no further reclosing takes place. When a multiphase fault occurs on a transmission line, all three poles are tripped and typically no reclosing takes place.

A single-pole tripping scheme must distinguish between multiphase faults and single-phase-to-ground faults. For multiphase faults, the scheme trips three circuit breaker poles. For single-phase-to-ground faults, the scheme produces a single-pole tripping output associated with the faulted phase. For this reason, the scheme requires a faulted phase identification logic.

The open-phase condition following a single-pole trip on a transmission line creates unbalances that can affect relays. The protection elements must be designed to be immune to the unbalance effects or must be desensitized or blocked during the single-pole open time. In addition, single-pole tripping

schemes must detect faults that occur or evolve during the single-pole open time. For this reason, the location of the voltage transformers (VTs) is very important in schemes based on distance or directional overcurrent elements. VTs located on the line side of the circuit breaker present challenges to distance and directional elements.

Polarizing quantity corruption can occur during single-pole open conditions in applications with line-side VTs if one of the input voltages to the memory polarizing algorithm is corrupted. Incorrect memory polarization may cause distance element misoperation. The voltage magnitude and angle on the line side of the circuit breaker during single-pole open conditions depend on whether a secondary arc still exists on the open phase, whether line shunt reactors are present, and whether power flows in the two healthy phases.

Shunt reactors located on the line side of the circuit breakers compensate the line charging currents and reduce overvoltages in long transmission lines. When the circuit breakers open at both line ends, the remaining circuit is basically an RLC circuit with stored energy in the reactor inductance and the line capacitance. The shunt reactors interact with the line capacitance and maintain ringing line voltages for several cycles. With line-side VTs, these ringing voltages corrupt the distance protection polarization and frequency estimation.

An evolving fault may start as a single-phase-to-ground fault and then involve additional phases while the initial fault is being cleared or during the reclosing dead time of the original faulted phase. Single-pole tripping schemes should detect and clear evolving faults.

In summary, single-pole tripping schemes must identify the faulted phases, avoid misoperation on unbalances created by the open phase condition, and detect faults that occur or evolve during the single-pole open time. These requirements increase the complexity of the logic of single-pole tripping schemes with distance and directional overcurrent elements. 87L schemes perform well during the single-pole open time and detect evolving faults naturally, because they compare the line terminal currents on a per-phase basis.

D. Multiterminal and Tapped Lines

Multiterminal lines have three or more terminals, each with substantial generation. Distance protection application to three-terminal lines is more complex than its application to two-terminal lines because of the large variety of possible tap locations, line impedances, source impedances, and system operation conditions [24].

We need to determine the impedance measured by distance elements for various fault and system conditions when calculating their settings. The measured impedance is not always the actual impedance of the line section from the relay location to the fault point. The voltage measured by the relay is the voltage drop between its location and the fault, which is affected by the infeed effect from the sources connected at the taps between the relay and the fault location. Thus, the measured impedance depends on the current contributions from the other terminals. The infeed increases the measured impedance value and causes distance elements to underreach.

In some three-terminal applications, there may be an outfeed current at one of the terminals during an internal line fault rather than an infeed current [3]. In this case, the measured impedance at the other line terminals may be smaller than the actual impedance to the fault (distance elements tend to overreach). An additional problem is that a forward-looking distance element at the terminal with outfeed current will not detect this internal line fault. In fact, if there is a blocking element at the terminal with outfeed current, it may declare the internal fault as an external fault and prevent tripping in a DCB scheme. If the Zone 1 elements at one of the other terminals respond to the fault, they will initiate circuit breaker tripping and remove the outfeed current. The remaining line terminals may then trip via the directional comparison scheme; however, tripping may be delayed by the current reversal logic.

In many three-terminal line applications, the third terminal may be a transformer-terminated load tap. In such applications, there may be no positive- or negative-sequence current source at the tap. However, if the line side of the transformer has a grounded-wye connection, there will be a significant zero-sequence current contribution. Therefore, in this application, the infeed effect does not affect the phase distance elements but it does affect the ground distance elements.

87L schemes for multiterminal lines handle three-terminal line protection challenges naturally. In addition, 87L schemes can handle some level of outfeed current, depending on the relay operating characteristic and the applied relay settings.

E. Short Lines

Transmission lines are sometimes classified as short, medium, and long. The IEEE Power and Engineering Society (PES) Power System Relaying Committee (PSRC) established the following criteria for line length in terms of the SIR [25]:

Short line: SIR > 4.0.

Medium line: 0.5 < SIR < 4.0.

Long line: SIR < 0.5.

Short line protection problems related to the high SIR value include low voltage at the relay location during faults and CCVT transients. Detecting high-resistance faults is another short line protection problem.

Microprocessor-based relays do not require a considerable amount of energy to operate. However, when the relay input voltage is very low, distance element operation is not well-defined and/or the operating speed is unsatisfactory. For proper distance element performance during faults, the voltage measured by the relay must be above the design voltage threshold. The SIR value determines the positive-sequence voltage at the relay location for a three-phase fault at the relay reach point. As the SIR increases, the voltage at the relay location decreases, which limits distance element sensitivity in short lines.

Coupling capacitor voltage transformer (CCVT) transients may impair the voltage measured by the relay during faults and cause distance elements to overreach. A Zone 1 overreaching condition due to CCVT transients is generally more likely in short lines (because of the higher SIR) than in long lines [26]. For high SIR values, the CCVT transient lasts longer and is more severe because the voltage at the CCVT location is low for remote faults. Also, the CCVT transient can distort the voltage waveform because most of the voltage signal consists of the CCVT transient output [3]. For low SIR values, the voltage at the CCVT location is high for remote faults and the CCVT transient has little effect on the voltage waveform. The traditional solutions (i.e., reducing Zone 1 reach or delaying its operation) affect high-speed fault clearing.

Modern microprocessor-based relays include logic to prevent the Zone 1 element from operating because of CCVT transients [3]. If CCVT blocking logic is enabled and the relay detects a high SIR value when a Zone 1 element picks up, the logic delays tripping for as long as 1.5 cycles to allow the CCVT transient to stabilize. For each fault, the relay estimates the SIR value as the ratio of the positive-sequence source impedance to the Zone 1 reach setting. The logic does not require settings. If the distance calculation stabilizes before 1.5 cycles, the logic unblocks tripping. Therefore, Zone 1 elements operate without significant delay when the CCVT has good transient response. A better solution is 87L protection, which does not use voltage information.

Another consideration for short line protection is R_F coverage. For ground faults, the total fault resistance can be very high, such as in the case of a fault involving a tree, a fault to ground through a fire, or a fault on a tower with very high footing resistance. The infeed effect from the remote line terminal current on the resistive fault path magnifies the measured fault impedance and shifts its phase angle. The apparent fault impedance may be much higher than the line impedance. A ground distance element may not detect these high-resistance faults. A better solution is ground directional overcurrent protection (67N) or 87L protection with 87LG or 87LQ elements [26].

Even for phase faults, the measured fault impedance may be high, as compared with the line impedance, and may limit phase distance element sensitivity.

F. Advantages of 87L Protection [3]

87L protection schemes do not require voltage information, thereby avoiding problems for close-in faults, blown potential fuses, ferroresonance in VTs, transients in CCVTs, and voltage inversion. However, 87L elements may require voltage information to calculate the line charging current in applications for long lines or cables. 87L protection schemes are almost immune to unbalances, current reversals on parallel lines, power swings, and magnetic mutual coupling. In addition, they perform well for evolving, intercircuit, and cross-country faults; tolerate high line loading; and may handle outfeed conditions, depending on their operating characteristic.

IX. Conclusion

This paper compares several line protection schemes, including distance schemes, directional comparison schemes using distance and directional elements, and 87L schemes in terms of speed, sensitivity, reliability, and selectivity. From this comparison, we conclude the following:

- The operating speed of phasor-based protection elements depends mainly on the window length of the digital band-pass filter. Modern phasor-based line protection elements with half-cycle or one-cycle data windows typically provide PSTT values of one cycle or less without impairing security.
- In line pilot protection schemes, the communications system delays operation. A relay-to-relay communications channel over a direct optical fiber introduces the smallest delay (0.8 ms/100 miles). In digital multiplexed fiber-optic networks, the multiplexer adds approximately 0.5 ms and each repeater (if used) adds 24 μs. A PLC channel adds a delay between 2 and 8 ms. Protection-class digital radios introduce delays between 4.8 and 7.4 ms.
- Computer simulation studies of three different example power systems show that modern protection schemes using high-speed elements and fast communications channels produce low (always under 1.2 cycles) and consistent PSTT values for various fault types and locations, line lengths, and source strengths. Many actual system events have validated the results of these simulations. Time-domain protection can further improve speed.
- Plotting the maximum value of R_F detected by a line protection scheme as a function of the fault distance allows us to simultaneously analyze the scheme sensitivity and speed. The R_F coverage regions resulting from computer simulation studies of three different example power systems show the higher sensitivity and speed of 87L schemes using 87LG and 87LQ elements as compared with POTT schemes using either 67N or 21N (or 21X) elements. These studies also show that 67N elements provide higher sensitivity and speed than 21N (or 21X) elements.
- From the dependability and security fault trees for different line pilot protection schemes with fiber-optic channels, we conclude the following:
  - The combination of 87L/21 and 21 schemes in separate relays provides higher dependability and security than the combination of POTT/21 and 21 schemes in separate relays.
  - The dual-redundant schemes with direct Zone 1 tripping (dual POTT/21, POTT/21 and 87L/21, and dual 87L/21 schemes) have much higher dependability and slightly lower security than the corresponding combinations of schemes in separate relays.
  - Removing Zone 1 tripping from the dual-redundant schemes improves their security without impairing

their dependability. However, direct Zone 1 tripping is faster than communications-based schemes (there is no channel delay) and enhances power system stability by providing faster clearing of close-in faults.

  - The triple-redundant voting 87L/21 scheme is significantly more secure than the dual-redundant 87L/21 and 87L schemes. Removing Zone 1 tripping (triple-redundant voting 87L scheme) further improves security.

- A protection scheme that provides high-speed tripping on all line terminals and high levels of security and dependability inherently provides selectivity.
- 87L protection is the best solution for lines. 87L protection does not require voltage information and is almost immune to unbalances, current reversals on parallel lines, power swings, and magnetic mutual coupling. 87L protection performs well for evolving, intercircuit, and cross-country faults; tolerates high line loading; and may handle outfeed conditions, depending on its operating characteristic.
- Triple-redundant voting 87L and dual-redundant 87L protection schemes allow maximizing line protection speed, sensitivity, dependability, security, and selectivity.

X. Appendix

Table V summarizes the results of the reliability study using fault trees reported in [1].

Table VI summarizes the reliability indices used in the fault tree analysis. We used the reliability indices reported in [1] (which provides a detailed justification of these indices), with one exception. We modified the value of unavailability caused by relay application and setting errors based on a recent North American Electric Reliability Corporation (NERC) report that provides protection system misoperation data for a fifteen-month period [27]. NERC concludes that incorrect settings, logic, and design errors caused 28 percent of the misoperations, while relay failures caused 20 percent of the misoperations. Using this information, we assumed $U = 200 \bullet 10^{-6}$ for relay application or settings errors (instead of the $U = 1{,}000 \bullet 10^{-6}$ value used in [1]).

Table VII summarizes the results of the reliability study using fault trees described in this paper.

Table V
Line Protection Reliability Comparison [1]

Protection Scheme	Dependability (Unavailability • 10^6)		Security (Failure Rate • 10^6)	
	Normal Commissioning Testing	Comprehensive Commissioning Testing	Normal Commissioning Testing	Comprehensive Commissioning Testing
Basic POTT (microwave)	2,562	1,339 (1.9 times)	23,318	12,938 (1.8 times)
Basic POTT (optical fiber)	2,452	1,229 (2.0 times)	22,784	12,364 (1.8 times)
Basic DCB (PLC)	2,122	943 (2.3 times)	48,704	33,180 (1.5 times)
Dual-redundant POTT	168	162 (1.04 times)	27,052	16,072 (1.7 times)
Dual-redundant POTT with relays from different manufacturers	174	162 (1.07 times)	29,552	16,572 (1.8 times)
Dual-redundant POTT with common-mode failures	1,178	268 (4.4 times)	28,102	16,202 (1.7 times)
Fully redundant voting POTT	160	160 (1.0 times)	916	750 (1.2 times)
Voting POTT: Two schemes share dc power system	220	172 (1.3 times)	2,892	1,146 (2.5 times)
Voting POTT: Two schemes also share communications channel	1,120	992 (1.1 times)	6,592	4,224 (1.6 times)
Voting POTT: Two schemes also share instrument transformers	1,464	1,136 (1.3 times)	10,182	6,826 (1.5 times)
Fully redundant voting POTT with common-mode failures	1,170	266 (4.4 times)	1,966	880 (2.2 times)

Note: The numbers in parentheses represent the effect of comprehensive commissioning testing. These numbers are the ratios of the unavailabilities or failure rates with normal testing to the unavailabilities or failure rates with comprehensive testing.

TABLE VI
RELIABILITY INDICES USED IN FAULT TREES [1]

Event	Dependability	Security	
	Unavailability • 10^6	MTBF (Years)	Failure Rate • 10^6
Relay fails	137	3,000	333
Relay application or settings errors	200	1,000	1,000
Circuit breaker fails	200	3,000	333
Circuit breaker fails to interrupt current	80	–	–
DC power system fails	30	1,000	1,000
Current transformer (CT) fails	9	6,370	157
VT fails	15	3,600	278
Fiber-optic equipment fails	100	500	2,000
Fiber-optic channel fails	100	500	2,000
Communications dc power system fails	50	500	2,000
DC system wiring errors	50	4,000	250
CT or VT wiring errors	50	4,000	250
Hidden failures	10	20,000	50

Note: The U = 200 • 10^{-6} value for relay application or settings errors shown in this table is different from the value reported in [1].

TABLE VII
LINE PROTECTION RELIABILITY COMPARISON

Protection Scheme	Dependability (Unavailability • 10^6)	Security (Failure Rate • 10^6)
Combination of POTT/21 and 21 in separate relays	1,372	16,708
Combination of 87L/21 and 21 in separate relays	1,072	13,410
Dual-redundant POTT/21	162	21,718
Dual-redundant POTT	168	15,942
Dual-redundant POTT/21 and 87L/21	162	19,220
Dual-redundant POTT and 87L	166	12,864
Dual-redundant 87L/21	162	17,722
Dual-redundant 87L	164	9,786
Triple-redundant voting 87L/21	160	3,008
Triple-redundant voting 87L	160	2,744

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XII. BIOGRAPHIES

Héctor J. Altuve received his B.S.E.E. degree in 1969 from the Central University of Las Villas in Santa Clara, Cuba, and his Ph.D. degree in 1981 from Kiev Polytechnic Institute in Kiev, Ukraine. From 1969 until 1993, Dr. Altuve served on the faculty of the Electrical Engineering School at the Central University of Las Villas. From 1993 to 2000, he served as professor of the Graduate Doctoral Program in the Mechanical and Electrical Engineering School at the Autonomous University of Nuevo León in Monterrey, Mexico. In 1999 through 2000, he was the Schweitzer Visiting Professor in the Department of Electrical and Computer Engineering at Washington State University. Dr. Altuve joined Schweitzer Engineering Laboratories, Inc. (SEL) in January 2001, where he is currently a distinguished engineer and dean of SEL University. He has authored and coauthored more than 100 technical papers and several books and holds four patents. His main research interests are in power system protection, control, and monitoring. Dr. Altuve is an IEEE fellow.

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