

Analysis and Lessons Learned from Protection Operations during a Fault, Resulting in the Loss of over 750MW of Generation and Several EHV Transmission Lines

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I. Introduction

An internal flashover in an open generator breaker occurred at a large generating station with over 2000 MW of generation. The fault and the associated protection system operations resulted in the loss of over 700MW of generation and the loss of several EHV lines.

This generating station has a breaker-and-a-half configuration with a potential paralleling scheme to provide voltages to the line relays. Three-phase Bus CVTs are connected in parallel to provide a voltage source to the line relays and provide redundancy for the loss of a Bus CVT. At the time of the disturbance, Bus 1 CVT had issues and all the line relays received voltage from Bus 2 CVT.

The initial fault internal to the open generator breaker caused the adjacent line to trip. When a breaker at the local substation attempted a reclose to restore the line, one of its bushing CTs saturated. This CT was wired to the low impedance bus differential relay protecting Bus 2. The CT saturation caused the high set differential element in this relay to operate for the external fault. As a result, the bus differential relay tripped and rolled the Bus 2 lockout.

When Bus 2 locked out, all the line relays lost their voltage measurement. The conventional loss of potential (LOP) logic in the line relays did not assert. Some of the line relays tripped on a zone 1 phase distance element, while other line relays restrained from tripping. The decision on whether to trip depended on the relay design, the fault detector setting, the memory duration setting for positive sequence memory polarization, and the load current flowing on the corresponding line.

This paper provides detailed analysis of the impact of CT saturation on the operation of the bus differential relay, the reason for the lack of LOP assertion in all relays, and the impact of memory duration on the response of distance relays. The paper also presents lessons learned and corrective actions implemented.

II. Event

The single line diagram in Figure 1 below shows the substation layout at the start of this event (breaker and a half arrangement of buses with potential paralleling scheme). A few weeks before this event, the bus 1 potential parallel scheme lockout rolled when a nearby transformer was energized. As a result, bus 1 potentials were removed from the potential parallel scheme and all relays in the substation were connected to bus 2 potential source (CVTs). A transmission operator tried to reset the potential parallel scheme lockout but was unable to. A crew was requested to investigate, but the lockout was still rolled when this event started. All transmission lines have primary and secondary protective relays.

Generator 1 was brought up to speed ready to be connected to the system through breaker BKR01. Phase B to ground fault internal to breaker BKR02 (that was open) resulted in tripping the line to SUB A, followed by the failed high speed reclose attempt from the remote end and another time delayed reclose attempt from the local end (BKR03) breaker.

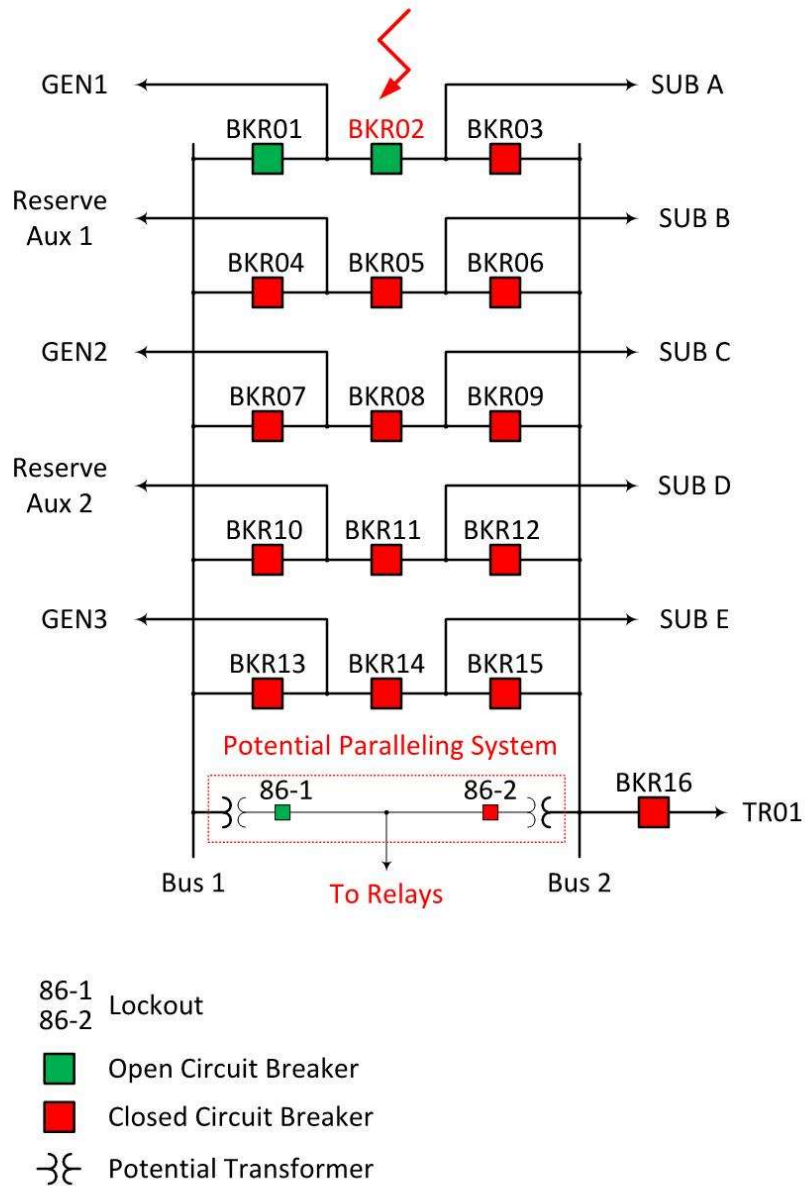
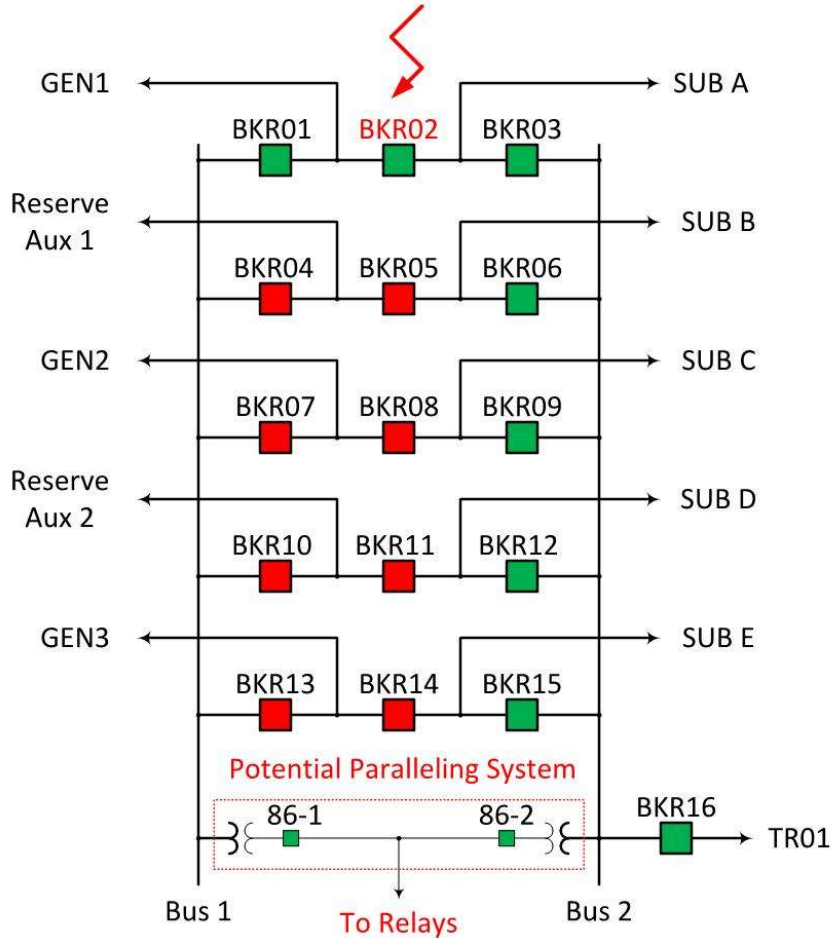


Figure 1. Single-line diagram of the substation at the start of the event

The local breaker (BKR03) time delayed failed reclose attempt resulted in bus differential relay operation due to CT saturation that tripped all breakers connected to Bus 2 and de-energized CVT resulting in no voltage to all relays in the substation. The single line diagram in Figure 2 below shows the substation layout after the Bus 2 lockout.



- 86-1 Lockout
- 86-2 Lockout
- Open Circuit Breaker
- Closed Circuit Breaker
- $\}\{\}$ Potential Transformer

Figure 2. Single-line diagram of the substation after the Bus 2 lockout

The fault internal to BKR02 should appear as a reverse fault for all the relays (except those protecting the lines to GEN1 and SUB A) and after fault clearing, relays were seeing only load currents out on the lines or from two generators with no potentials connected to them.

There was no declaration of LOP and there was no distance relay operation from one manufacturer, but other manufacturer relay's phase distance zone 1 element tripped transmission lines to GEN2, GEN3, SUB B, and SUB D. Transmission line to SUB C did not trip due to load current direction and memory voltage duration. Transmission line to SUB E did not trip because the remote end of the line

III. Bus differential operation

When line protection attempted to reclose BKR03, high magnitude current close to 70kA peak flowed through the BKR03. The CT of this breaker was already stressed by the 1st fault and remanence effect contributed to the CT phase saturation. Figure 4 below depicts phase B currents in all circuits connected to the bus #2, including BKR03 current. Looking at this figure, however, CT saturation is not obvious.

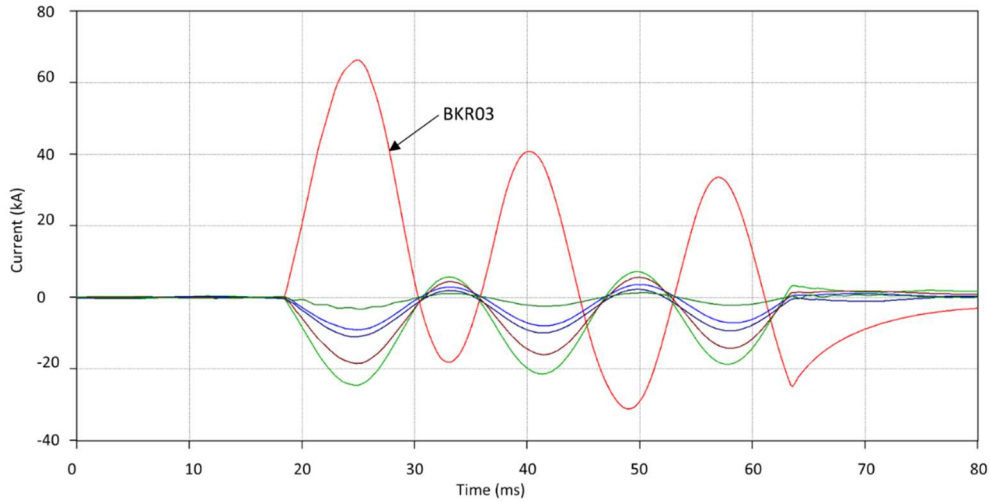


Figure 4. Current phase B in all connected to the bus #2 circuits

To demonstrate CT saturation, all currents except BKR03 current, were summed up and inverted. Ideally, current from all other circuits feeding the fault through the BKR03 would be equal to BKR03 current with opposite polarity resulting in zero differential current. However, as it's shown in the Figure 5, in approximately one cycle, BKR03 CT starts saturating, as observed by the sudden loss of DC in the current waveform. The resulting errors in phase angle cause raw differential peaking at 32.393kA and filtered differential magnitude as high as 11.425kA or 3.8pu. This value exceeded the 3pu pickup of the instantaneous bus differential element resulting in a trip. All bus zone CTs are C800 with a 3000/5A ratio.

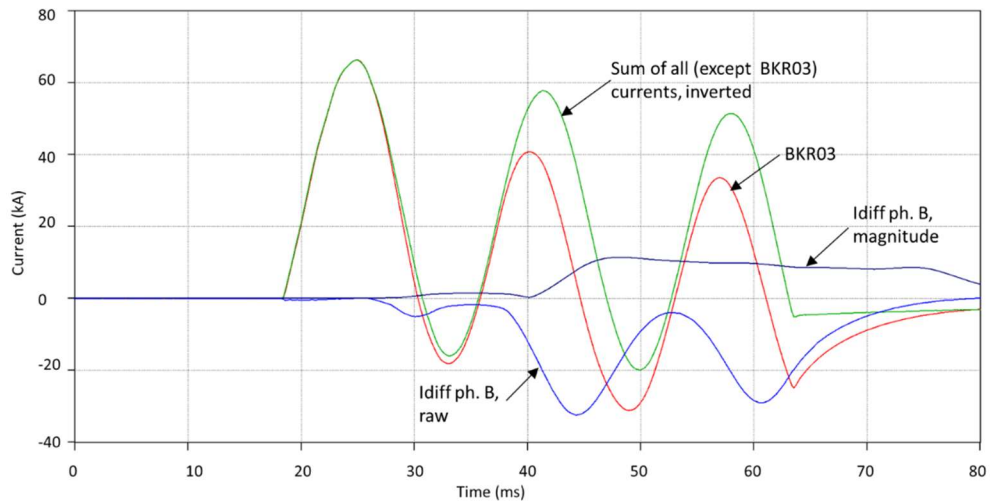


Figure 5. CT saturation in BKR03 causes high differential current

To confirm that CT saturation could theoretically occur in this situation, the necessary parameters were input to the IEEE CT saturation tool [1]. A 1pu offset in the primary current and a remanence of 0.7pu was used. The output of this tool is shown in Figure 6 below, which is very similar to Figure 5 above. This confirms that the initial fault followed by reclosing BKR03 into the fault can push the BKR03 CTs into phase saturation (error in both magnitude and current angle).

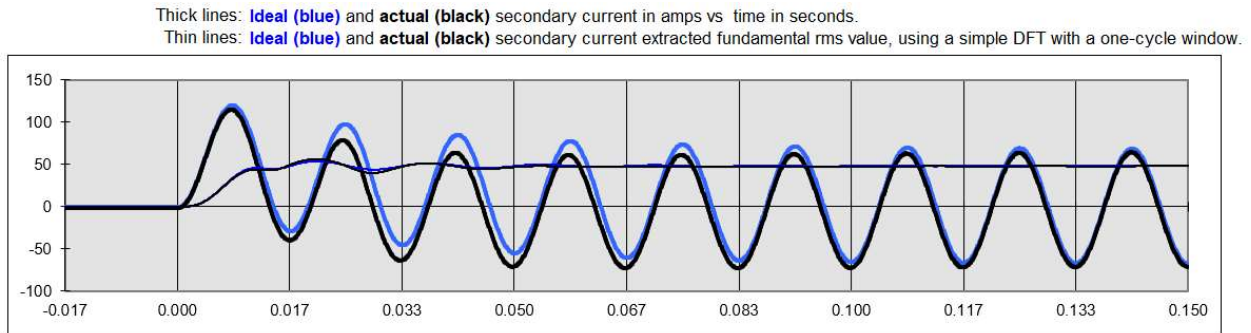


Figure 6. IEEE CT saturation tool shows BKR03 CT saturation (error in current angle)

Although the bus differential relay is equipped with a CT saturation detector, this detector picked up initially, but dropped out during fault, allowing the differential element to trip. Percent differential was above the slope in operate region as well (although this element has additional directional supervision and rate-of-change supervision). All breakers connected to the Bus 2 were tripped, however lines to substations B, C, D, and E were still carrying the load supplied from the Bus 1. Unfortunately, tripping Bus 2 left all in service line relays without potentials, since the prior potential parallel scheme lockout operation had left 86-1 lockout open. Next sections will further describe sequence of events during this major system disturbance.

IV. LOP lack of operation

Loss of potentials (LOP) is needed in distance relays to block operation when at least one phase VT voltage is lost and it's not a result of a system fault. Common design approach is to detect a disturbance (unbalance) in voltages without a corresponding disturbance in currents; when both voltages and currents are changing, this is true indication of a system fault and LOP should not operate.

Different quantities can be used to identify voltage and current disturbance, such as positive-sequence voltage and current, negative-sequence voltage and current or zero-sequence voltage and current. Most important is that LOP has a "memory" effect of the current disturbance (fault) to prevent erroneous assertion of the LOP and would not respond to a loss of potentials for some time.

Simplified LOP logic is shown below in the Figure 7. First, LOP must operate fast for true LOP condition in order to prevent phase distance zone 1 misoperation. Once LOP has operated, it must be latched until healthy voltage is restored and is present for some time.

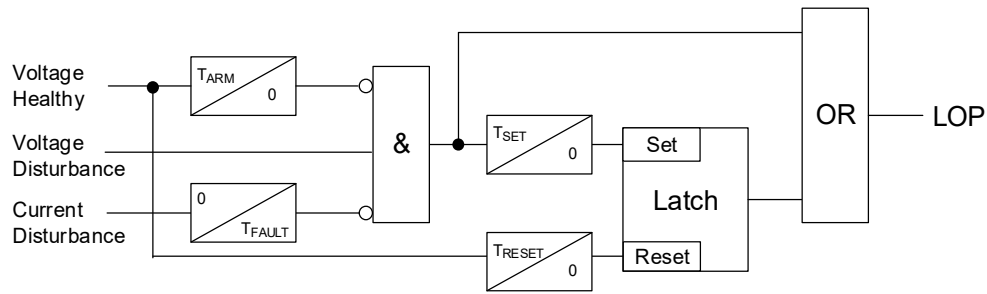


Figure 7. Simplified LOP logic

When a line is de-energized with VTs located on the line side of the breaker, LOP becomes operational after some arming time, denoted by the T_{ARM} timer, which is typically 20-30 cycles. This is because during energization voltage and current transients make it impossible to distinguish between healthy line conditions and fault or LOP conditions. Anyways, during line energization we rely on the switch-onto-fault function, rather than on the distance function. Once LOP is armed, it's monitoring voltage and current disturbance. To achieve faster operation, both are using delta quantities, comparing the present value with a previous value (1-2 cycles before). Most important and relevant to the event described in this paper is a drop-off timer T_{FAULT} in current disturbance path: this timer is needed to ensure current disturbance is not reset during fault, as fault current can come into steady state.

LOP asserts once the output of the AND gate asserts but latches after T_{SET} time. This is to account for possible racing between voltage and current disturbance to prevent erroneous LOP latching if such racing occurs. Once LOP is latched, it will be unlatched only after healthy voltage is restored.

It's obvious from this analysis, that during fault and for some time after fault, the LOP was not able to detect LOP conditions occurring immediately after fault clearance. The T_{FAULT} timer is typically hard-coded for 30-50 cycles and during this time LOP is inhibited.

This is exactly what happened during this event: when the bus differential relay operated and tripped all breakers, LOP in all line relays was inhibited due to current disturbance so the distance function was not blocked. This is a vulnerability of the line distance relays for the situation when potential paralleling scheme is relying on one bus VT only and the bus locks out during a system fault. Distance relays can trip right away or lose functionality when memory voltage expires, and this double contingency must be considered when designing the protection scheme. It's undesirable to trip an unfaulted line, but on the other hand it's not acceptable to have a line in service without adequate protection.

V. Memory voltage effect on the operation

This section will focus on the details of the distance memory and how difference in the memory voltage design can result in a different response during fault or a potentials loss. Memory voltage is a polarizing quantity for the distance comparator.

Investigation of the different response of different distance relays during this event proved direct relationship between memory duration and fault direction discrimination on the unfaulted lines to substation B and substation D.

Table 1 below clearly demonstrates this, where distance relays on these lines with a short memory tripped whereas distance relays on these lines with a long memory did not trip. At the time these relays tripped, load current was flowing into the substation from the lines to generators 2 and 3. Load current was flowing out of the substation on the lines to stations B, C, and D. At first glance, it is puzzling why the relays tripped at the same time given the different load current directions. However, this can be explained by considering the memory voltage duration.

Line	Relay	Memory	Distance operation
Line to substation D	Relay A	Short	Forward
	Relay B	Long	Reverse
Line to substation B	Relay A	Short	Forward
	Relay B	Long	Reverse
Line to substation C	Relay A	Medium	Reverse
	Relay B	Long	Reverse
Line to generator 2	Relay A	Medium	Forward
	Relay B	Unknown	No trip and no records
Line to generator 3	Relay A	Medium	Forward
	Relay B	Unknown	No trip and no records

Table 1. Distance operation depending on the memory duration

Another observation from the Table is that lines to generators 2 and 3 were tripped, even though distance relays were on the medium duration voltage. As stated above, lines to generator were importing power, while lines to other substations were exporting power. Also, lines to other substations tripped 1 ¼ cycle after bus fault was cleared, while lines to generator were tripped in 2 ¼ cycles after bus fault was cleared.

A distance function needs a memory voltage to ensure the relay has sufficient voltage to determine whether close-in faults are internal or external when the actual voltage becomes very low, and not measurable. Different polarizing quantities can be used, but most common is positive-sequence voltage, because angle of the pre-fault and fault positive-sequence voltage will not change much in at least initial 5-10 cycles into the fault, when distance zone 1 must operate. Another benefit of memorizing pre-fault voltage is the expansion of the MHO characteristics, which helps detect resistive faults [2], [3].

On the other hand, memorized pre-fault voltage V_{1MEM} cannot be used too long, because system voltage can start shifting during prolonged disturbance or during power swing. This calls for adaptive memory voltage approach, when duration of the memory voltage can be controlled by some factors or settings. Some approaches involve a combination of memory voltage V_{1MEM} and actual voltage V_{1ACT} , gradually decreasing the amount of memory voltage and increasing the amount of actual voltage to form polarizing quantity over a few power cycles, $V_{POL} = n \cdot V_{MEM} + (1 - n) \cdot V_{ACT}$, where n denotes variable percentage from 100% to 0% within defined transition time. Varying n upon pre-defined conditions, either short or medium adaptive memory voltage duration can be achieved. For example, short memory can ensure that in 1 cycle relay is switched to completely using actual V_1 voltage for polarization, but with medium length memory voltage will switch to actual V_1 voltage in 16 cycles or longer. Before this relay will be using weighted mix of actual V_1 and pre-fault memory voltage, gradually increasing weight of the actual voltage.

A different approach is to keep pre-fault memorized voltage for the user defined time and switch to the actual voltage V_{1ACT} only if actual V_{1ACT} voltage is sufficient, for example above 10% of the nominal [4]. Duration of the distance memory voltage is controllable by the settings in the distance relays and Table above is highlighting different response of the distance relays based on the set memory duration at this substation.

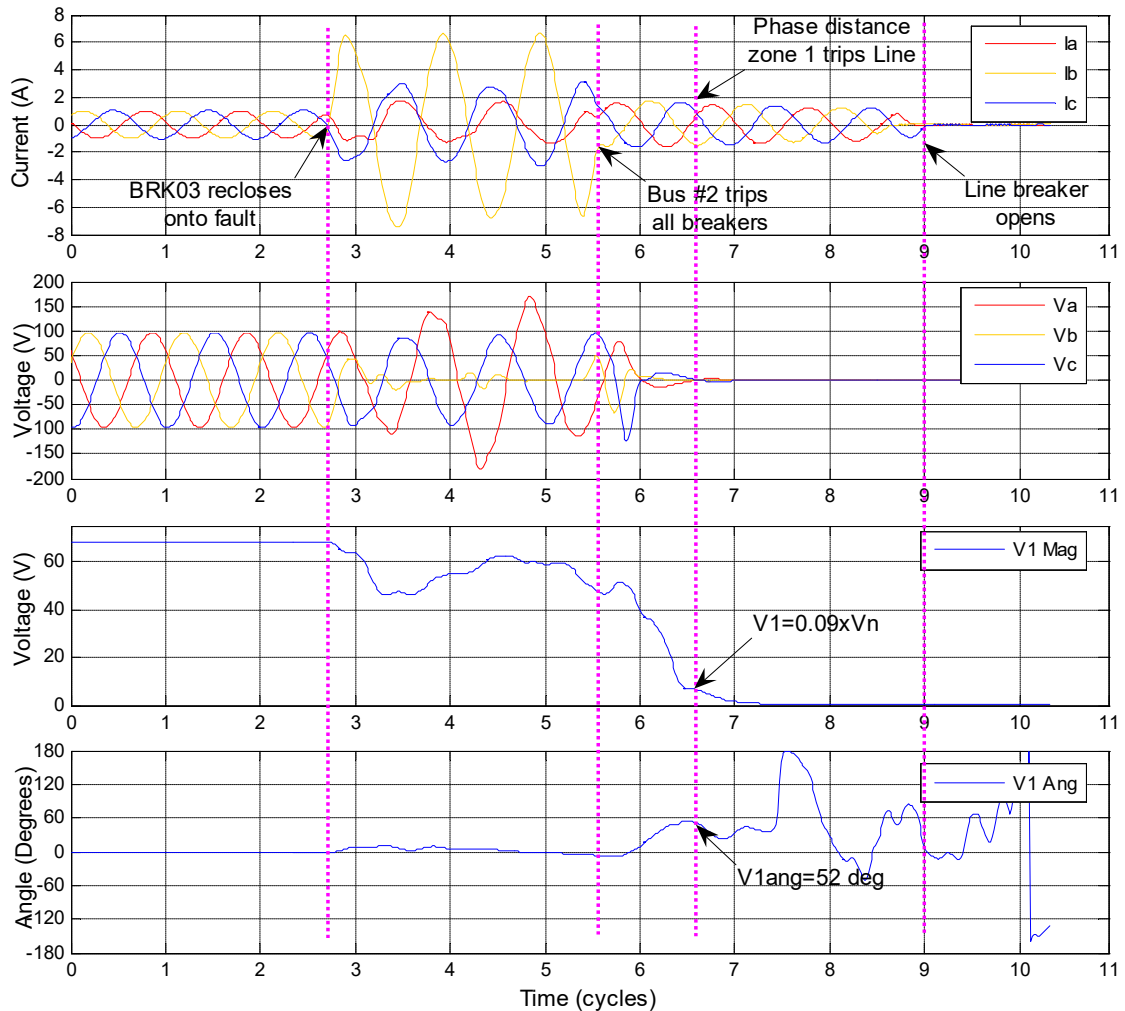


Figure 8. Line to substation D secondary currents, voltages and V1 voltage

Figure 8 above captures waveforms in secondary volts and amps from the unfaulted line to the substation D, tripped by the phase distance zone 1 during this event. It also captures positive sequence voltage magnitude and angle, which help to understand relay operation. We can notice from the 2nd plot that voltages experienced significant transients during fault, where phase A voltage experienced significant distortion and transient overvoltage, reaching 179.1V peak secondary, which is 190% of the nominal. Post-event investigation pointed to the phase A CVT failure, which was confirmed by comparing this CVT phase voltage with other phase A connected single-phase CVTs used for synchronism check. These transients during fault and fault clearance may cause positive sequence voltage to be unpredictable and unreliable—we can see from the 4th plot how angle of positive sequence voltage was changing within 1-2 cycles after Bus 2 protection tripped all breakers.

There were 3 major questions to be answered:

- Is phase distance zone 1 tripping for unfaulted lines during loss of potentials and exporting power flow justified?
- Why line relays operated differently on the loss of potentials, where one relay operated phase distance forward zone 1, while another relay operated reverse phase distance zone?
- What can be done to mitigate risk of losing so many lines again in the future?

In the Table 2 below, secondary values for the line to substation D are captured for the 3 stages: a) pre-fault, b) during line-to-ground fault which is reverse fault for this relay, c) 1 ¼ cycles after bus protection opened all Bus 2 breakers. Prior to the fault this line was carrying power $S=242.4-j107.5$ MVA, meaning it was exporting 242.4 MW and was importing 107.5 MVAR.

	Stage a: Pre-fault		Stage b: Line BG fault		Stage c: 1 ¼ cycle after bus trip	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
IA	0.70 A	23.4°	1.17 A	122.0°	1.13 A	25.5°
IB	0.71 A	-101.3°	5.30 A	-33.2°	1.23 A	-100.7°
IC	0.74 A	144.1°	2.20 A	140.5°	1.15 A	144.1°
VA	68.27 V	-1.71°	94.27 V	23.7°	0.71 V	-166.6°
VB	68.53 V	-121.9°	3.43 V	-49.0°	2.52 V	-58.9°
VC	68.52 V	118.1°	63.50 V	114.6°	3.22 V	155.5°
V1	68.41 V	-1.9°	1.17 A	122.0°	1.67 V	51.1°

Table 2. Secondary phasors for line to substation D during pre-fault, line-to-ground BG fault and 1 ¼ cycle after bus trip

We can see that during stage (c) when zone 1 operated, phase voltages were decaying and were very low. Positive-sequence voltage was also very low with an angle shifting dramatically by 53° compared with a pre-fault angle, which caused the distance operation as will be explained below.

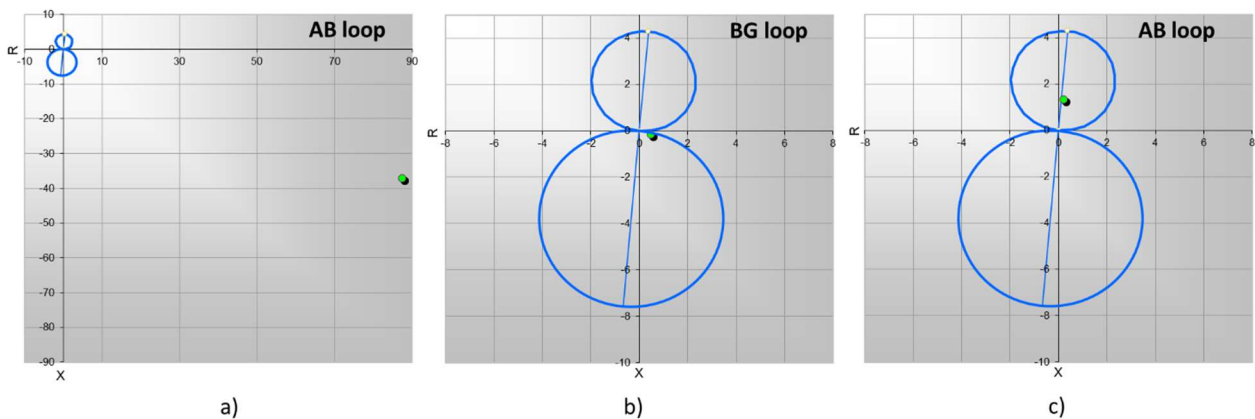


Figure 9. Apparent impedance for line to substation D: (a) pre-fault, (b) reverse BG fault, (c) 1 ¼ cycle after bus fault cleared

R-X plots above in Figure 9 are showing apparent impedance (green dot) seen by the line D relays for these 3 stages. Forward zone 1 with a 4.3Ω reach and reverse zone with a 7.6Ω reach are shown for illustration purposes. We can see that during pre-fault stage impedance locus is in the IV-th quadrant in

plot (a), matching power flow for the characteristics. If potentials were not lost, after bus protection operation we would expect apparent locus will be somewhere close to this point in the R-X diagram. During the reverse BG fault shown in plot (b), when breaker BKR03 closed onto fault, apparent impedance appears in the reverse direction in the IV-th quadrant and reverse distance zone is picking up as expected by both A and B relays. In plot (c) apparent impedance is getting into forward phase distance zone 1 characteristics in 1 ¼ cycles, which appears to justify relay A operation because it was not blocked by the LOP, as explained earlier. However, relay B at the same line with the same distance settings did not operate for the same condition.

We'll now explain this operation and illustrate the importance of the memory voltage for the correct operation of the distance function. We all know that classic MHO function is comparing angles of the following quantities for phase distance AB loop, as an example:

$$\underbrace{(I_A - I_B) \times Z - (V_A - V_B)}_{\text{Operating quantity, OQ}} \text{ and } \underbrace{(V_A - V_B)_{POL}}_{\text{Polarizing quantity, PQ}} \quad \text{Eq. 1}$$

where $(V_A - V_B)$ stands for the actual voltage and $(V_A - V_B)_{POL}$ for the polarizing voltage, which can be memory voltage, actual voltage or combination of two as explained above. When the angle between operating and polarizing quantity is less than 90° , it's an indication that locus is inside MHO characteristics and element operates. When the angle is above 90° , the locus is outside characteristics.

However, as mentioned above, relays are using positive-sequence voltage polarization, which means $(V_A - V_B)_{POL}$ voltage is V1 voltage shifted by the 30° leading for the AB loop.

$$(V_A - V_B)_{POL} = V1 \cdot e^{j30^\circ} \quad \text{Eq. 2}$$

Using these equations with the voltage and current values shown in the Table 2 during this event, we will explain the difference in relays response. First, we analyze relay stage "c" response using 100% memory voltage, meaning V1 voltage taken prior to the fault at stage "a".

$$\begin{aligned} OQ &= (1.13A \cdot e^{j25.5^\circ} - 1.23A \cdot e^{-j100.7^\circ}) \cdot 4.3\Omega \cdot e^{j85^\circ} - (0.71V \cdot e^{-j166.6^\circ} - 2.52V \cdot e^{-j58.9^\circ}) = \\ &= 6.24V \cdot e^{j140.3^\circ} \end{aligned} \quad \text{Eq. 3}$$

$$PQ = 68.41V \cdot e^{-j1.9^\circ} \cdot e^{j30^\circ} = 68.41V \cdot e^{j28.1^\circ}$$

Comparator difference with memory voltage is:

$$Diff_{MEM} = |\arg(OQ) - \arg(PQ)| = |140.3^\circ - 28.1^\circ| = 112.2^\circ > 90^\circ \quad \text{[no trip]} \quad \text{Eq. 4}$$

Comparator difference with actual voltage is:

$$Diff_{ACT} = |\arg(OQ) - \arg(PQ)| = |140.3^\circ - (51.1^\circ + 30^\circ)| = 59.2^\circ < 90^\circ \quad \text{[trip]}$$

To confirm the analysis above, the memory duration was changed on Relay B protecting the line to substation D. During the event, this relay didn't operate on the zone 1 because its memory was set to a long duration. The memory in this relay was changed to a short duration and the event waveform was played back into the relay. The result was that zone 1 in Relay B then operated exactly same way that Relay A had during the event.

With regards to the lines to generators 2 and 3 tripping, distance relays were on the medium duration memory voltage and operated 2 ¼ cycles after bus #2 trip. Line to generator 2, for example, was carrying power $S=-360+j150$ MVA, meaning it was importing 360 MW and was exporting 150 MVAR.

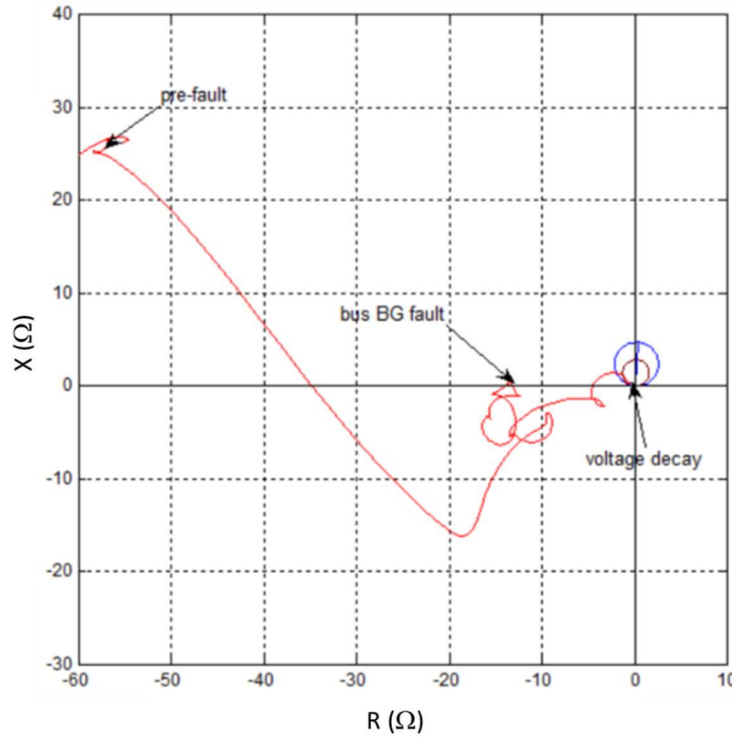


Figure 10. Line to Generator 2 phase distance AB loop trajectory

Medium duration ensures polarizing voltage is filtered such as pre-fault voltage is having higher weight compared with an actual voltage providing smooth transition. With a medium duration memory voltage, polarizing voltage didn't experience a shift of 53° as happened with a short memory voltage. So, why did these distance relays on the generator lines with medium duration memory voltage operate? Figure 10 above demonstrates the trajectory of the phase distance AB loop for the line to generator 2 for the 3 stages: load prior to the fault, BG fault resulting in the bus #2 trip and finally when voltage decayed due to VT signal loss. In the final stage, the apparent impedance enters the phase distance zone 1 characteristics. To prove that phase distance zone 1 had a valid condition to operate, we'll look at comparators again at the moment of operation.

$$OQ = (1.24A \cdot e^{-j155^\circ} - 1.34A \cdot e^{j83.9^\circ}) \cdot 2.83\Omega \cdot e^{j85^\circ} - (0.06V \cdot e^{-j103.9^\circ} - 0.04V \cdot e^{j137.2^\circ}) =$$

$$= 6.29V \cdot e^{-j38.8^\circ} \quad \text{Eq. 5}$$

$$PQ = 68.41V \cdot e^{-j1.9^\circ} \cdot e^{j30^\circ} = 68.41V \cdot e^{j28.1^\circ}$$

Comparator difference with memory voltage is:

$$Diff_{MEM} = |arg(OQ) - arg(PQ)| = |-38.8^\circ - 28.1^\circ| = 66.9^\circ < 90^\circ \quad [\text{trip}] \quad \text{Eq. 6}$$

The conclusion is that even if we maintain proper memory voltage, the phase distance still can operate on the importing power when voltages are going down and LOP fails to block phase distance.

Of course, the event we are describing is exceptional and normally it should not happen that multiple relays are losing potentials while LOP is inhibited and distance consequently is not blocked. However, are we paying attention to the memory voltage settings? Figure 11 below illustrates the concept of the dynamic expansion of the MHO [3]. Expansion is achieved because relays are using healthy pre-fault voltage E . The amount of the dynamic expansion is defined by the source impedance Z_s , which means expansion will be larger with a weak source and will be smaller with a strong source. For a very weak source, expansion may be so large that it endangers security of the zone 1 during out of zone fault. Therefore, using memory voltage too long in a very weak system may not be a good idea.

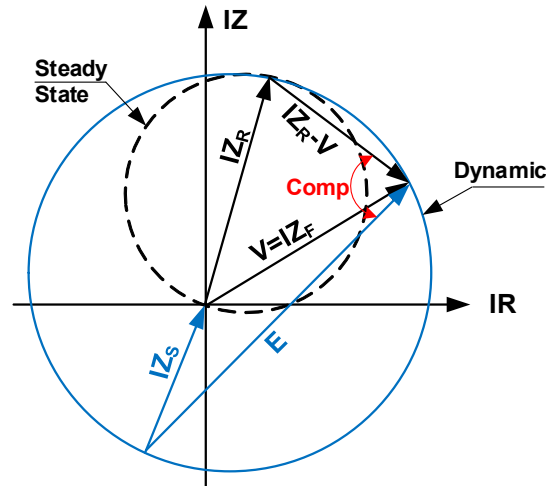


Figure 11. Dynamic expansion of the MHO, forward fault

On the other hand, voltage transients during fault are causing errors in phasors magnitudes and angles estimation. Figure 12 below depicts voltage transients during the fault and errors in positive sequence voltage angle and VAB angle, which both can be used as a polarizing quantity. If polarizing quantity is switched from the pre-fault to the actual voltage, making distance function self-polarized, the accuracy and security can be jeopardized. It can be observed that VAB angle is experiencing shift up to 50° even before fault is cleared, while V1 angle is experiencing errors as well. This is also due to the failure of the phase A CVT. During fault clearance, switching-off transients are becoming even more prominent, further jeopardizing distance function security.

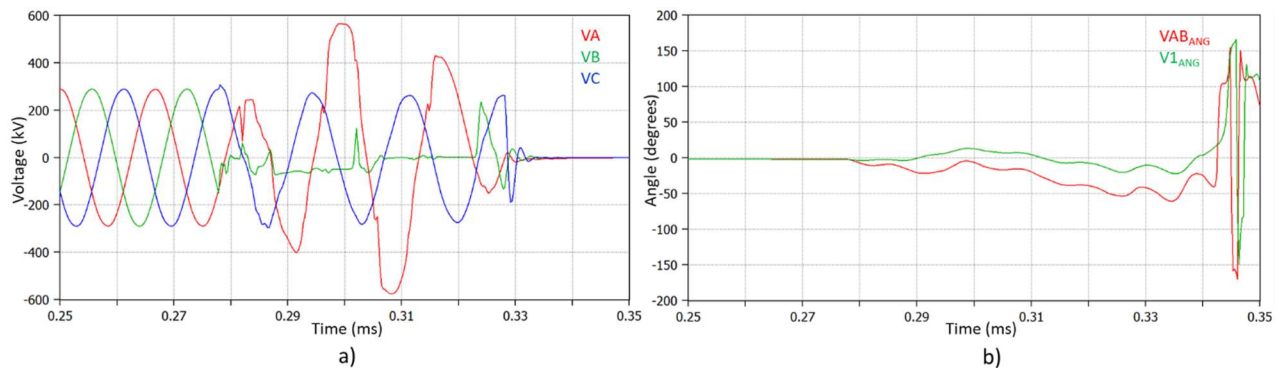


Figure 12. Voltage transients (a), errors in voltage angles during fault transients (b)

Considerations for the V1 memory voltage duration are as follows:

- V1 memory duration should be long enough to ensure close-in fault clearance and to avoid errors during fault or switch-off transients.
- V1 memory duration should not be too long since voltage can start shifting after fault clearance.
- If V1 voltage is too low after memory timer expires, continue using memory voltage because the actual voltage may not be a reliable source for polarization.
- For applications on series-compensated lines, consider longer memory duration.
- During power swings or off-nominal system frequency conditions, switch to actual voltage immediately to ensure self-polarization to avoid misoperation.
- For weak source applications, consider shorter memory voltage since the MHO element can expand too much. For medium or strong system applications, consider medium duration as the MHO element will not expand very much, but voltage transients can be more severe [5].

VI. Lessons learned and corrective actions

There were several lessons learned from this event.

1. It is important to consider remanence when studying CT saturation.

This event describes a CT that is sized so there is no CT saturation during the first fault. However, during a reclose attempt, the remanence was enough to push the CT into saturation. Even mild CT saturation, which occurred during this event, can cause high bus differential current. Also, this event shows that the high set current differential element is very susceptible to CT saturation. Remanence value of 0.7-0.8 can be used during the CT saturation study. If the high set element is used, it should be set well above the worst-case CT saturation (taking high differential current due to remanence into account). One corrective action taken as a result of this event was to disable the high set current differential element for Bus 1 and Bus 2. Only the percent differential element will be used to provide full bus protection from now on.

2. There is a high risk when operating with a potential paralleling scheme lockout rolled.

Another lesson learned from this event is the high risk involved with operating the potential paralleling scheme in the abnormal configuration of only one bus VT feeding all the distance relays. Normally, the potential paralleling scheme has a VT on each bus feeding the distance relays in parallel. In this normal configuration, the distance relays will still receive a good potential measurement even if one bus is lost. However, when operating in the abnormal configuration of only one bus VT feeding all the distance relays, the distance relays will completely lose their potential measurement if that bus is lost. This has a significant impact on many distance relays at the same time.

3. LOP may fail to operate and block distance elements if potentials are lost during or immediately after a fault.

For the event described in this paper, the distance relays lost their potential measurement when a bus locked out due to a fault. This paper explained that the conventional LOP logic is disabled for some time after a fault is detected. Therefore, the conventional LOP logic will not assert in the case described. This

severely compromises the protection capability of the distance relays since they will have no potential measurement and they do not assert LOP. This contingency must be considered and addressed.

Strong consideration should be given to setting phase distance overcurrent supervision above the maximum line load. This is especially true when there is a strong source behind the relay and will ensure that LOP failure will not cause the same outcome as described in this paper.

4. Memory voltage duration can have a significant impact on distance relay operation.

Another lesson learned during this event is how a distance relay will respond when there is a fault followed by a complete loss of potential, with no assertion of the conventional LOP. In this situation, the distance relay is relying on memory voltage to calculate an impedance. Depending on the memory voltage design and settings in the relay, the relay may declare a forward fault or a reverse fault. This paper explains how the relay will make this declaration. The distance relays may or may not trip, but either way this is not a good operating condition. Attention must be paid to the memory voltage duration. However, memory voltage alone may not ensure non-operation of the phase distance function during LOP conditions due to power flow as it happened on the lines to the generators during this event.

5. Changes were implemented to mitigate risks of potential paralleling schemes.

Due to the high risk involved with operating the potential paralleling scheme in the abnormal configuration of only one bus VT feeding all the distance relays, more focus will be placed on resolving a lockout in the potential paralleling scheme. If a potential paralleling lockout asserts, the transmission operation group will promptly investigate the VT circuit associated with that lockout to identify any signs of damage. If no damage is found, the operations group will attempt to reset the lockout. If they are unable to reset the lockout, then the system protection engineering group will be contacted immediately to investigate the lockout. Once notified, the system protection engineering group will place a high priority on identifying and correcting the problems with the potential paralleling scheme. These steps are designed to return the potential paralleling scheme to its normal configuration as soon as possible.

In addition to the improved potential paralleling lockout response, a program to eliminate the risk of potential paralleling schemes in the long term has been initiated. Within this program, a project will be initiated at each substation with a potential paralleling scheme. During the project, three-phase VTs will be installed on each element that utilizes distance relays. Once these three-phase VTs are installed, the potential source for all distance relays will be changed from the potential paralleling scheme to their corresponding VT. Then, the entire potential paralleling scheme will be removed. Once this program is complete, there will be no potential paralleling schemes on the transmission system.

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VIII. Biographies

James D. Redinger received his Electrical Engineering degrees (BSEE and MSEE) from the University of Minnesota – Twin Cities. He has worked as a system protection engineer with Xcel Energy in Minneapolis, Minnesota for the last 4 years and continues to enjoy this role. He has been involved with investigating faults on the transmission system and corresponding protective relay operations as well as designing protection schemes for projects on the transmission and distribution system.

Ilia Voloh received his Electrical Engineering degree from Ivanovo State Power University, Russia. He is currently an applications engineering manager with GE Grid Solutions in Markham Ontario, Canada where he has been heavily involved in the development of UR-series and 8-series of relays. His areas of interest are current differential relaying, distance relaying, advanced algorithm and advanced communications for protective relaying. Ilia authored and co-authored more than 50 papers presented at major North America Protective Relaying conferences. He is a recipient of the best paper award at Georgia Institute and Technology Protective Relaying Conference in 2012. Ilia is a senior member of the IEEE, member of the IEEE PSRC main committee, a member of the IEC TC 95 committee and a member of the CIGRE B5.65 working group. He is a member of the WPRC Committee.