

Protection Issues and Solutions for Protecting Feeder with Distributed Generation

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1. Introduction

These days the distributed generation (DG) is developing fast because of the benefits it could bring into the system, such as the relief of transmission and distribution burden and usage of the clean energy. However, at the same time, DGs are also bringing some challenges to well-known traditional protections in distribution systems, especially with high penetration level of DGs. One of them is during a fault where DG could contribute to the fault current in addition to the contribution from the existing power grid.

IEEE 1547 Standard for Interconnecting Distributed Resources with Electric Power Systems defines technical requirements for integrating distributed sources. In addition to IEEE 1547 Standard utilities are defining their own requirements for interconnecting a distributed generating source to its distribution system as well. However, standard does not recognize the impact of the distributed generation penetration on the traditional protection performance and is not giving recommendations on how to take this into account when choosing protection scheme.

This paper will first give an overview of the distributed generators behavior and their current contribution during the fault. Special focus will be given to inverter interfaced DG (IIDG) which has fault behavior significantly different from that of a conventional DG while having not been adequately studied. It will examine the key features of IIDGs' fault behavior with respect to interference with distribution protection. As an example, current and voltage waveforms from a commercially available photovoltaic converter will be shown through a hardware-in-the-loop (HIL) simulation setup using real-time digital simulator (RTDS). Then impact and complications of such fault behavior of DG on the traditional feeder overcurrent protection performance will be analyzed as well.

Finally, possible application solutions are presented and analyzed for the feeder protection with a considerable penetration of DGs. This includes usage of directional comparison and distance protection and partial differential protection.

2. Impact of Distributed Generation on Feeder Protection

2.1 General Impact and Common Problems

Conventional power distribution system is radial in nature, characterized by a single source feeding a network of downstream feeders. Protection scheme for distribution system consists of fuses, reclosers and overcurrent relays and they have been designed assuming the fault current is with single direction, from the single source to the fault location.

With rapid expansion and commercialization of DGs, distribution system would look something like the one shown in the figure. DGs might be interconnected at substation, distribution feeder or

customer load level. In such a system, a couple of challenges would arise in terms of feeder protection:

- Bi-directional fault current:** multiple sources could contribute to the fault current which makes the fault current bi-directional. Therefore, traditional relays that are insensitive to direction might become unacceptable.
- Reduced/increased fault current seen by relays:** with DGs connected, previously coordinated relays in the system may see increased or decreased fault current. Relay coordination may be upset.
- Changing fault current levels:** most of DGs, like photovoltaic (PV) or wind turbines, are intermittent sources. Connection status of DGs is highly variable. Fault current levels may constantly change accordingly. Conventional protection, which can only work with fixed settings, may be difficult to properly coordinate, if not impossible.

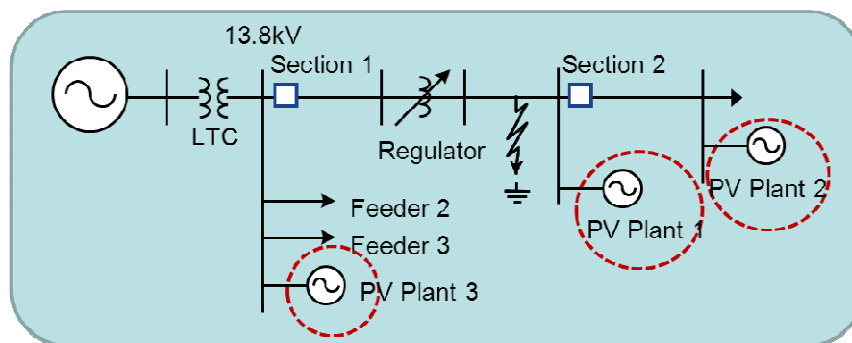


Figure 1: Potential distribution protection problems with DG

Some commonly discussed problems are summarized in Figure 2 [1]-[6].

Figure 2 (A) is showing blinding of protection. When DG is connected downstream of the main feeder protection and a fault occurs at the far end of the feeder, fault current contribution from DG may reduce the fault current the feeder protection experiences and blind or delay its operation.

Figure 2 (B) shows a fault on one feeder could possibly trip the relay on another feeder if no direction element is built in that relay.

Figure 2 (C) illustrates how DG may disturb fuse saving scheme. A fuse saving scheme usually includes a circuit breaker or a recloser on the main feeder and a fuse on tapped laterals. For a fault on one lateral, the recloser operates on its fast trip curve, before the lateral fuse, thus saving the fuse from blowing. When the recloser recloses, it is set on its slow trip curve. If a permanent fault is present, the lateral fuse will blow prior to recloser pickup after reclosing. Without DG connection, the recloser and the fuse in Figure 2 (C) always see the same fault current and they can follow the fuse saving logic very well. But with the interconnection of DG, the recloser now sees less current than the fuse does. This current discrepancy may make the fuse operate faster than the recloser thus breaks the recloser-fuse coordination.

Figure 2 (D) is about miscoordination of previously coordinated relays. For time over current (TOC) relays, they are coordinated up to a certain current level. The connection of DG at substation may increase the maximum fault current that both relays R1 and R2 in Figure 2 (D) may experience, which may push them out of the current coordination range.

Figure 2 (E) shows conflicting requirements on relay coordination. During fault f1, with DG connected, fuse 2 should clear before fuse 3; while during fault f2, fuse 3 should clear before fuse 2. For each fault, both fuses see the same fault current. Therefore, two fuses are facing conflicting requirements on coordination with DG.

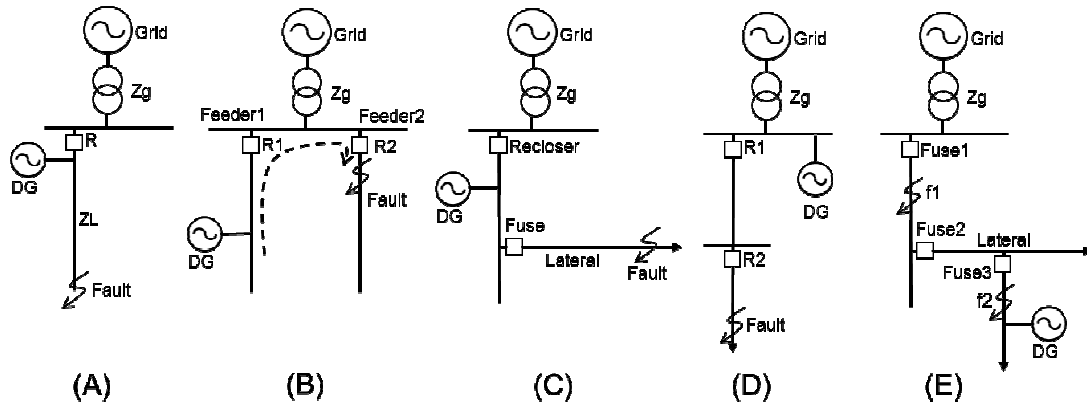


Figure 2: Potential distribution protection problems with DG

2.2 Islanded or Grid Connected Modes

Besides general problems we just discussed, microgrids have some specific protection problems with DG integrated.

Most microgrids can operate with both grid connection mode and islanding operation mode. These two modes can be with different fault portfolios since short circuit capacity of the grid and the DG can be significantly different. The protection in microgrids has to work for both operation modes.

Another protection challenge for microgrid protection is that during islanding operation mode, if most DG is IIDG with well-regulated fault current output close to rated current, there is not sufficient fault current to trip the relay.

2.3 Factors Affecting the Impact of DGs

As mentioned in previous sections, during a fault DG could contribute to the fault current in addition to the contribution of the existing grid, it will pose a challenge to the protection of the feeder it is connected. As for the amount of fault current contribution, its duration and whether or not it causes a feeder protection problem, it depends on the factors listed below [5]:

- a. **Features of DG:** Type of DG (conventional generator or IIDG) and its impedance, control and protection of DG, DG grounding and interface transformer
- b. **Integration of DG:** Locations of DG on the feeder and penetration level

- c. **System being integrated to:** Configuration and impedance of feeder, the existing protection of feeder

In the following sections, we will examine in details the impact in terms of different factors.

2.3.1 Conventional Generator versus Inverter Interfaced Generator

Many DGs, such as most wind turbines and micro turbines, and all photovoltaics, interface with power systems through inverters [7]. While many publications discuss the general impact of DG on protection [1]-[6], only a few of them differentiate inverter interfaced distributed generator (IIDG) from other types in terms of fault behavior [4]-[6]. Fault behavior of conventional generators, like synchronous generators and induction generators, is well known. Sub-transient and transient impedance and time constant will dominate the fault behavior. A voltage source behind a certain reactance is usually used to represent a conventional generator during the fault condition. As for IIDG, the fault behavior is highly determined by the converter control and protection, which is designed and implemented by manufacturers both to protect their equipment and to follow the industry standards. Interestingly, this fault behavior dependence on control is not widely discussed, although the IIDG fault current contribution is substantially different from that of the conventional generators.

To give a quick glance of the difference of fault behavior, the terminal voltage and output current of synchronous generator and IIDG with a remote 3-phase fault are illustrated in Figure 3. Detailed simulation setting to generate these waveforms will be discussed in later sections. But generally simulation parameters are set to provide an apple to apple comparison (with the same DG MVA level, same location in the same system and the same fault).

We can observe that after the fault occurs at 0.05 sec the synchronous DG generated much higher thermal fuse duty (I^2t) than the IIDG, which is the most important factor of fuse operation time. Also, the synchronous DG outputs rather high sub-transient and transient current before decaying to its steady state value while the IIDG settles down almost instantly. When the thermal energy is calculated up to ten cycles after the fault, the energy from the synchronous DG is about four times of that from the IIDG.

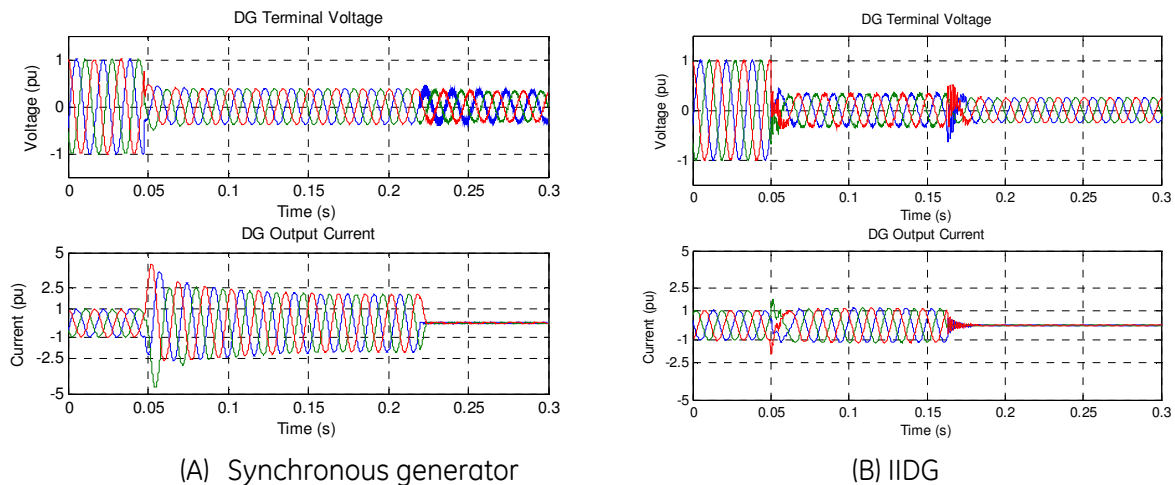


Figure 3: Terminal voltage and output current of DG with a remote 3-phase fault

In the following sections, we will examine in detail the key features of IIDGs' fault behavior with respect to interference with distribution protection. A case study will be performed to investigate the impact of IIDG on the recloser - fuse coordination in the fuse saving mode.

2.3.2 Fault Behavior of IIDG [6]

As a power electronics-based converter, the fault behavior of an IIDG is largely determined by its control. Essentially, the individual designer has his own preferences on how to operate the IIDG under fault circumstances and then design the control to behave in certain ways. Therefore, it is neither practical nor possible to come up with one or several generalized IIDG model(s) and use them to accurately predict the fault behavior. In [4], the authors categorized IIDG into two different types based on their control schemes (one is voltage control scheme and the other is current control scheme), and then represented the dynamics of voltage controlled IIDG as a linear PI (proportional and integral) transfer function. In reality, this approach is considered as over-simplified since many non-linearities are always incorporated in both the control system and hardware protection of all IIDGs. Such nonlinearities, including hardware current limiting functions on gate-drive boards, certain control functions hitting their limits, state machine changing its state, and etc, play a major role in the transient behavior. Unless these nonlinearities are adequately modeled, such a fault analysis will be inaccurate and often misleading.

This being said, one may still be able to obtain a rough idea of the fault behavior of an IIDG and estimate its impact on system protection given the specific application requirements. This is because no matter what the detailed control design is, there are always certain hard boundaries that constrain all IIDG designs, which include the overload limitations of IGBT devices and certain standards pertaining to grid integration requirements.

In this section, we will discuss the different aspects of an IIDG's fault current and how they are affected by various considerations.

2.3.2.1 Voltage vs. Current Control Scheme

Before we start the fault current discussion, it is necessary to first give a brief introduction to two control schemes that can be used for IIDGs. One is a voltage control scheme, and the other is a current control scheme. Figure 4 illustrates the simplified block diagrams of these two schemes. Typically, both schemes regulate real and reactive power. The P/Q regulator(s) could be a multi-variable optimal controller or two decoupled PI controllers. The P regulator may sometimes be replaced by a DC link voltage regulator.

What really determines if an IIDG is running on a voltage control scheme or a current control scheme is the implementation of its inner loop. For the voltage control scheme, it directly regulates voltage magnitude through either open or close loop control. Therefore we call it voltage control. For the current control scheme, it has a fast current control loop to regulate the current directly and so it is called current control. Knowing the type of control scheme is important for us to understand the fault behavior of an IIDG.

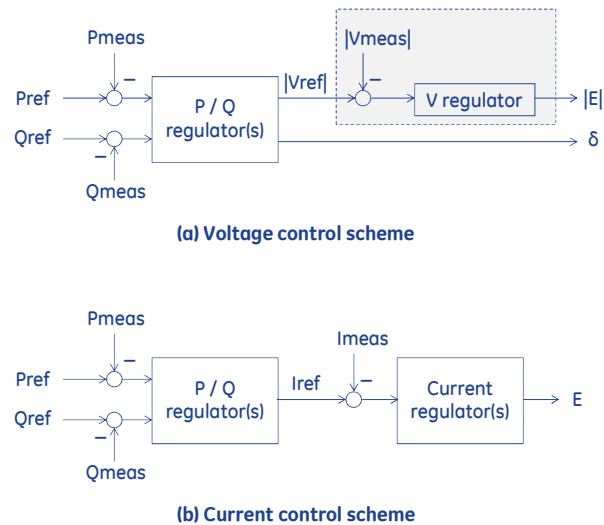


Figure 4: Illustrative block diagram of voltage and current control schemes for IIDG

2.3.2.2 Fault Current RMS Profile

Unlike rotating electric machines, power electronics-based IIDGs often have rather limited overload capability. One may find that some commercial IIDGs allow 10% to 30% overloading for a short period of time (e.g., one to several seconds), but seldom more than that. To protect those semiconductor switching devices (e.g., IGBT, IGCT) from thermal breakdown, an IIDG often has at least two layers of overcurrent protection. During a fault if the IIDG's output current becomes very high (e.g., peak value exceeds a threshold that is typically around 2~3pu), the hardware overcurrent protection on the gate drive board will stop firing temporarily and clamp the instantaneous current to that threshold. It is expected this period is short, and within several cycles the control-based protection is able to effectively reduce the RMS current to a lower level (1.0~1.2pu). In an IIDG with current control scheme, this control-based protection is simply realized by its inner current control loop. If the fault lasts for more than several seconds, a trip could be issued to disconnect the IIDG unless other protection functions trip first. For ease of our discussion later, we use transient and steady-state to describe the two fault durations said above. Figure 5 below illustrates the magnitude envelop of fault current through the two durations.

In Figure 5, the transient current magnitude, A_1 , is determined by the impedance between the IIDG and the fault location, and the fault severity. The smaller the impedance (e.g., closer to the fault location) and/or the higher the fault severity (e.g., smaller fault impedance), the higher the transient current. However, even under the worst condition, A_1 will not exceed the threshold determined by the hardware over-current protection if that is in place.

The transient time duration, T_1 , depends on the bandwidth of the IIDG's control-based protection function (for current control scheme, it is the current control loop). In most cases, IIDGs with current control scheme reacts much faster (sometimes less than half a cycle) than those with voltage control scheme (several cycles) due to the high bandwidth of current control loop.

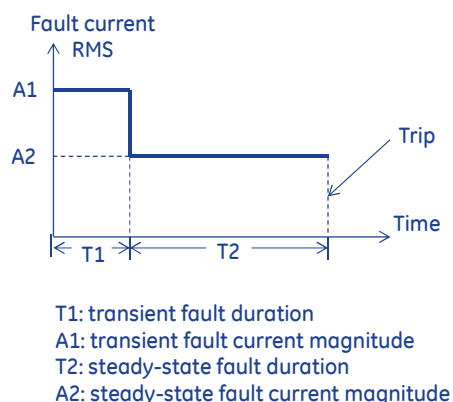


Figure 5: Magnitude envelop of an IIDG's fault current

The steady-state fault current, A2, is determined by the application requirement that a specific IIDG may be subject to during the fault event.

The steady-state fault duration, T2, ends when the IIDG trips or the fault is cleared. IEEE 1547 [8] gives the maximum tripping time for various fault voltage levels (Table 1). This could be a determining factor if the IIDG follows this standard. In the future, as the penetration level keeps increasing and islanding operation becomes a possible option, fault-ride-through capability may be required. In such a circumstance, T2 may continue until the fault is cleared or isolated, or the maximum fault duration is reached, whichever happens first. Obviously T2 is critical to determine in terms of the time frame whether the IIDG will impact the operation of distribution protection.

Table 1: Interconnection system response to abnormal voltage

Voltage range (% of base voltage) ^a	Clearing time (s) ^b
$V < 50$	0.16
$50 \leq V < 88$	2.00
$110 < V < 120$	1.00
$V \geq 120$	0.16

^a Base voltages are the nominal system voltages stated in ANSI C84.1-1995, Table 1

^b DR \leq 30 kW, maximum clearing times; DR > 30 kW, default clearing times

2.3.2.3 Fault Current Composition

For the purpose of system protection study, the fault current composition (i.e., real and reactive current components) is another important aspect to be considered. For example, one per-unit reactive current impacts much more than one per-unit real current if the grid's fault current contribution is mainly reactive.

Again, the specific application requirement on the IIDG plays an important role in determining this aspect. For example, IEEE 1547 requires that DG shall not actively regulate the voltage. The steady-state fault current may contain very little reactive current if unity power factor is commanded. In the transient duration, a higher reactive current may be observed either because the sudden grid voltage drop is not picked up by the measurement or because the PLL (phase lock loop) takes some time to capture the phase jump caused by the fault. In contrast, if an IIDG is required to provide voltage regulation, such as transmission interconnected wind turbines designed to follow the E.ON

grid code [9], then a significant level of reactive current will be expected depending on the voltage level.

2.3.2.4 Sequence Current

In practice, most faults in power systems are unbalanced. Therefore, the sequence current generated by an IIDG is also an important aspect of its fault behavior.

There are two factors that will affect the sequence current during an unbalanced fault. One is the negative sequence behavior of the IIDG. Some designs use certain control logic to generate a large equivalent negative sequence impedance in the IIDG in order to lower the negative sequence current. If this is the case, the positive sequence and negative sequence circuits of the IIDG in the fault analysis have to be treated separately. Another factor is the grounding type of IIDG. A good discussion of this topic can be found in [7] (pp. 699-750) where the interfacing transformer configuration and the IIDG neutral connection together determine if the IIDG is a grounded source or not. A grounded IIDG decreases the feeder ground-relay sensitivity to a single-line-to-ground fault current due to the zero-sequence path.

2.4 Example of the Impact on the Fuse Saving Scheme

2.4.1 Case Study – Test Setup

2.4.1.1 The Protection Scheme of Fuse Saving

The case study presented in this paper examines the impact of a DG on a fuse saving scheme when it is connected immediately downstream of a recloser, as shown in Figure 6. One reason to choose this particular problem to study is that the fuse saving scheme is commonly applied in distribution feeder protection (in 2000, 66% of the U.S. utilities use fuse saving [7]). Another reason is that the DG terminal voltage in this case maintains a relatively high value during the fault due to the long distance (high impedance) from its location to the fault. Hence the DG would stay in the system for a longer time before tripping which enables its interaction with feeder protection.

A fuse saving scheme usually includes a circuit breaker or a recloser on the main feeder and a fuse on tapped laterals. For a fault on one lateral, the recloser operates on its fast trip curve, before the lateral fuse, thus saving the fuse from blowing. When the recloser recloses, it is set on its slow trip curve. If a permanent fault is present, the lateral fuse will blow prior to recloser pickup.

The notional scenario considered in the paper is: A distribution feeder with a lateral is protected by a recloser and a lateral fuse with fuse saving scheme, IIDG is then interconnected to the feeder downstream of the recloser. Due to the presence of the DG, the lateral fuse will see a larger fault current than the recloser does. In addition, the fuse will see a potentially longer-duration fault because the recloser operation does not remove all current from the fuse. The fuse will continue to see the current contribution from the DG until the DG trips. The higher the DG short circuit capacity and the slower the DG trip time, the larger discrepancy in current the two protection devices will see. When this discrepancy becomes large enough, the recloser-fuse coordination will be broken, and the fuse blows before the recloser can save it.

In this paper, such a current discrepancy is evaluated with different DG capacities. Then the recloser – fuse coordination is checked based on different recloser and fuse settings.

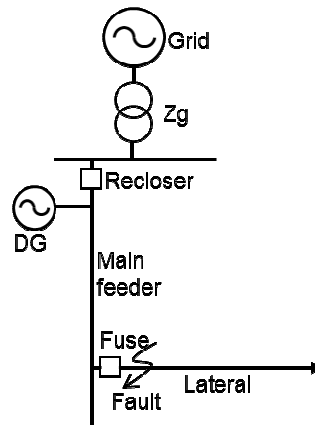


Figure 6: A case system with fuse saving protection scheme

2.4.1.2 Hardware-in-the-loop (HIL) Setup with Commercially Available Solar Controller

In our case study, a solar generator, which dominates the DG application, is taken as an example to show the impact of IIDG. The entire system shown in Figure 6 is simulated in RTDS with the IIDG modeled as a two-stage three-phase converter and a simplified PV panel. A commercially available solar controller is externally connected to the simulator to control the operation of the simulated converter. The control implementation of the controller is of current control scheme.

The system parameters taking the values generally from IEEE 34 node system [10], are listed in Table 2.

Table 2: Case system parameter

Component	Parameter	Value
Source	Line-Line Voltage (RMS)	138 kV
	Resistance	0.001 Ω
	Reactance	0.377 Ω
Substation Transformer	Rating	2.5 MVA
	Leakage Inductance	0.08 p.u.
	Ratio	138 kV / 24.9 kV
Feeders (Main feeder and Lateral)	Resistance	1.35 Ω /Mile
	Reactance	1.35 Ω /Mile
	Distance from Lateral to Substation	10 Miles

2.4.1.3 Recloser – Fuse Coordination

With the continuous load current in the main feeder to be about 40A, a recloser with 50A continuous rating is chosen. The A and B curves of the recloser, as given by the manufacturer data sheet [11], identify the fast curve and the delayed curve of the recloser. As recommended by the manufacturer, the A curve is adjusted by multiplying the time by a factor of 1.25 to coordinate with downstream fuses.

As for the fuse, both K and T links can carry 150% of the nominal current rating indefinitely. Without the DG, the maximum fault current caused by a fault on the lateral is 388A. The K link 25A fuse is chosen to protect the lateral since it is large enough to carry the normal load current and could coordinate with the recloser up to 460A maximum current.

Of course larger fuses can be chosen too. It will be shown later that selecting larger fuses is actually a good way to mitigate the impact of the DG. But it should be noted that the coordination of the fuse with both the fast and the delayed curves of the recloser should always be held.

2.4.2 Case Study – Test Results

2.4.2.1 Fault Behavior of the Hardware Controller

Figure 3 (B) shows the terminal voltage and current profile of the DG due to a 3-phase fault located right after the lateral fuse. The lateral is 5 miles from the substation and the DG is connected close to the substation. The fault starts at 0.05 second. Immediately after the fault occurs, the DG current shows a high peak due to the sudden drop in the feeder voltage. A phase adjustment from PLL resynchronization can also be observed following that current peak. Within 2 cycles, the fast control loop settles down to the steady-state fault condition with 1.2 pu current output (based on current rating of the IIDG).

In this test case, the DG terminal voltage drops to about 43% of its rated voltage and the controller trips at 0.12 second after the fault. This tripping time satisfies the requirement of IEEE 1547 shown in Table 1. Similar tests are performed with different DG terminal voltages by changing the distance between the substation and the lateral. The results are summarized in Table 3. It is shown that with higher terminal voltage, DG stays in the system longer and contributes less reactive current.

With a continuous fault current contribution for 0.12s, this DG poses a definite concern regarding performance of the system protection within the similar time frame. Although other DG designs may trip faster, it is always worthwhile to check the DG's response time to such faults.

Table 3: DG fault behavior with different DG terminal voltages

Distance between Substation to Lateral	DG Terminal Voltage ⁽¹⁾	DG Output Current ⁽²⁾	DG Output Current Contribution (degrees that I lags behind V)	Trip Time (second)
1 Miles	0.14 pu	1.2 pu	102.5	0.12
5 Miles	0.43 pu	1.2 pu	66.0	0.12
10 Miles	0.61 pu	1.2 pu	51.8	1.8
15 Miles	0.72 pu	1.2 pu	42.1	1.8

2.4.2.2 Impact on Fuse Saving Scheme

Table 4 shows the current seen by the recloser and the fuse with DG interactions. As penetration level goes higher, the IIDG's impact increases while leading to larger current difference seen by the recloser and the fuse. Actually at 100% penetration level, and with a K-25A fuse to protect the lateral, the operation time of the recloser and the fuse is very close with less than 5 millisecond margin. With 150% penetration level, the fuse will blow before the recloser trips as shown in Figure 7. Although a larger fuse, for example K30 or K40 in our case, can maintain the coordination, this may not always be possible since the fuse still has to coordinate with the delayed curve of the recloser.

Table 4: Current seen by protection with DG

Penetration Level	$I_{fuse} - I_{rc}$	
	With IIDG (pu / percentage change) ⁽¹⁾	With Synchronous Generator (pu / percentage change) ⁽²⁾
50%	0.66 pu / 10.33%	0.85pu / 13.82%
100%	1.16 pu / 18.96%	1.42pu / 25.01%
150%	1.83 pu / 31.53%	2.29pu / 43.45%
200%	2.35 pu / 42.54%	2.97pu / 58.80%

Note: (1), (2): Current is measured in the reference of rated current of substation transformer

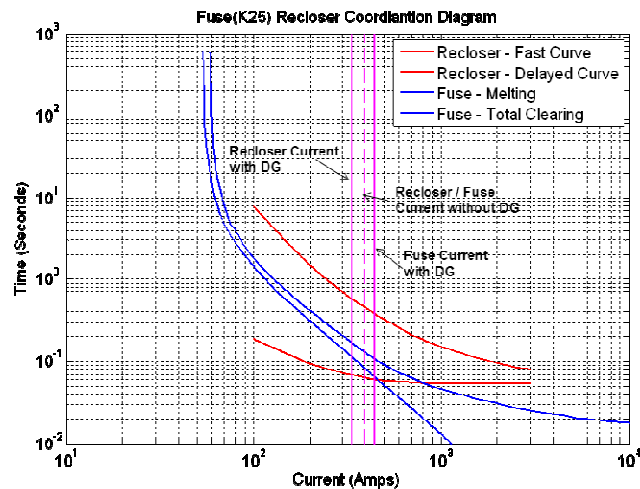


Figure 7: Fuse (K25) recloser coordination diagram with 150% penetration level

2.4.2.3 Comparison with Synchronous Generator

For comparison, a test with a synchronous generator type of DG is also performed. Different penetration levels are tested by keeping the same machine parameters (from [7]) shown in Table 5 while modifying the machine capacity from 1.25MVA (50% penetration level) to 5MVA (200% penetration level).

Table 5: Parameters of the synchronous generator

H	0.7 MWs/MVA	Xa	0.160 pu	Ra	0.013 pu
Xd	2.38 pu	Xd'	0.264 pu	Xd''	0.201 pu
Xq	1.10 pu	Xq'	0.376 pu	Xq''	0.35 pu
Tdo'	2.47 sec	Tdo''	0.018 sec		
Tqo'	0.3 sec	Tqo''	0.009 sec		

The test results with 100% penetration level are shown in Figure 3 (A). A 3-phase fault occurs at 0.05 sec and lasts 30 cycles. During the fault, after 1-2 cycles of sub-transient period, we see a transient current of about 1.5 to 2 times of the generator rated current. In this case, IEEE Type 1 exciter is included which increases the field voltage to about 1.3 times during the fault.

Table 4 summarizes the test results with IIDG and synchronous generator based on the steady-state fault current magnitude. It is illustrated that IIDG does not cause as large current difference as the

synchronous generator does. We also mentioned earlier that the synchronous DG generated much higher thermal fuse duty than an IIDG, which is the most important factor of fuse operation time.

3. Possible Protection Solutions

People are starting to look at this problem and currently some potential solutions are being discussed.

3.1 Adaptive Overcurrent Protection

One method is directional overcurrent relay with dynamic settings. This method needs fast and effective monitoring of system conditions. Basically it will automatically update relay settings based on prevailing system conditions [12].

Two types of adaptive protection exist. One is based on pre-calculated values and the other is based on real-time calculation [12]. Generally for the second type more information is needed to conduct real time calculation continuously of the actual fault current.

This method is with high complexity of implementation. For pre-calculated adaptive protection, it is hard to work for stressed system conditions not set or designed for.

3.2 Distance and Directional Comparison Protection

Distance protection is widely used at the transmission and sub-transmission level but was not traditionally applied at the distribution level. Even with obvious advantages of better and simpler downstream coordination, fixed reach zone and relative immunity to the source impedance behind the protection relay, it was not considered at the radial feeders. However, nowadays many utilities are applying this protection at the distribution level.

First of all, due to distributed generation penetration, the fault current becomes bi-directional, which brings directionality issues to protection scheme. As distance protection is inherently directional, it solves this problem. Secondly, distance is not affected by the changing fault current level due to changing source impedance compared with overcurrent protection. However, distance protection has its own challenges such as resistive fault coverage and variable apparent impedance seen by the relay due to the fault contribution from the distributed generators.

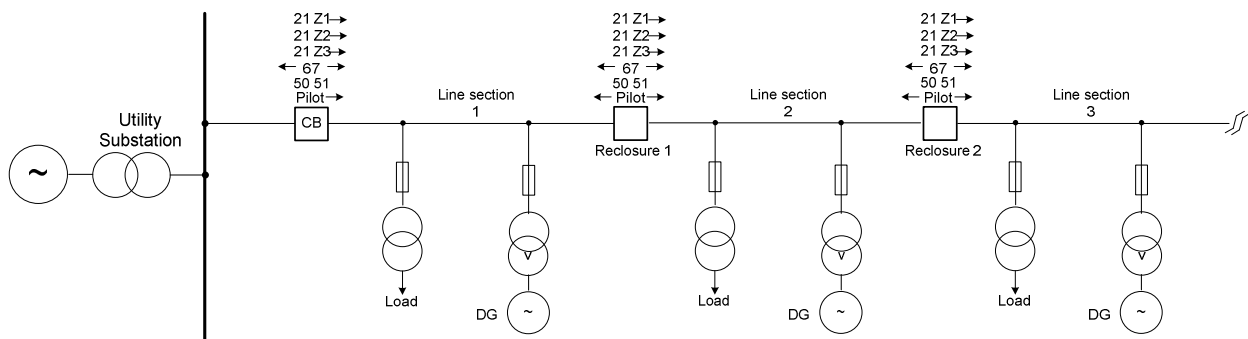


Figure 8: Distance and directional overcurrent with communications aids

Communications may play an important role in optimizing protection performance on feeders with distributed generation. Figure 8 above captures the concept of the protection scheme using distance, overcurrent directional and communications aids to achieve better performance. Directional comparison schemes are widely used at the transmission level with a good success and good understanding and experience by protection and control personnel. In the past pilot communications were not available at the distribution level which is changing these days. Wireless technologies including WiMAX and WiFi radios are penetrating into distribution system allowing take advantage of these communications infrastructures to deploy IEC 61850 concepts.

Protection scheme above is using pilot signals between sections of the feeder and also between substation, reclosers and distributed generators as well. Reclosers should not trip for reverse faults: this means when fault is detected on the particular section, one only switching apparatus which is closer to utility supply should open only. This can be achieved by sending pilot signal to upstream apparatus relay indicating that fault is in the reverse direction which is sensed by the distance (21) or directional overcurrent relay (67). Regular overcurrent protection (50/51) serves as a backup if there are problems with communications or voltage transformers needed for distance and directional operation.

3.3 Means to Reduce Impact of DGs

With DG integrated in distribution systems, extra fault current contribution from DG may cause the fault current in the system higher than the fault current design limit and present a risk of damage to and failure of the equipment. Fault current limiters are proposed to be used in this application to limit the fault current level below the design limit of the various grid equipment [13].

There is also some thinking of disconnecting all DG during the fault to maintain coordination. However, throwing off all DG would make the system very unreliable when a certain penetration level is reached.

3.4 Partial Differential

Another possible solution is line current differential protection. Its fundamental principle is based on the Kirchhoff's current law (KCL) that says "The algebraic sum of currents in a network of conductors meeting at a point is zero". When talking about a single transmission line, the KCL means that the current injecting into one side of the line should equal to the current leaving the other side. If not, then there must exist at least an unexpected current path (i.e., a fault) somewhere on the line. This scheme in nature ignores power flow change and can provide good sensitivity and selectivity for a large range of fault level without any setting modification. It is also long-term applicable with evolving loads and DGs. Those unique features make it intriguing to those situations when more and more DGs are introduced into distribution systems.

3.4.1 Application Examples

Two application examples are shown here to illustrate the advantage of line differential.

In Figure 9, the DG downstream of the feeder relay reduces the fault current the relay will see, thus delay or blind the relay operation. The red curve shows higher penetration level leads to less current sensed by the feeder overcurrent relay. The relay operation may be delayed or even blinded. While

current differential, composed by the measurement points represented by the blue dots in the figure, maintains a high value and even increases with penetration level providing a very good sensitivity.

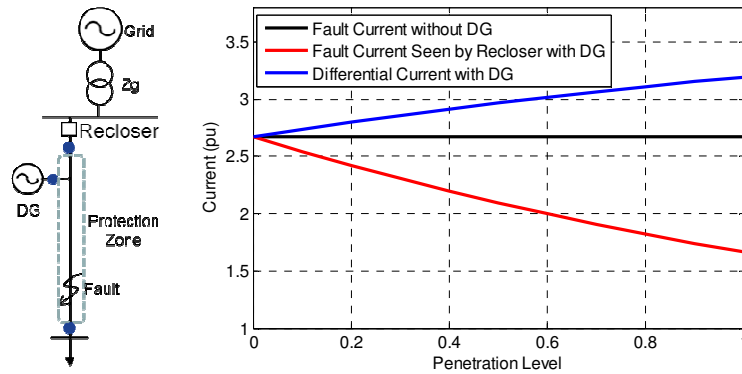


Figure 9: Blinding of protection caused by DG integration

Line differential protection also suits well for microgrid or weak grid application. As we mentioned in previous sections, one protection challenge for microgrid is insufficient fault current level in the islanded operation mode due to low short circuit capacity of the sources. While overcurrent protection can hardly differentiate fault condition with usual load condition, differential protection can provide much better sensitivity as illustrated in Figure 10.

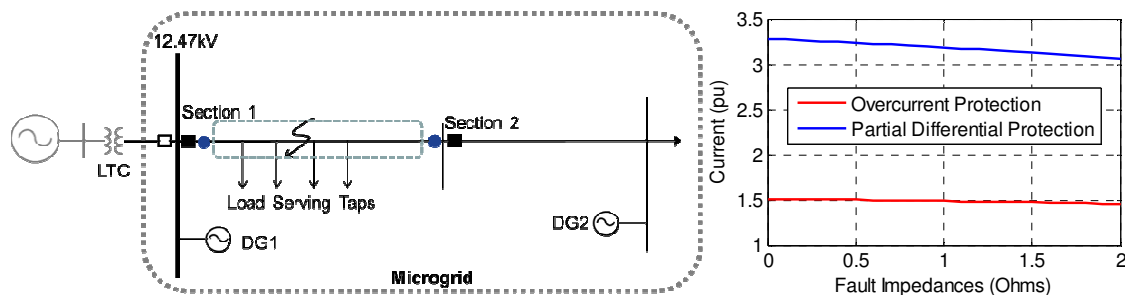


Figure 10: Microgrid / weak grid application

3.4.2 Partial Differential Protection and Sources of Differential Errors

While line differential protection has been commonly applied in transmission system to protect transmission lines, it is not that straightforward to apply it to distribution feeder protection. First, unlike transmission lines that transfer a certain amount of power directly from one end to the other, a distribution feeder has loads distributed along it as illustrated in Figure 14. The strict interpretation of the KCL requires all currents including those on the load serving laterals being measured and summed, while economically it's impractical to put current sensors everywhere for most applications. A more feasible way to apply line differential to feeders with taps would be to only take the current at feeder terminals to do partial differential without measuring tap current.

In doing this, we expect to see tap load current showing up as a differential error during normal operation. Besides leakage tap load current, other sources of differential error include motor back feeding, transformer inrush current, zero sequence current caused by external ground fault, and etc. We will discuss those different types of differential errors in the following sections.

3.4.2.1 Leakage Tap Load Current

With partial line differential protection that only puts current measurement devices at feeder terminals, the tap load current would show up as a differential error during normal operation since it is not measured and counted in the differential comparison. One way to avoid mis-operation is to raise the pickup value above the maximum leakage tap load. Tap load current can be estimated based on the rating of tap transformers or other utility knowledge about the load. Usually the leakage tap current will not be greater than 1 pu thus the pickup will not be greater than 1 pu either. Raising the pickup may sacrifice some sensitivity in some degree. Here we use an example to illustrate a method that can be used to evaluate whether adequate sensitivity can be achieved. In the exemplar case we have a test system with an infinity source feeding a feeder through a substation transformer. The system parameters are illustrated in Table 6.

We evaluate the required sensitivity by worst case analysis. The worst case is defined to be the in-zone fault that causes the least differential current. In our study, it is found to be the case with only one source feeding the fault at the end of the feeder, and during the fault the tap load drops to zero which means during the fault the relays sees only the fault current. Short circuit analysis with different types of fault is then conducted to show the relationship between the worst-case current with the feeder length and fault impedance as shown in Figure 11.

Table 6: Test system parameters

Component	Parameter		Value
Source	Line-Line Voltage (RMS)		69 kV
	Resistance		0.001 Ω
Substation Transformer	Rating		6.5 MVA
	Leakage Inductance		0.1 p.u.
	Ratio		69 kV / 12.47 kV
Feeders ⁽¹⁾	Positive Sequence Impedance	Resistance (R1)	0.2070 Ω /Mile
		Reactance (Z1)	0.6347 Ω /Mile
	Zero Sequence Impedance	Resistance (R0)	0.4409 Ω /Mile
		Reactance (Z0)	1.7957 Ω /Mile

From Figure 11 (A) we see a 20 ohms fault 3 miles from the substation can still cause at least 1.1 pu differential current. Figure 11 (B) and Figure 11 (C) show results with 5 miles and 10 miles feeder. Given the feeder length and the impedance of the fault that needs to be detected, this analysis provides the information to evaluate whether the sensitivity of the partial differential scheme is adequate. This analysis is based on system parameters and fault conditions from the feasibility point of view. Other impacting factors like measurement error and CT saturation are not considered.

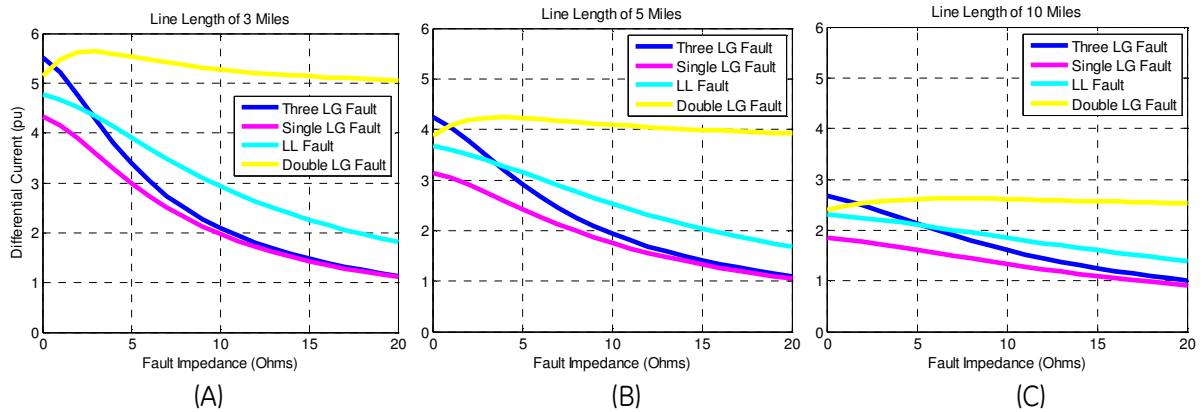


Figure 11: Sensitivity analysis with different fault impedances and feeder lengths

3.4.2.2 Motor Back Feeding

Motor back feeding with dropped voltage is another source of differential error that should not trip differential protection. Motor back feeding to external faults is relatively small decided by $\left(\frac{1}{X_d''} + \text{offset}\right)$. Usually it will decay to normal levels in 1~3 cycles, so one way to avoid mis-operation could be to add a redundancy check in a certain time (for example 3 cycles). Whether the redundancy check will delay relay operation depends on whether the relay is designed to trip instantaneously or with some time delay and how much the time delay is. Usually distribution feeder protection has a more relaxed requirement on tripping time compared with transmission line protection.

Figure 12 shows an example using PSCAD simulation. When an external fault in zone 2 drags the motor terminal voltage down to 0, zone 1 differential relay sees a differential error of about 2 pu, but it decays rapidly in about 3 cycles. Therefore, only section 2 relay will trip but section 1 relay will not.

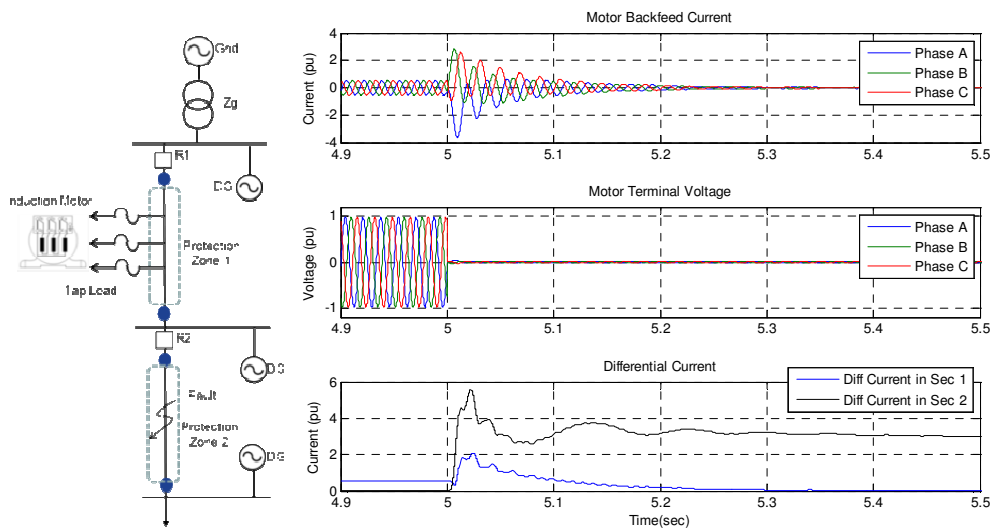


Figure 12: Motor back feeding

3.4.2.3 Impact of Transformer Inrush Current

Transformer inrush current is another source of differential error. The magnitude can be high and the duration can be long. Initial inrush due to energization usually generates more current than recovery inrush after an external fault because the voltage at the transformer location is not going to drop dramatically during external faults [14]. The second harmonic current is a good differentiator for inrush and fault conditions. If this measurement is not available, the differential protection may need to be disabled temporarily during energization.

3.4.2.4 Zero Sequence Current due to External Ground Fault

For a Y/delta tap transformer with Y grounded, it provides a path for zero sequence current during an external ground fault. Therefore, a differential error will be introduced. Meanwhile restraint current increases too since external ground fault also causes phase current rise. We need to look at the incremental value for both differential and restraint current to see whether the differential scheme is jeopardized in this situation. As shown in Figure 13, the zero sequence current flowing through the tap transformer is a portion of the zero sequence component of the fault current (I_{L0}). So the associated differential error is less than I_{L0} . If the restraint current is designed to be $I_{RST} = \text{Slope} \times (|I_L| + |I_R|)$, in which I_L and I_R are local current phasor and remote current phasor respectively, the restraint current can increase by the slope times almost six times of I_{L0} . So for slope value greater than about 0.2, the incremental value for constraint differential current is larger than differential current and it is safe. Otherwise, distance supervision or other techniques discussed in [14] and [15] can be implemented to avoid mis-operation.

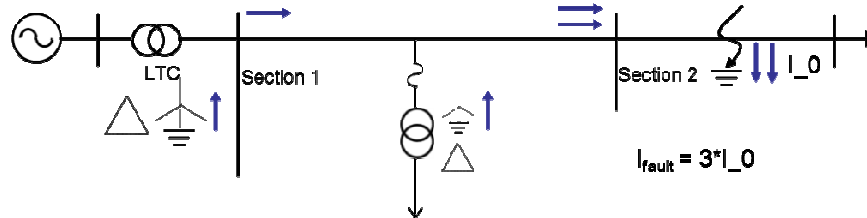


Figure 13: Zero sequence current mis-match caused by external ground fault

3.4.3 Coordination with Lateral Fuses

With partial differential scheme, faults on the lateral downstream of the fuses may also trip the differential scheme which is the main feeder protection, if it hasn't been properly coordinated with lateral fuses.

One possible solution is to incorporate inverse time over current (TOC) feature into the partial differential scheme. Here the current means differential or operational current. Higher differential current will lead to faster tripping. This coordination can work for both fuse-saving and fuse-blowing scheme.

Figure 14 takes fuse blowing as an example. TOC curve of the differential scheme should coordinate with the largest fuse on the laterals, which is with the slowest operation time with the same current. Some extra current margin should be included to incorporate the fact that differential scheme may see an extra portion of leakage tap load current while the fuse only sees fault current with a lateral

fault. Figure 14 shows the generated TOC curve for the differential scheme. It's based upon the largest fuse on the in-zone laterals which is K50 in this case. Time margin is set to be 1.1.

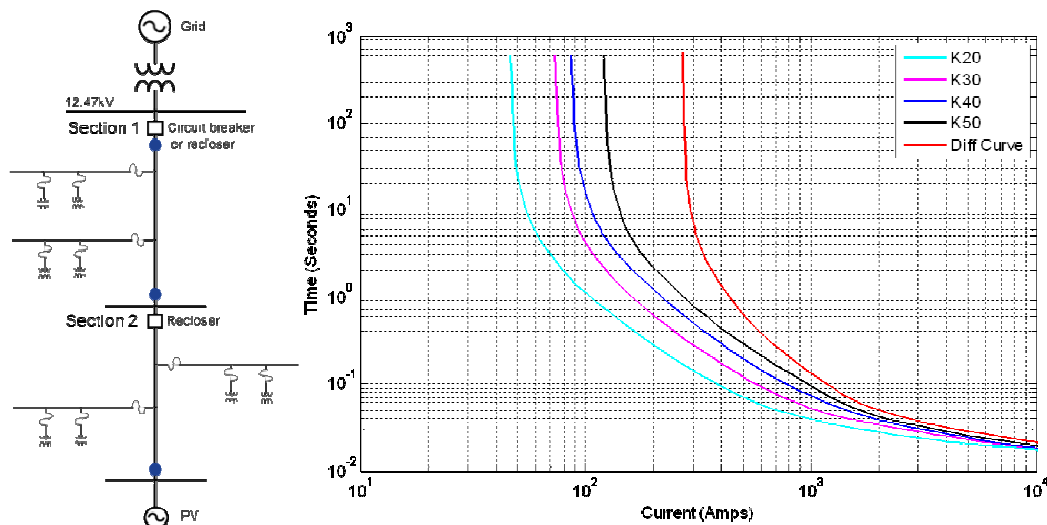


Figure 14: Coordination of main feeder partial differential with lateral fuses

If the operation time of differential scheme is beyond the tripping time requirement, extra current sensing may be needed to put on the large lateral and multi-terminal differential then coordinates with smaller size fuses.

4 Conclusions

This paper presented challenges of protection of feeders with distributed generation and possible solutions. Protection of such feeders is still developing area where many options are being explored. Paper explained that different types of distributed generators would create different fault current levels which may not be suitable for a given type of the protective relay to provide selective and optimum fault clearance. Big challenge is bi-directional fault current distribution which requires either directional or unit protection principles to be used.

Paper also presented some protection schemes, including adaptive overcurrent, distance and directional with pilot aids, partial current differential. Availability of the modern communications allows new protection solutions when protecting feeders with distributed generation.

Application examples were given to illustrate applications problems and possible solutions. Protection and control engineer needs know what type of the distributed generator is he/she dealing with and what is the expected fault current distribution and behavior to choose the protective scheme to achieve best performance. Simulations of the fault scenarios for a given distribution feeder with a given type of distributed generators would be helpful.

5 Literature

- [1] K. Kauhaniemi and L. Kumpulainen, *Impact of Distributed Generation on the Protection of Distribution Networks*, Electric Energy, Online.com, http://www.electricenergyonline.com/?page=show_article&mag=22&article=173
- [2] A. Girgis and S. Brahma, *Effect of Distributed Generation on Protective Device Coordination in Distribution System*, IEEE Large Engineering Systems Conference on Power Engineering, 2001.
- [3] J. A. Silva, H. B. Funmilayo and K. L. Butler-Purry, *Impact of Distributed Generation on the IEEE 34 Node Radial Test Feeder with Overcurrent Protection*, IEEE 39th North American Power Symposium, 2007
- [4] M.E. Baran, I El-Markaby, *Fault analysis on distribution feeders with distributed generators*, IEEE Transaction on Power Systems, Vol. 20, Issue 4, pp. 1757-1764, Nov. 2005
- [5] B. Wojszczyk, B. Flynn and T. Taylor, *Engineering for Increased Penetrations of Distributed Generation, Energy Storage, and Plug-In Electric Vehicles*, Internal Report of General Electric, 2011
- [6] Y. Pan, W. Ren, S. Ray, R. Walling and M. Reichard, *Impact of Inverter Interfaced Generation on Overcurrent Protection in Distribution Systems*, Power Engineering and Automation Conference (PEAM), 2011 IEEE, Wuhan, China
- [7] T. A. Short, *Electric power distribution handbook*, CRC Press LLC, Florida. ISBN 0-8493-1791-6.
- [8] IEEE Standard for Interconnecting Distributed Resources with Electric Power systems, IEEE Std 1547-2003
- [9] Grid Code – High and extra high voltage. E.ON Netz GmbH, Bayreuth, Germany, 1st April 2006
- [10] <http://ewh.ieee.org/soc/pes/dsacom/testfeeders/index.html>
- [11] <http://www.cooperpower.com/library/pdf/R280916.pdf>
- [12] http://www.microgrids.eu/documents/A_Oudalov_Protection_and_Control_Issues_%20Network_Designs.pdf
- [13] Novel Protection Systems for Microgrids, <http://www.microgrids.eu/documents/688.pdf>
- [14] B. Kasztenny, I. Voloh, M. Adamiak and J. Zeek, *Application of Current Differential Protection to Tapped Transmission Lines*, <http://store.gedigitalenergy.com/faq/Documents/L90/GER-3978.pdf>
- [15] B. Z. Kasztenny and C. B. Campbell, *Line Current Differential Protective Relaying Method and Relay for In-Zone Tapped Transformers*, US Patent, US6,829,544, B1

6 Biography

Yan Pan received the M.E.E. in 2003 from Wuhan University, Wuhan, China and the Ph.D. in E.E. in 2009 from Center of Advanced Power Systems of Florida State University. She worked with Beijing Sifang Automation and Relay Company for two years as a relay engineer from 2003 to 2005. Currently she is an electrical engineer with GE Global Research Center, Niskayuna, NY. She mainly works on renewable integration, power system modeling and control, and power system protection. She is an IEEE member.

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