GEC Measurements

Series Compensated Lines: Application of Distance Protection

by

A. Newbould, P. Hindle, *GEC Measurements, United Kingdom*

SUMMARY

Where distance relays are applied to protect series compensated lines, or to protect uncompensated lines directly adjacent to series compensated lines, protection designers and application engineers have recognised that voltage inversion is one of the major electrical phenomena which are characteristic of the series capacitor. This effect needs to be fully considered, since it may prove problematical for the protection. Unfortunately, engineers have lacked a quantitative means of fully determining the degree of voltage inversion that will occur on a practical installation. This paper develops such a method, and via practical examples calculates and plots the extent of the resultant voltage profile. The system configuration chosen is believed to be the worst case for voltage inversion, that with the relay measuring voltage located adjacent to a capacitor. Modern overvoltage protection in the form of MOV's are assumed to be applied to the capacitors. The numerical techniques for representing the non-linear nature of the MOV, replacing it by a linear series equivalent with numerical values dependent upon fault current level, are taken from a previous paper, reference 1. The designer's concern for distance protection, especially when choosing polarising quantities, is to arrive at a figure for the maximum magnitude of voltage inversion, and to understand upon which factors it depends. A simple graphical technique is arrived at which determines the boundary of fault location and values of fault resistances for which the onset of voltage inversion occurs. This is useful in selecting faults during model testing.

Keywords:

Series Compensated Lines, Impedances Seen, Power System Modelling, Metal Oxide Varistors, Distance Protection

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INTRODUCTION

In considering the application of distance relays to protect series compensated lines, or to protect non-compensated lines directly adjacent to series compensated lines, it is important to evaluate the additional electrical phenomena that are characteristic of the insertion of a capacitor into the power system. This paper examines one of the major effects, already recognised by protection engineers as being problematical for distance protection. It is commonly referred to as voltage inversion, although upon detailed analysis, this term can be shown to be somewhat erroneous. The classic explanation is that voltage inversion occurs as a result of inductive current flowing through a capacitive impedance. From a relaying point of view, the maximum magnitude of voltage inversion is expected to occur at a measuring location directly adjacent to a capacitor location. It is for this reason that the end compensated line is judged to be the most demanding for relaying, and has been chosen throughout this paper to develop both the theory and the examples. The mid-compensated line, with its voltage measuring points located well away from the capacitor, is much less likely to produce voltage inversion at the relay; consequently it has been neglected in this work.

A major objective has been to find a means of quantifying, via numerical analysis, the extent by which the voltage inverts. This has a dual purpose, firstly so that a designer of distance protection has reliable information to decide what polarising signals to employ, and secondly so that a protection application engineer can understand the influencing parameters for selecting protection for a particular project. The paper goes on to develop a simple drawing technique to show which faults, of all possible locations, with or without fault resistance, will produce voltage inversion. This is useful during the selection of fault locations prior to model testing. The numerical analysis relies on the techniques developed in two earlier papers, which independently arrived at a linearized model for the non-linear nature of the Metal Oxide Varistor (MOV) overvoltage protection fitted to the capacitor. MOV's represent the most modern method to protect the capacitor from large overvoltages under heavy fault current conditions, and are recognised as giving superior re-insertion performance after clearance of an external fault. For these reasons it is believed that MOV's will prove to be the first choice on all new installations of series compensation. This paper limits its scope to studying series capacitors fitted with MOV overvoltage protection.

LIMITS TO PRESENT TERMINOLOGY

The term voltage inversion is believed by the author to be somewhat of a misnomer, since most of the fault locations on a real compensated line will not produce voltage inversion, but will produce voltage phase shifts stretching beyond those expected on a plain feeder. Support for this point of view will be developed in diagrams later in this paper.

Before doing that, it is worth considering how the term voltage inversion came about. Without the advantage of today's computing resources, engineers attempted to simplify the rather difficult analysis of series compensated lines. It appears that they chose to eliminate one of the smallest parameters, the circuit resistance. This approach leads to only two types of impedance, inductive and capacitive reactance. The overall impedance, being the sum of a positive and negative reactance, then can only be one of the two types, depending upon which has the larger magnitude. The resultant voltages lie along the line of the EMF, and are therefore either in-phase or in anti-phase with it. The latter possibility led to the term 'voltage inversion'. At the balance point, where the reactances are equal but opposite, then major resonance would theoretically occur, making the current and voltage indeterminate; a problem never fully resolved by earlier proponents of this simple technique.

Engineers who have studied resonant circuits in detail will recognise the weakness in this approach. It is the circuit losses dissipated in the form of heat, above all else, that decide the degree of resonance. In fact in other fields, engineers have developed specific terms to define the likelihood, and/or the degree of resonance. "Damping ratio" is the usual control theory term, which is then classified under "overdamped", "critically damped", and "under-damped" subgroups. Such definitions assist in evaluating the likely type of transient performance. The alternative term of "Q factor" is used in communication circuits, especially those involving oscillators. In essence, both of these terms strive to relate the ratio of energy stored against energy dissipated for a particular component, or for a whole circuit.

A totally different and separate argument can be made for power systems. If it were possible to design a series compensated line such that there was a risk of major resonance, then large transient overvoltages and overcurrents would result whenever a shock was applied to the system, such as the occurrence and clearance of faults. This could push the system beyond safety limits on both voltage and current, risking damage not only to the capacitors, but also to much of the insulation. The author is convinced that this does not happen in practice. The circuit losses, both in the form of conductor resistance and the heat dissipated within the varistor appear to be very effective in controlling the degree of resonance.

It should now be an obvious statement that an accurate study of series compensated lines requires that the most important parameter, the circuit losses, are included in the model. By accurately representing the power losses, particularly in the MOV, the following analysis does that.

DESCRIPTION OF SERIES COMPENSATED LINE EMPLOYED DURING ANALYSIS

As explained in the introduction, the system configuration chosen is that with the capacitor at the line end location, as this is reasoned to produce the greatest degree of voltage inversion at the relay measuring location. Fig. 1 shows the single line diagram of the total arrangement. The Potential Transformers (P.T.'s) are taken to be on the Bus side, also the capacitors are fitted with MOV overvoltage protection. The type of fault analysed is the 3 phase fault. The numerical example has been chosen from a practical example of series compensated line, with physical parameters as given in Fig. 1.

ANALYSIS OF VOLTAGE PROFILES

Since a distance relay is expected to provide high speed clearance for all internal faults, then instead of searching specifically for voltage inversion, it is better to generalise the analysis. What is required is a view of the total relay measuring voltage profile for all fault locations, inclusive of fault resistance. From this the voltage inversion issue will then be an obvious subset. A polar diagram can be drawn which shows the maximum voltage at any one phase angle to which the relay will be subjected. Since the relay measuring voltage is a function of source impedance, line impedance and fault resistance, then to gain a complete picture it is necessary to vary all parameters over their expected range. This paper has chosen a method which firstly fixes the source impedance, then calculates a set of voltage loci for all fault locations and fault resistance, plotting these on a diagram. This is repeated for several steps of source fault level. The final chart then is formed from the accumulated boundary into which all other voltage loci fit. Readers should recall that the concern is to find the maximum voltage that can occur at any phase angle. Lesser voltages are not expected to produce problems, since these occur on all systems under fault, including plain feeders.

Using the linearised model developed in references 1 & 2, this is a relatively simple task. The parallel capacitor/MOV components need to be replaced by an equivalent linear series model as summarised in Fig. 2. The numerical values are dependent upon the level of fault current, and arrived at via a look-up table. Since the fault current itself depends upon the state of the capacitor/MOV combination, then this problem demands an iterative solution. This was accomplished on a personal computer. For more details see reference 1. Once the fault current is known, then it is a simple task to arrive at the voltages at any point along the network model. Figs. 3a and 3b illustrate the voltage loci that have been calculated. Fig. 4 then integrates all of these loci onto one diagram. The dotted line shows the equivalent figure for a plain feeder. Although not calculated, it is relatively easy to show that this is basically a semicircle for the sending end of the line. To complete Fig. 4, the MOV trigger voltage has been added, and shown as a reference for inverted voltage on the negative axis. The maximum inverted voltage component never exceeds the MOV voltage, in fact, the closest it comes is around 85% of the MOV trigger voltage.

FACTORS AFFECTING THE CHOICE OF POLARISING VOLTAGES FOR DISTANCE RELAYS

The prime advantage of using the quantitative approach of Fig. 4 is that it places a maximum magnitude against the degree of voltage inversion that can occur in a practical application. The diagram further relates this maximum with the MOV protection level expressed in voltage terms, rather than the more usual current form. The data highlights that strict voltage inversion occurs only for a minority of faults, and in truth, excessive phase shifts are much more common. From this we can develop a basis to select the right mix of polarising for a distance relay designed for such applications.

The relay designer is faced with 3 main options for polarising signals :

1. Self (Fault Voltage) Polarising
2. Memory Voltage Polarising
3. Sound Phase Voltage Polarising

Although early designs of distance relays tended to restrict the choice of polarising to one main type, today's static relay designs can easily use a variety of signals, without adding cost or complexity to the circuitry. For example, summing amplifier techniques can provide several inputs, simply by adding one input resistor per signal.

Within a distance relay, the main function of the polarising signal is to act as the phase reference signal, to which other signals, in particular, the V-IZ compensated voltage signal, are compared via a phase comparator. The optimum polarising signal is one that maintains its vectorial position regardless of what system parameters, type of fault, fault location, or fault resistance, occurs. From the application viewpoint, a mix of signals can be advantageous, since no one signal appears to provide reliable polarising for all the circumstances envisaged.

Before addressing the recommended choice of polarising signals for a modern relay, it is appropriate to consider two aspects that have been recognised as issues in the past: memory design and grounding practices on series compensated lines.

MEMORY TECHNOLOGIES

It has long been known that one of the ways in which a distance relay can be made to overcome the risk of losing its directional sense during voltage inversion is to employ some form of memory polarising, i.e. pre-fault voltage polarising. Early practical designs relied upon an LC resonant tank circuit, tuned to system frequency, which continued to oscillate after the input voltage collapsed due to the fault. Two problems existed, firstly the magnitude of the memory was not fixed, but decayed exponentially with time, and secondly it was difficult to keep the phase relationship correct. The circuit was prone to run slightly off tune, accumulating phase errors as time extended after the fault. Maloperation of distance relays due to loss of directionality could result. Non-linearity of the inductance and an inability to track system frequency changes were further problems that limited the extent to which memory could be applied. Generally speaking, the LC resonant tank technology could only provide a relatively small magnitude of memory for a short duration.

Relay designs employing new technology have overcome these problems, for example a digital delay line can be used. On loss of its input voltage, a delay line will continue to play the stored pre-fault voltage to its output, thus providing an effective memory action, see Fig. 5. A delay line holding several cycles of system frequency can easily be manufactured from standard electronic parts available today. The "clock" or "heartbeat" that drives the delay line is now frequency locked with the power system frequency, thus avoiding any discrepancy between the memory and the power system frequencies. For this reason, the feature within the commercial product, (Micromho distance relay), is called Synchronous Polarising. The magnitude is fixed by nature of the digital square wave signal, hence a constant size of memory is available, avoiding the variable amplitude problems of the earlier designs.

A more esoteric issue relates to the waveshape of the memory signal. Early LC tank circuit designs gave an inherent sinewave output, while digital technology, in its simplest form, offers square wave techniques. Where MOV's are applied across the series capacitor, the resultant system voltage takes on a definite square wave nature during faults due to the instantaneous voltage limiting qualities of the MOV. Proof of this has come from both Electro Magnetic Transient Program (EMTP) computer studies, and also Fig. 2 of Reference 1. The mixing of sine and square waves is more complex than sine plus sine. There is a definite tendency for the resultant phase angle, defined by the zero crossings, to become "phase locked" to the square wave, unless the sine wave is several times larger than the square wave. Because of this phenomenon, there must be some doubt as to whether a sine wave memory could actually prevent distance relays maloperating under voltage inversion, as the MOV voltage could dominate the resultant polarising phase angle, and thus fail to prevent voltage inversion from reaching the comparator input.

If the memory is a square wave, and the incoming voltage is a square wave, then this problem does not exist, as long as the relay memory magnitude is greater than the square wave component arising from the MOV. This is one reason why the analysis of the maximum inverted voltage, summarised in Fig. 4, is so important to the relay designer. The author believes that because of these arguments, there must be a definite preference to employ square wave memory polarising to distance relays applied to series compensated lines employing MOV protection on the capacitors.

The description so far has been on a single phase basis; however, the actual memory is a 3 phase device. In a full distance relay, 6 comparators will normally be employed, 3 connected phase to phase, and 3 connected phase to ground. Each comparator requires its correct polarising reference. Rather than use 6 memories, one digital memory can be used that has 6 take off points at different positions on the delay line. This is advantageous both in reducing hardware, but more importantly it ensures that all 6 memory polarising signals are phase locked to each other; an obvious requirement.

The single phase input to the delay line is achieved by first delaying 2 of the phase-neutral voltages by an appropriate angle to arrive at 3 co-phasal signals, see Fig. 5. All voltages at this point are square waves. The resultant is formed by a majority gate whose instantaneous output will follow the polarity of the majority, i.e. if 2 or more of the inputs are positive, then the output will be high, otherwise the output will be low. An interesting, and useful by-product of this approach is that the resultant can still be correct even with the loss of one phase. This means that the input to the memory system can be maintained virtually unchanged during single phase to ground faults. The memory then has an unlimited length, since correct loading of the delay line input is continuous. Only under multiple phase faults will the input become unreliable and the memory will eventually become exhausted. The present design caters for a memory length up to 11 cycles of fundamental frequency.

IMPACT OF Zs0/Zs1 RATIOS

It is well known that the ratio of Zs0/Zs1 varies on practical power systems, with the exact figure depending very much upon the grounding practices and the location of the ground points relative to the substation of concern. For distance protection, the implication of high Zs0/Zs1 ratios is that the sound phase voltages undergo considerable induction arising from the flow of ground fault current, so much so, that they can become unreliable as sources for polarising. In most EHV power systems the Zs0/Zs1 ratio is small, and often less than unity; thus the problem of sound phase voltages moving in phase and magnitude during ground faults is very limited. This is because most substations have within them power transformers, often considerable amounts in terms of MVA. Such transformers are normally grounded, thus providing a local route for zero sequence current to flow, and it is this path which keeps the Zs0 figure low.

Series compensated lines are inherently involved with long distance transmission. Typically they would connect two strong parts of an overall power system, with each part involving low Zs0/Zs1 ratios. However, experience of practical series compensated power systems has shown that some of the intermediary substations on the long distance transmission route have been installed primarily to house some of the capacitors. In fact in a few cases, no power transformers were included at all in the substation. The outcome was that the relay locations at the intermediary substation had very high Zs0/Zs1 ratios, similar in fact, to the incoming lines. This ratio can be pushed even higher when the incoming lines are themselves series compensated at the remote end. The figure encountered for the Zs0/Zs1 ratio was near to 6 for the worst example. This is the largest figure ever encountered for an EHV line that is known to the author. Under these circumstances, the sound phase voltages were found to rise up to 140% of normal during ground fault conditions. Significant phase shifts can also result. This ruled out the extensive use of sound phase polarising for ground fault relays.

PRACTICAL POLARISING VOLTAGES FOR SERIES COMPENSATED LINE APPLICATIONS

A practical choice of distance relay polarising voltages for series compensated line applications has to take into account both of the factors addressed above, i.e. the maximum degree of voltage inversion and the fact that large Zs0/Zs1 ratios may exist at a few of the substations. Fortunately both of these factors produce similar effects, and therefore, benefit from the same type of solution.

As stated earlier, a mix of polarising signals is seen to be an effective way of covering the variety of conditions encountered. The practical solution has, therefore, been to summate all three types of polarising, but in a definite order of priority. The prime candidate is self polarising; this has been credited with a 1.0 per unit rating. This obviously will reduce under fault conditions, and may invert to a limited extent, as defined by Fig. 4. To prevent such reversals overpowering the total polarising signal, thus risking the loss of directional response of the protection, then the memory signal forms the second component in the polarising mix. A figure of 0.8 p.u. has been employed. This is larger than the maximum amount of voltage inversion expected in practice. As concluded from Fig. 4, the maximum voltage inversion is related to the MOV overvoltage protection. MOV protection levels encountered in practice typically lie between 0.3 and 0.65 p.u. Note, this p.u. figure is related to the system emf and not to the current rating of the line. Rather than varying the amount of memory for different applications, a fixed figure of 0.8 p.u. of memory has been chosen so that it covers what is believed to be the worst case condition. This ensures that the one design of relay is potentially suitable for all applications.

The third component is cross polarising; a small amount has been retained to ensure that the relay can still provide Zone 2 and 3 time delayed trips for zero voltage ground and phase-phase faults. Under these conditions the memory may well be exhausted by the time that the delayed zones are expected to operate, and with no fault voltage, there will be no polarising reference for the comparators. A minimum amount of cross polarising solves this problem.

GRAPHICAL METHOD TO IDENTIFY FAULT LOCATIONS UNDERGOING VOLTAGE INVERSION

Although the text so far has addressed the problem of finding the maximum amount of voltage inversion that can occur at a relay measuring point, there is no rationale to pinpoint those faults producing voltage inversion in a given system. In fact we have shown via the diagrams of Fig. 3 that a system configuration with a strong source does not produce voltage inversion at all. Engineers would benefit from an approach that would easily identify, for a given system, those faults undergoing voltage inversion. This would be especially useful during model testing. Rather than the present random fault selection technique, a series of tests could be particularly chosen to stress a relay's ability to withstand voltage inversion.

The objective of this section is to show that there is a simple graphical method to highlight both those fault locations and those fault resistances, which will result in a component of voltage inversion at the relay location. The method relies on the results of a past paper. Reference 1 developed the principles behind a set of impedance seen diagrams, taking full account of the non-linear nature of the MOV protection. To avoid duplication of the explanation, the examples employed to develop the graphical method in this paper will be taken directly from reference 1. In particular Figs. 6, 7a, 7b, 7c and 7d will be repeated here. The diagrams show that the impedances seen are significantly affected by the firing of the MOV's. Not only does this introduce a resistive component to the impedance seen, to represent the heat loss in the MOV, it also significantly reduces the effective value of capacitance.

EXPLANATION OF GRAPHICAL CONSTRUCTION

The relay measuring fault voltage is a phasor quantity which can, for convenience, be broken into two orthagonal components, namely a component that is in phase with the pre-fault voltage, and a second component that is in quadrature with the pre-fault voltage. Ignoring load currents, then the pre-fault voltage is in fact the system emf. The onset of the voltage inversion phenomena occurs when the fault voltage is in quadrature with the emf, i.e. when the in-phase component of fault voltage is zero. Protection engineers are accustomed to drawing the E, IZs, I(ZL + Rf) vector triangle since E = IZs + I(ZL + Rf) see Fig. 8. Locating the quadrature condition of E and V is easy: it must lie on the boundary of a circle as drawn in Fig. 8. The circle is drawn to intercept the origin and the tip of the -Zs vector. From this simple figure we can make three observations, as follows :

> Fault locations which give impedances seen lying on the boundary of this circle will have a fault voltage in quadrature with the emf, i.e. the fault voltage has no voltage inversion component.
>
> Fault locations resulting in impedances seen lying outside the circle will have a fault voltage with a component in phase with the emf.
>
> Fault locations resulting in impedances seen lying inside the circle will have a fault voltage with a component in anti-phase with the emf.

The degree of voltage inversion grows as the impedance seen vector approaches - Zs, although how close the point can move towards the "Black-Hole" of infinite resonance, i.e. at the lower tip of the Zs vector where (ZL + Rf) = - Zs, depends upon the maximum degree of resonance that is possible on any given power system. Infinite resonance is impractical in that it represents zero losses in the system. Even major resonances must be avoided since they could overstress much of the power system equipment. The degree of resonance is defined and controlled by the MOV's firing voltage. In this context it is best expressed as a per unit figure relative to the system emf, and not as a by-pass current level. The two figures are simply related, since the voltage by-pass level equals the current by-pass level multiplied by the reactance of the capacitor.

SUPERIMPOSING THE IMPEDANCES SEEN CHARTS WITH THE VOLTAGE INVERSION CIRCLES

The task of superimposing the voltage inversion circle on top of the impedance seen diagram is extremely simple. For each impedance seen diagram, it is necessary to draw the - Zs vector with its tip touching the origin. A circle is then constructed with its diameter on the Zs vector, see Fig. 9. Fault locations which result in impedances seen lying within the circle will have a component of voltage inversion within their fault voltage. An overview of the voltage inversion problem is obtained by surveying the five diagrams of Figs. 9 and 10. Strong sources produce the least number of fault locations and the least magnitude of voltage inversion. Conversely, weak sources produce the greatest number of fault locations and the greatest magnitude of voltage inversion. The diagrams further illustrate that the number of fault locations undergoing voltage inversion are a relatively small proportion of all faults, assuming a random dispersion of faults along the line.

CONCLUSION

This paper has shown that there is a means for analysing series compensated lines that models the resonance correctly, taking full account of the power losses in both the conductors and more importantly in the MOV capacitor overvoltage protection. The technique has been used to study, over a full range of fault location and fault resistance, the phenomenon of voltage inversion. The author shows this term to be a misnomer. Voltage phase shifts beyond those expected on plain feeders is strictly the phenomenon that is occurring on series compensated lines. It is difficult to come up with a new phrase that adequately defines the true effect, hence the existing term of voltage inversion is likely to remain endemic in the protection engineer's mind. Hopefully, engineers having read this paper will begin to add conditional statements in future to their use of the term "voltage inversion".

The work has given credence to the correct selection of polarising voltages for distance relays for series compensated lines. Although it could be possible to adjust the percentage of memory polarising for every application, a simpler and more universal approach is to design the relay for the maximum expected degree of voltage inversion, shown in this paper to be related to the capacitor overvoltage protection. For this purpose, the overvoltage protection needs to be expressed in per unit terms relative to the system emf. Typical values range from 0.3 to 0.65 p.u. The practical relay has 0.8 p.u. memory polarising, thus exceeding presently known levels of MOV overvoltage protection.

A graphical method has been introduced which extends the results of earlier work. Using the impedances seen calculations and diagrams of reference 1, it is possible to rapidly identify those fault locations and fault resistances undergoing a component of voltage inversion.

It is not proposed at this stage that the theory contained in this report is ready to displace what has been up to now the only practical means of proving protection performance on series compensated lines, namely model tests. The author believes that the main strength of the theory is to give direction and purpose to a series of tests. For example, it is now possible to identify those fault locations where voltage inversion is most dominant. If any protection undergoing customer approval is believed to suffer in performance from voltage inversion, then the theoretical means exist to optimise a set of tests to stress its abilities in that area.

ACKNOWLEDGEMENTS

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REFERENCES

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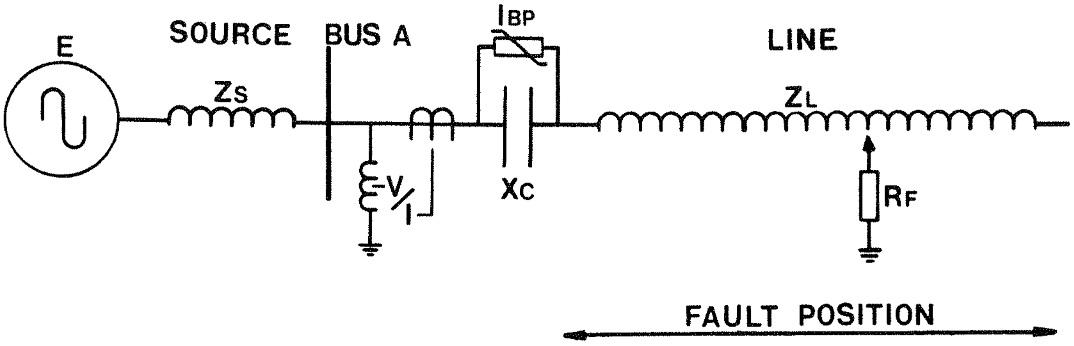
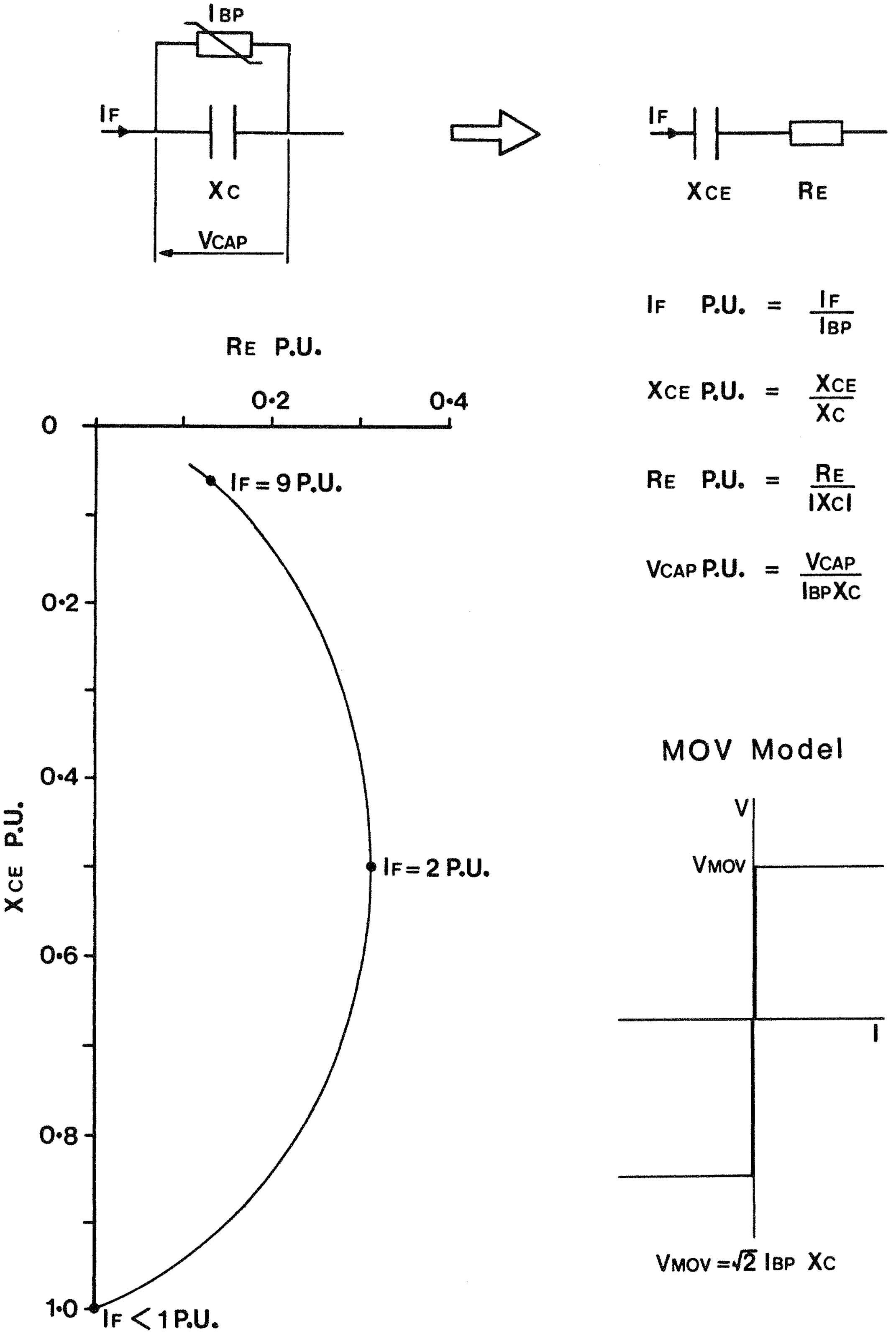
2. Daniel L Goldsworthy, "A Linearized Model for MOV-Protected Capacitors" IEEE/PES Summer Meeting 1986

Single Line Diagram



Parameter	Symbol	Value	Units
System EMF	E	525	KV
Source Impedance	Z_S	0.2 + j5 to 3.2 + j80	Ohms
Line Impedance	Z_L	4 + j60	Ohms
Fault Resistance	R_F	0 to 40	Ohms
Capacitive Reactance	X_C	−j18	Ohms
MOV Bypass	I_{BP}	5.6	KA

Fig 1 Power System Details Employed During Analysis



$$I_F \text{ P.U.} = \frac{I_F}{I_{BP}}$$

$$X_{CE} \text{ P.U.} = \frac{X_{CE}}{X_C}$$

$$R_E \text{ P.U.} = \frac{R_E}{|X_C|}$$

$$V_{CAP} \text{ P.U.} = \frac{V_{CAP}}{I_{BP} X_C}$$

Fig 2 Equivalent Series Impedance of Capacitor with MOV
Copied from Reference 1

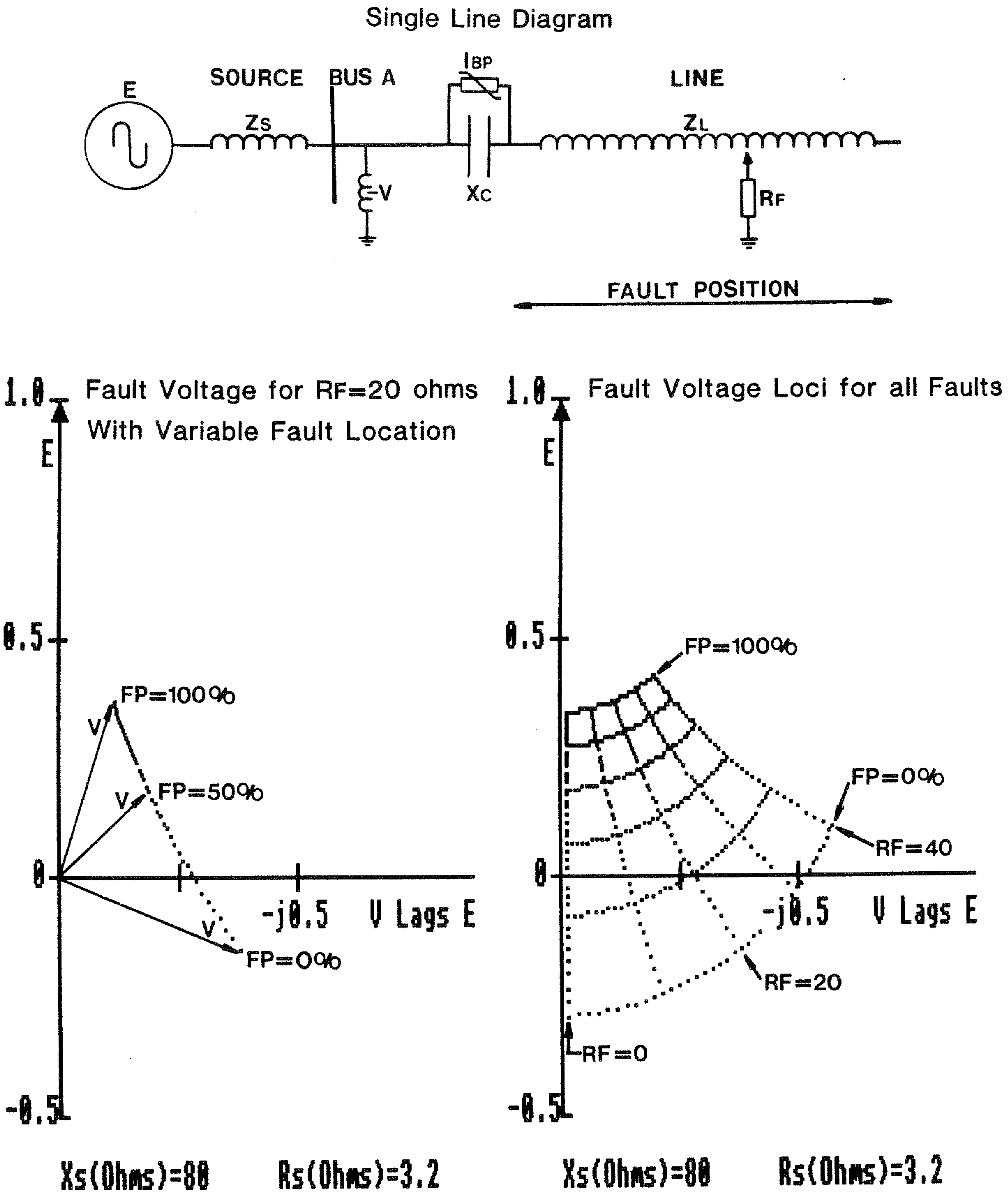


Fig 3a Development of Fault Voltage Loci

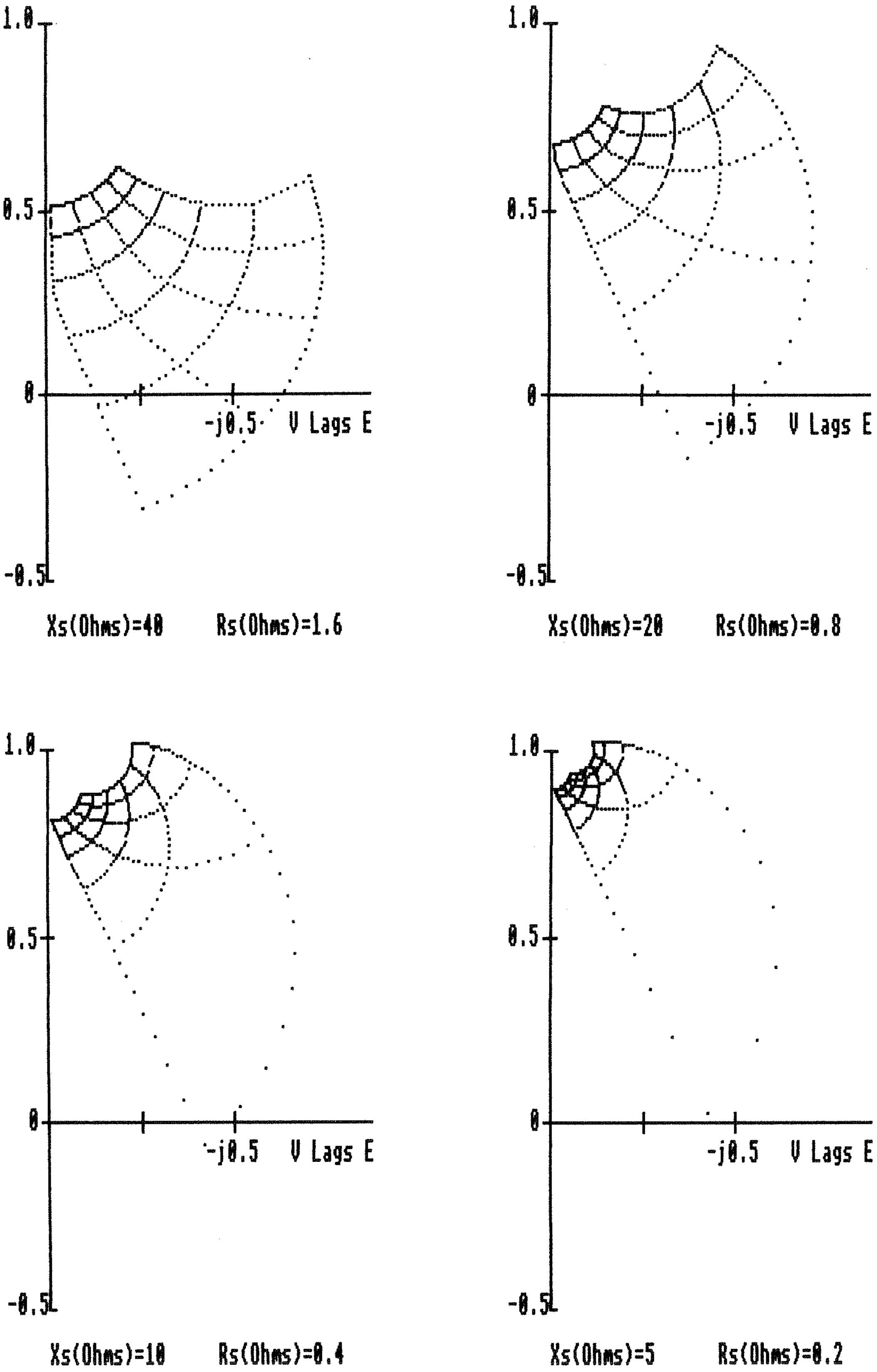


Fig 3b Fault Voltage Loci for Various Source Conditions

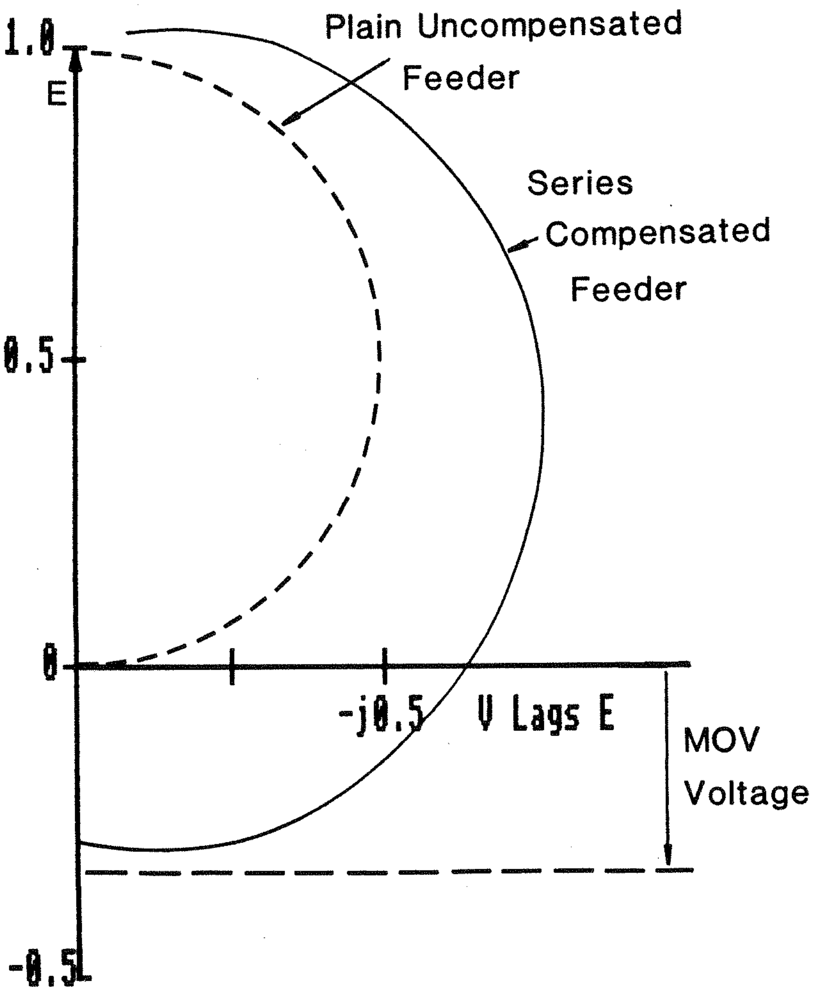
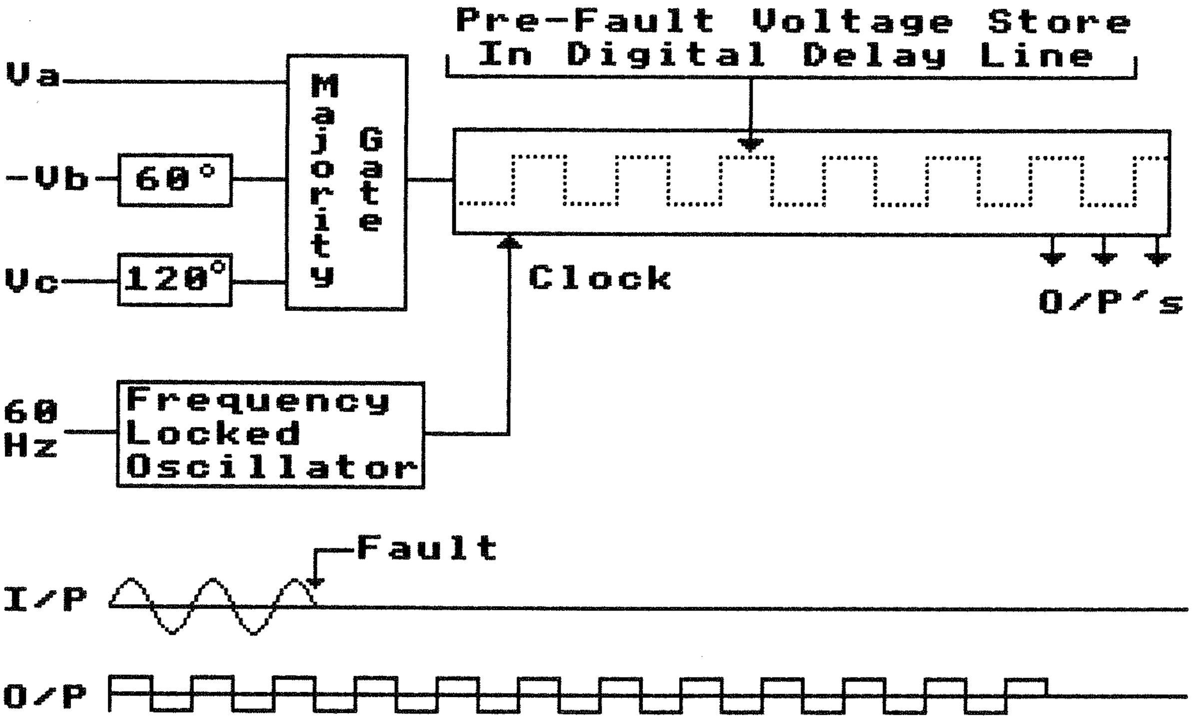


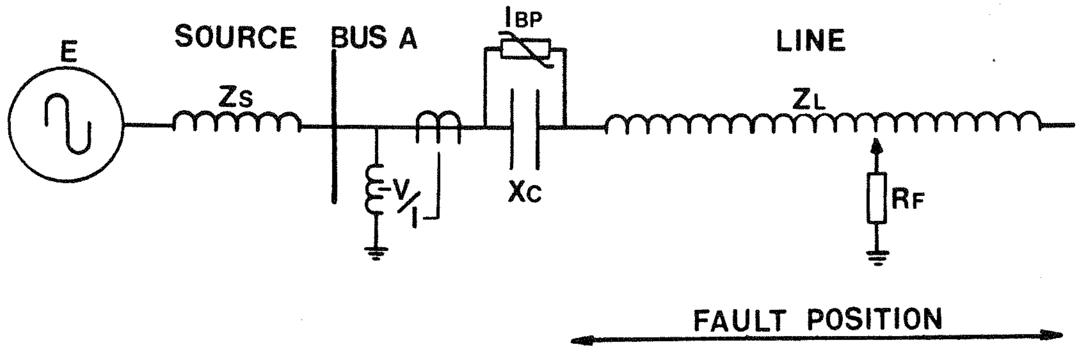
Fig 4 Overall Limits to Fault Voltage
- Series Compensated Feeder Example
- Plain Uncompensated Feeder



Note - Memory Length Not To Scale

Fig 5 Schematic of Digital Synchronous Polarising

Single Line Diagram



Impedances Seen at Measuring Location for Line Faults

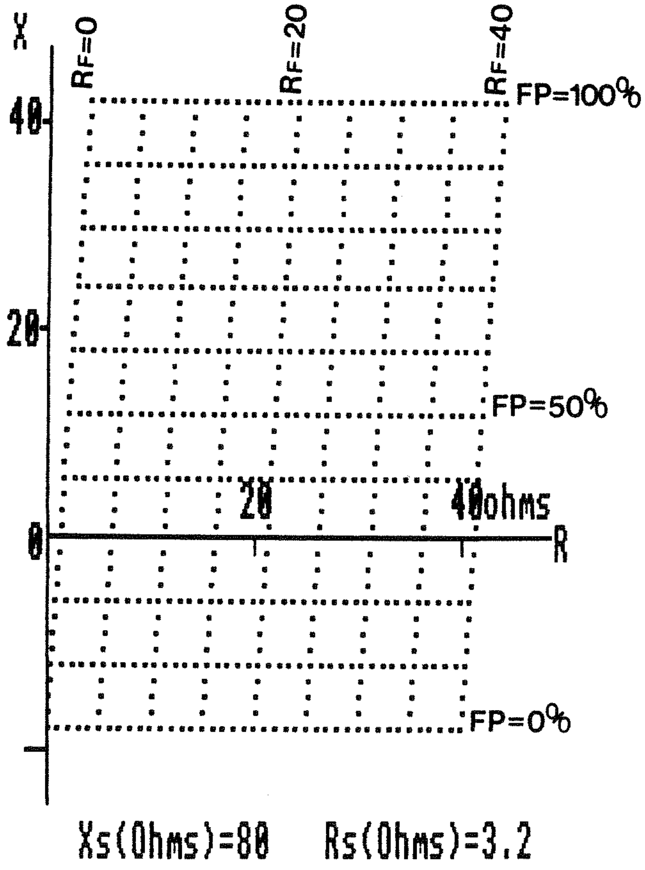


Fig 6 Line End Compensated Scheme

Copied from Reference 1

Example Plot with ZL=4 + j60, Xc=−j18, Ibp=5.6 KA, E=525 KV

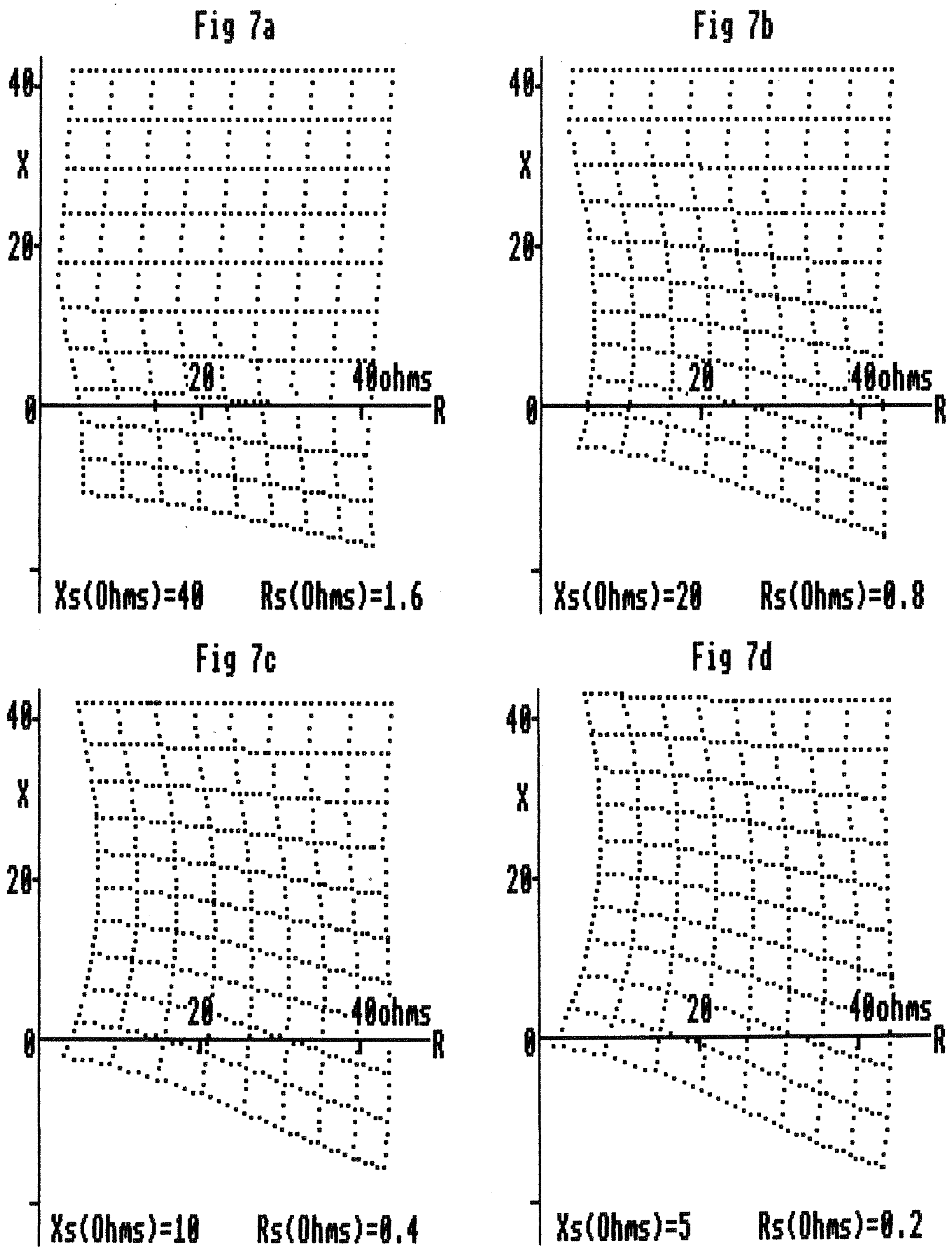
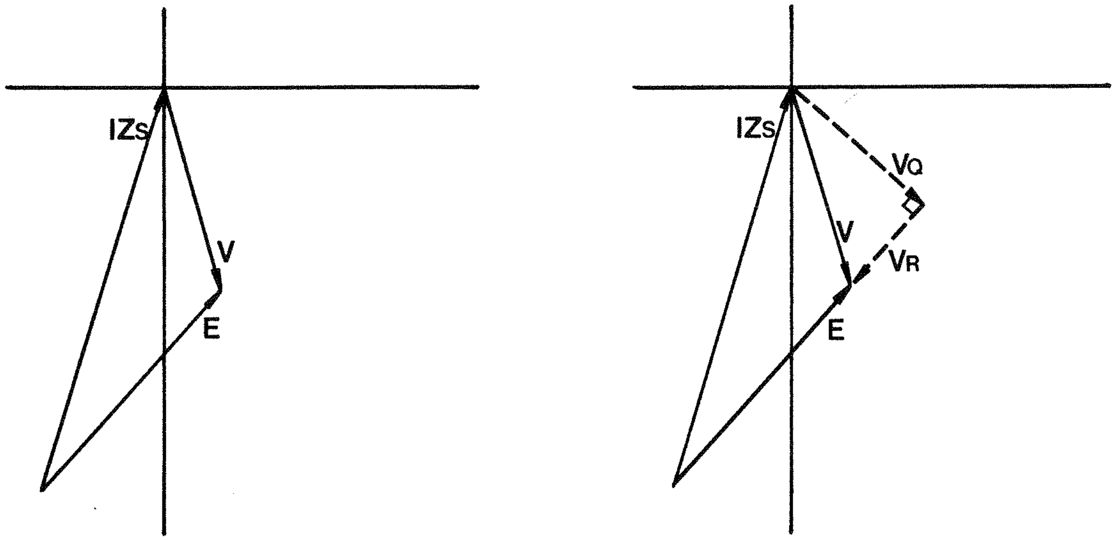


Fig 7 Impedances Seen at Measuring Location for Line Faults
Details as Fig 6
Copied from Reference 1



E,V,IZs Vector Triangle

Orthagonal Components of V

Boundary of Voltage Reversal is when $V_R=0$, Then $V = V_Q$
Hence V and E are in Quadrature

Voltage Inversion Circle

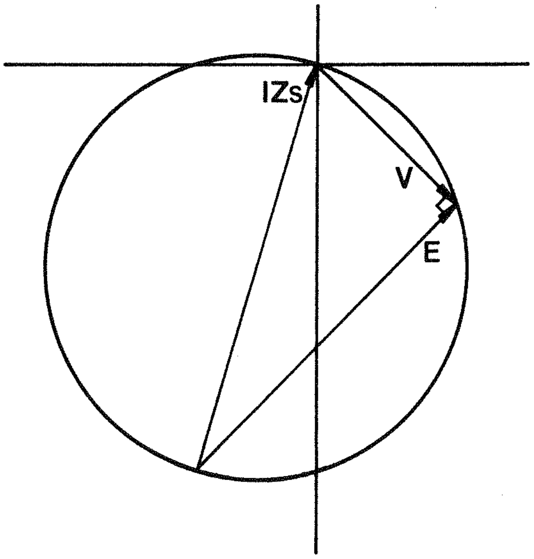
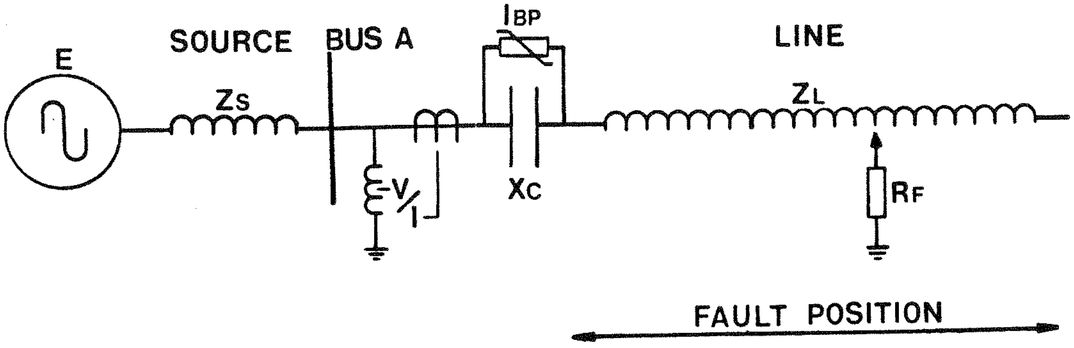


Fig 8 Graphical Method to Identify Boundary of Voltage Inversion

Single Line Diagram



Impedances Seen at Measuring Location for Line Faults

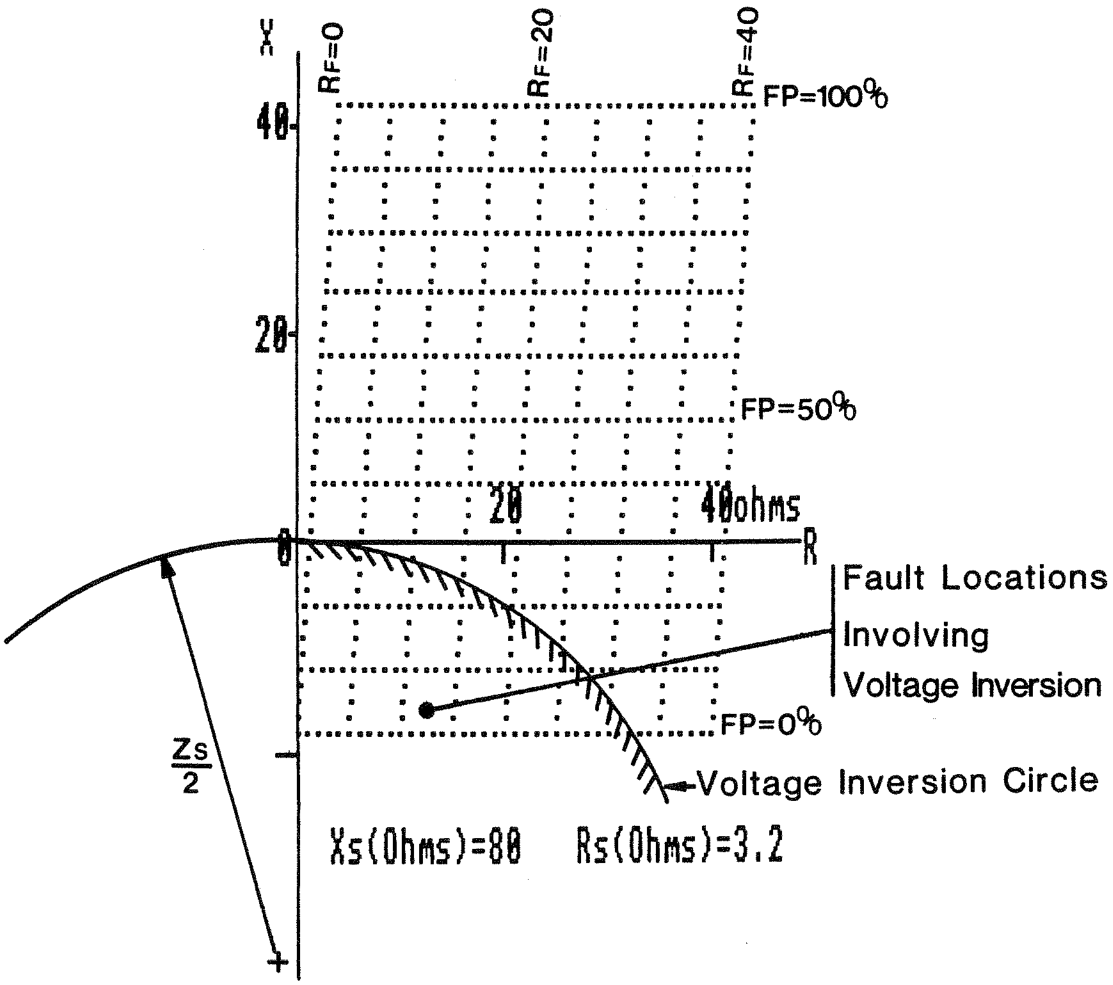


Fig 9 Impedance Seen Diagram Modified to Show Faults Involving a Component of Voltage Inversion

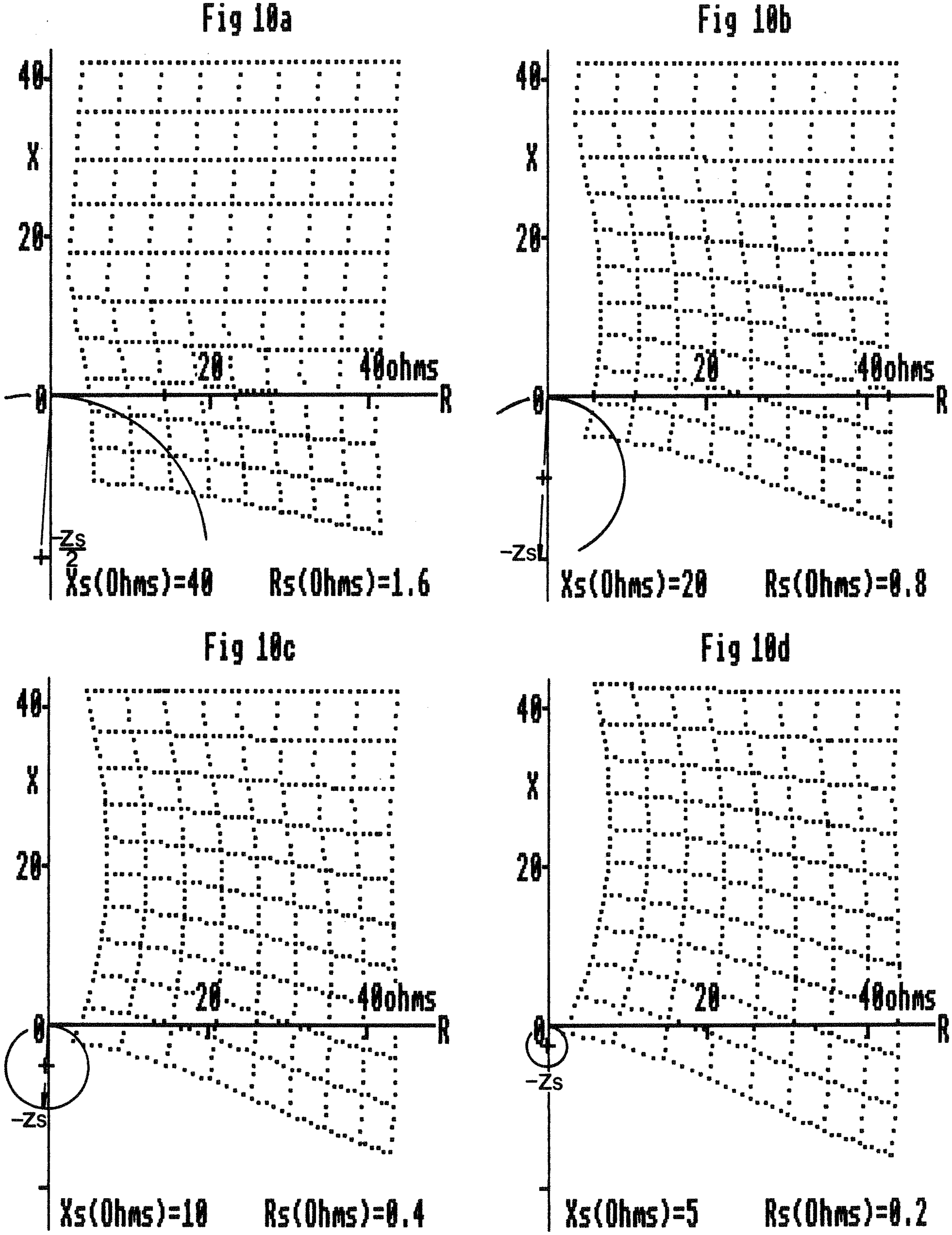


Fig 10 Impedance Seen Diagrams Modified to Show Faults Involving a Component of Voltage Inversion

GEC Measurements

The General Electric Company p.l.c., of England
Relay and Instrument Division
St. Leonards Works Stafford ST17 4LX England
Telephone: 0785 223251 Telex: 36240

The English Electric Corporation
106 Midland Avenue
Port Chester
New York 10573 U.S.A.
Telephone: 914 937 7450 Telex: 4750323

GEC Canada Ltd.
5112 Timberlea Boulevard
Mississauga
Ontario
L4W 2S5
Telephone: (416) 624 8300 Telex: 06-961280

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