CANADIAN ELECTRICAL ASSOCIATION

MARCH 1987
VANCOUVER

SERIES COMPENSATED LINES
ISSUES RELEVANT TO THE APPLICATION OF DISTANCE PROTECTION

A Newbould
GEC Measurements
Stafford, United Kingdom

SUMMARY

Where distance protection is applied to series compensated lines, engineers lack a readily available and accurate means of plotting the impedance loci of faults, which takes into account the capacitor and the non linear nature of its own overvoltage protection. This paper develops an enhanced steady state representation of the overall capacitor impedance with parallel voltage limiting metal oxide varistors fitted, which varies depending upon the level of fault current flowing at the capacitor location. The method begins with transient numerical analysis yielding instantaneous voltages and currents, from which steady state fundamental frequency components are derived via Fourier analysis. By dividing the voltage vector by the current vector, a complex impedance is obtained giving an effective series impedance i.e., an effective value of capacitive reactance plus an effective resistance. The results are found to fit into reliable curves on the X-R impedance diagram, following very close to the arc of a circle. Taking the conclusion of this work as an element, the paper then constructs, using numerical iteration, the 3 phase fault impedance loci seen on three practical examples of series compensated lines as the fault location and fault resistance are varied.

Keywords: Series Compensated Lines, Impedances Seen,
Power System Modelling, Metal Oxide Varistors,
Distance Protection

INTRODUCTION

Where distance relays have been applied to series compensated lines, there has always been a significant technical problem of how to represent the fault impedance loci on a standard X-R impedance diagram, taking into account the effect of the capacitors and their own overvoltage protection. Without a basis for judgement, engineers have been known either to completely ignore the capacitors, on the false basis that their overvoltage protection will always fire, or inversely, always include the capacitor in their calculations and on their impedance chart, regardless of the fault current entering the capacitor. Using the latter erroneous assumption it is easy to identify fault locations where the voltages and currents that would result are beyond all sensible maximum limits. If this did occur, then the insulation of the whole system would be threatened, and circuit breakers would be pushed dangerously beyond their safe breaking capacity. Clearly neither of these events happen in practice, and this is readily confirmed by consulting the technical literature of the series capacitor manufacturers. To enable the series compensated line to function within its design limits, the capacitor must flash over for heavy faults, not only to protect itself, but also to avoid the risk of major resonance which would stress other components in the power system. Lesser fault currents, however, cannot be guaranteed to cause the overvoltage protection to function.

With an inadequate theory, protection engineers have been forced either to ignore the true effects of the series capacitors, or to fund extensive laboratory model tests to find out what performance can be expected from the protection. The author's company has already successfully undertaken several of these test series involving the application of distance protection to series compensated lines. The modern laboratory approach is to employ the EMTP suite of computer programs, feeding data to a Programmable Transmission Line. Despite the success of this practical work, the protection engineer would benefit from any theoretical method which encompassed as many of the aspects of the series capacitor as possible. Any proposed technique, therefore, must make a valid judgement as to whether the fault level is, or is not, above the varistor by-pass level of each capacitor bank, and to take this into account in the impedance loci that are drawn.

The purpose of this paper is to show that there is a simple technique available to arrive at an equivalent impedance for the capacitor installation, which is complimentary to the larger EMTP type of computer analysis. In fact much of the motivation for the approach has stemmed directly from trying to make some valid pre-judgements prior to starting a comprehensive EMTP analysis for protection testing purposes.

VALIDITY OF EXISTING STEADY STATE ANALYSIS METHODS

For the application of distance protection to plain, non series compensated feeders, it has been customary to perform steady state calculations. These normally take the form of an algebraic manipulation of the power system equations using the impedance vectors, Zs, ZL and Rf, and the relaying equations utilising the setting vector Zr. Although not specifically stated such analysis assumes that the relaying equations are valid for all values of voltage and current, no matter how small or how large they may be. The resulting equations are often recognised by inspection to be either in the form of circles or straight lines, hence it is possible to construct the theoretical characteristic onto an impedance diagram. Experience has shown that these techniques work, therefore any objections raised must be restricted to areas other than plain feeders.

The author believes that these techniques have an inherent shortcoming when they are used without modification on series compensated lines. The major point is that the capacitor overvoltage protection is a non linear function, which is very sensitive to the actual level of voltage. Any method that deals with only the ratio of V/I and throws away the values of the voltage and current cannot be expected to succeed. Consequently to advance the analysis of series compensated lines, any new method must incorporate a means of retaining the actual voltages and currents, thus allowing a continuous inspection of the state of the capacitor overvoltage protection. Only as a final step, should the voltage be divided by the current, to arrive at the effective impedance.

IMPROVED STEADY STATE MODELLING

To develop an improved steady state model of the series capacitor and its varistor overvoltage protection, the model of Fig. 1 was employed. The scope of this paper is restricted at present to 3-phase faults, consequently a single line representation is adequate. The power system behind the capacitor is represented by a single equivalent infeed represented by X and R of the source. The only other elements in this part of the analysis are the capacitor and its parallel overvoltage limiting metal oxide varistor. To minimise the complexity, it was assumed that the overvoltage clamping was perfect, i.e. the varistor maintained an infinite impedance below its threshold, and had zero slope resistance once the voltage reached the threshold. The varistor protection level, despite being a true voltage function, is normally quoted as the capacitor current level, in fundamental frequency RMS amperes, at which the varistors trigger to by-pass the capacitor bank. The driving emf was a sinusoidal supply of fundamental frequency and one per unit magnitude. At this stage all the parameters were kept as variables.

Using a personal computer, a numerical technique based on solving the differential equations by incrementing time in infinitesimal steps was employed. This method is similar to the principles used in EMTP analysis. The output was in the form of the instantaneous voltage across the capacitor and the loop fault current. Although the point on wave of starting the fault was variable, it was of no consequence, since to obtain the best steady state figures the program was run for 11 electrical cycles.

This ensured that all short term transient effects had been dissipated. By dealing with instantaneous voltages, it is easy to check each time through the computer program loop whether the capacitor voltage has exceeded the varistor by-pass level. When it is found to occur, the differential equations are modified to represent the extra parallel conduction path around the capacitor. When the capacitor voltage returns below the varistor threshold, the original differential equations are reinstated. It is assumed that the varistor switches in and out of circuit, in line with the instantaneous voltage, without any observable delay mechanism. A one cycle window of results for further analysis was triggered at the end of the 10th cycle. A second part of the computer program then completes a Fourier analysis on the one cycle set of results, to yield the fundamental frequency components of voltage and current, with their angular references, as well as the RMS values for comparison. The program was organised to run a range of bus fault levels to enable a family of results to be given.

In all cases, the source of data input was taken from practical power system parameters, including data from actual 230KV, 345KV, and 525KV series compensated systems. An example of the type of result obtained is given in Fig. 2. The instantaneous voltage and current are plotted for one case study, the data for which is given in the appendix. The waveshapes show that the most distortion occurs in the voltage, while the current clearly maintains its sinusoidal shape. The results of the Fourier analysis, shown lower in the frequency spectra of Fig. 2, confirm this.

Initially, many of the data input parameters were varied and the program rerun in the belief that the results would show a heavy dependence on such things as the X/R ratio of the source, the size of the capacitor, or the by-pass level of the varistors. This argument was not substantiated. Instead it was found that the results were remarkably uniform if expressed in per unit terms; the important reference parameter being the nominal current rating of the varistor overvoltage protection expressed in fundamental frequency rms amperes. An example set of results is tabulated in Table 1 in actual impedance terms; and then in per unit terms in Table 2. The claim for uniformity of the results is further substantiated by Reference 1), which has taken a very similar, although not identical, approach.

The complete set of results can be assembled onto diagrams in one of two ways. The first method is to plot a graph of the results of the effective series capacitance and the effective series resistance against the variable of fault current. This has been done in Fig. 3. This method is useful for further numerical reference. The same results can be plotted onto an X-R diagram, as shown in Fig. 4. Here a much more definite pattern can be seen, the results falling very close to the arc of a circle. Below the varistor triggering level, the impedance of the capacitor proves to be as expected, its nominal value. As the current is raised, the varistor begins conducting and introduces a resistive element into the equivalent series impedance. This resistance represents the heat dissipated inside the varistor. Increasing the overall fault current further, the varistor conducts for a greater proportion of the cycle, and as a result the effective capacitance falls. An interesting observation is that when the fault current is twice the varistor by-pass level, then the effective capacitance has fallen to one half of its nominal value.

One practical aspect that is not covered is the thermal modelling of the varistor. It is known that to avoid overheating and possible damage to the varistors, a by-pass circuit breaker is switched in when the varistor temperature has reached the design threshold. This is done at the correct instant of time by the thermal control circuitry. In general, the by-pass circuit breaker will only trigger when the fault levels are at their highest, or when a delayed clearance of the fault current occurs. The author has taken the view that for high speed line protection, the probability is that the operating time of the distance protection would lie within the time to trigger the by-pass circuit breaker. On this basis it can be ignored. Reference 1) has, however, taken this into account.

PRINCIPLE OF CURRENT BOOST

Because the above analysis began with a bus fault level, i.e. the fault level without the capacitor in circuit, it is possible to examine the degree of fault current boost that the capacitor introduces. Again, it is best expressed in per unit, relative to the varistor protection level in amperes. The results have been plotted in Fig. 5a, and show that the maximum current boost that the capacitor can give to the fault level is the order of 85% of the varistor by-pass rating in amperes. Notice that this only occurs at relatively high fault levels. This observation can form the basis of a useful "rule of thumb". If a Busbar has a fault level of 12KA, and there is a capacitor installation at the terminals of an out-going line with varistor protection rated at 4KA, then we know by inspection that the close-in line fault level will approach, but not exceed the sum of these two figures, i.e. 16KA.

Because the historical approach of the protection engineer has tended to ignore the voltage limiting elements fitted to the capacitors, it is useful to compare the actual current boost derived above, with the hypothetical figure assuming no voltage limiting. The results are compared in Fig. 5b. Clearly, there is no resemblance between the two curves. This adds further weight to the argument that the theoretical resonances that would result from ignoring the capacitor overvoltage protection, do not occur in practice.

EXAMPLES OF PRACTICAL SERIES COMPENSATED LINES

Not all series compensated lines are identical. The major variables for the protection engineer are the degree of compensation, the capacitor position and whether it is split in two parts, the type of overvoltage protection, its operating level and the location of the relay measuring transformers. The variation in the length of the line is a less important variable. It can be useful to investigate the statistics of actual installations of series compensated lines, and to derive a typical, or average line. The author has details of 24 installations in N. America. This information yields the average length of series compensated line to be 220Km, with an average positive sequence impedance of 85 ohms.

To ensure coverage of the major variables, three examples have been chosen for further analysis. These cover the mid-line compensated scheme plus two examples of line end compensation. The difference in the latter two being the location of the voltage measuring transformer. It appears that several utilities prefer to measure the line side voltage in preference to the bus side voltage. The capacitor overvoltage protection is taken as the more modern metal oxide varistor type. These are known to possess several advantages, especially with regard to fast re-insertion times of the capacitor bank following a major fault incident on the power system. Because of these inherent advantages, the usage of the varistor overvoltage protection is expected to increase and become standard practice on most new installations. The three examples are shown schematically at the top of figures 6, 8 and 9.

CALCULATION OF IMPEDANCES SEEN

Where distance protection is to be applied to series compensated lines it is important for the protection engineer to have an insight into exactly what impedance loci will be presented to the relay for internal faults. This can be demonstrated by making use of the results of Fig. 3. The requirement is to plot the impedance seen at the measuring location for a variety of 3 phase short circuit faults located at various points along the line. To extend the impedance chart, a variable fault resistance within the range 0 to 40 ohms is to be added at each fault location. For the first example, the results will be re-calculated for 5 different values of source impedance, ranging from the highest fault level anticipated, to a relatively weak in-feed.

The non-linear nature of the effective capacitor impedance, varying as it does with the fault level, demands an iterative solution. A numerical technique, based on a personal computer has been employed. Experience has shown that the best method of iteration is to begin by ignoring the capacitor thus gaining a first estimate of fault current. The look-up table is then used to insert the effective series capacitance and effective series resistance of the capacitor and its varistor protection for that current level. The second estimate of fault current is then calculated, taking the effective capacitor bank impedance into account. This loop is continued until two sets of results are within a close margin. The two figures had to lie within 0.5% before an output result was taken.

To maximise the visual impact of the display, the X-R diagrams have been plotted with lines of constant fault location, these being the approximately horizontal lines, plus lines of constant fault resistance, these appearing as near vertical lines. The grid approach allows any twisting of the matrix to be clearly visible. The results of this exercise are plotted in figures 6, 7, 8 and 9.

COMMENTS ON THE IMPEDANCES SEEN

The conventional approach to applying distance protection to series compensated lines, is to assume that the impedances seen are pushed vertically downwards towards the capacitive region by an amount exactly equal to the capacitive reactance. This effect occurs at the point where the capacitor is encountered. Fig. 6 shows that this approach can be conditionally valid. With a source impedance of 80 ohms and a series capacitor of 18 ohms reactance, the results follow this expectation, by stretching from -18 ohms to +42 ohms in the reactive axis as the fault location sweeps the line length of 60 ohms. Further, this remains true even when fault resistance is added. In fact all the impedances seen in Fig. 6a fall into parallel paths. The reason for this is that the maximum fault current is severely limited, being the order of 4000A, restricting it beneath the varistor protection of 5600A. A linear solution in this limited case is therefore to be expected.

It is when the fault currents result in capacitor voltages which exceed the varistor protection that the solution turns non-linear. This can be illustrated by figures 7a, 7b, 7c and 7d. The maximum fault current progressively increases through these figures. The impedances seen begin to twist and generally contract, especially when the fault level is at its highest. In Fig. 7d, the loci for solid faults is condensed into a range of approximately -1 to 44 ohms, instead of the 60 ohm spread initially expected.

In the second example, Fig. 8, the capacitor has been moved to the centre of the line, an approach which is favoured by several Canadian Utilities and also by Scandanavian manufacturers. To keep the display clear, the number of grid lines has been reduced. The results for the first 50% of the line produce a linear parallel matrix, as expected. Beyond the capacitor the discontinuity in the impedance seen becomes very apparent.

For the third and final example, the end compensated scheme is shown with a split location of current and voltage measuring transformers, see Fig. 9. The origin of this technique appears to lie in the United States. The impedances seen for line faults show no distortion, even though the strongest fault level has been used. In fact, the results are identical to those expected for a plain feeder. This highlights one of the prime advantages of this scheme. The capacitor is effectively part of the source impedance, and as such, does not come into the expression for forward faults.

IMPLICATIONS FOR DISTANCE RELAYS

This new technique of plotting the impedances seen for series compensated lines goes a significant way forward in offering a theory to explain the good practical results found during recent laboratory tests. The relay type under test being the memory cross polarised mho characteristic. The nature of the polarised mho relay element expanding as it does to cover forward capacitive faults, seems well suited to cover the results of figures 6, 7, 8 and 9. It is noticeable that the degree of capacitive coverage required in Fig. 7 to guarantee relay operation for forward short circuit faults goes down significantly as the source fault level increases. This is directly in line with the established theory for the cross polarised mho element.

IDEAS FOR FURTHER DEVELOPMENT OF THE TECHNIQUE

Although the results of this paper will be interesting to the protection engineer applying distance protection to series compensated lines, it is obvious that further work is yet required. The main task has to be to calculate the relay's response to the voltages and currents derived from this analysis, and to superimpose the region of operation of the protection on top of the impedances seen. It is hoped to report the outcome of this extended work in a future paper.

CONCLUSION

The major objective of this paper has been to show that by adopting an improved steady state model of the series capacitor, fitted with varistor overvoltage protection, it is possible to arrive at an effective series impedance for the capacitor installation, which takes into account the non-linear nature of the varistors. This formed the basis for calculating the impedances seen for faults on three examples of practical series compensated line. The results fit directly onto the conventional X-R impedance diagram.

The analysis has also established a generality of the effective series impedance of the capacitor installation when expressed in a per unit form. Reference 1) serves to confirm this observation. This means that engineers can use the results, in particular those of figures 3 and 4, without repeating the detail of the underlying fundamental work.

The protection engineer should seriously consider adopting this technique where distance relays are applied to modern designs of series compensated lines fitted with metal oxide varistors. The major benefit being that it offers a sound theory for representing the non-linear nature of the practical capacitor installation. This theoretical base is not available with existing techniques.

ACKNOWLEDGEMENTS

The Author wishes to acknowledge the support of GEC Measurements, Stafford, UK during the writing of this paper, and in particular, the contribution made by various Engineers within the Company.

REFERENCES

1. Daniel L Goldsworthy, "A Linearized Model for MOV-Protected Capacitors" IEEE/PES Summer Meeting, July 1986.

APPENDIX

The examples given in the figures have been selected to be representative of the typical series compensated line found in practical installations. Where engineers wish to repeat some of the calculations, the following additional data may be useful.

FIGURES 2 AND 5

These examples were calculated for the following parameters:-

E = 525 Kv RMS Zs = 1 + j27 ohms

Xc = j18 ohms Ibp = 5.6 KA RMS

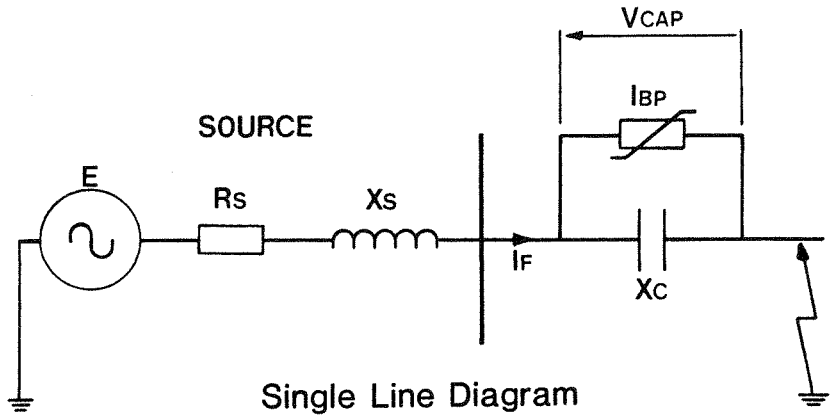
f = 60 Hz

BUS Fault Level (KA)	V Cap (KV)	If (KA)	Z Cap (ohm)	Z Cap (Deg)	
2.80	60.5	3.36	18.0	-90.0	Answers in Ohmic Values
3.36	75.6	4.20	18.0	-90.0	
3.92	92.0	5.11	18.0	-90.0	Nominal Reactance
4.48	105.7	6.07	17.4	-85.6	of Capacitor 18 ohms
5.04	110.6	6.87	16.1	-78.9	
5.60	113.6	7.62	14.9	-73.7	By-pass Level of Metal
6.72	117.4	9.06	13.0	-66.6	Oxide Varistor 5.6 KA
7.84	119.5	10.44	11.5	-61.3	
8.96	121.0	11.78	10.3	-57.2	System Frequency 60 Hz
11.20	122.7	14.36	8.5	-50.8	
14.00	124.1	17.51	7.1	-45.5	System Voltage 525 KV
16.80	125.0	20.62	6.1	-41.8	
22.40	126.0	26.63	4.7	-36.4	BUS Fault X/R 25
28.00	126.6	32.44	3.9	-32.3	
33.60	127.0	38.30	3.3	-29.9	
44.80	127.5	49.63	2.6	-25.8	

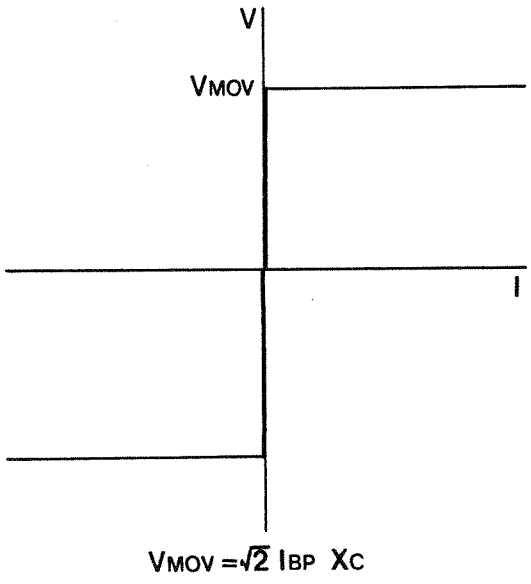
TABLE 1 - Effective Series Impedance of the Series Compensation Capacitor in Parallel with its Metal Oxide Varistor

BUS Fault Level (PU)	V Cap (PU)	If (PU)	X Cap (PU)	R Cap (PU)	
0.5	0.600	0.600	1.000	0.000	Answers in Per Unit
0.6	0.750	0.750	1.000	0.000	
0.7	0.910	0.910	1.000	0.000	
0.8	1.049	1.084	0.964	0.074	
0.9	1.097	1.227	0.878	0.172	
1.0	1.127	1.361	0.795	0.232	For Definition of
1.2	1.165	1.618	0.663	0.287	Per Unit Terms
1.4	1.186	1.864	0.560	0.307	See Figures 3 & 4
1.6	1.200	2.104	0.481	0.310	
2.0	1.217	2.564	0.366	0.298	
2.5	1.231	3.127	0.281	0.276	
3.0	1.240	3.682	0.226	0.253	
4.0	1.250	4.755	0.155	0.210	
5.0	1.256	5.793	0.116	0.183	
6.0	1.260	6.839	0.091	0.159	
8.0	1.265	8.863	0.063	0.130	

TABLE 2 - Effective Series Impedance of Series Compensation Capacitor in Parallel with its Metal Oxide Varistor



Single Line Diagram



Metal Oxide Varistor Model

Fig 1 Power System Models used for Analysis

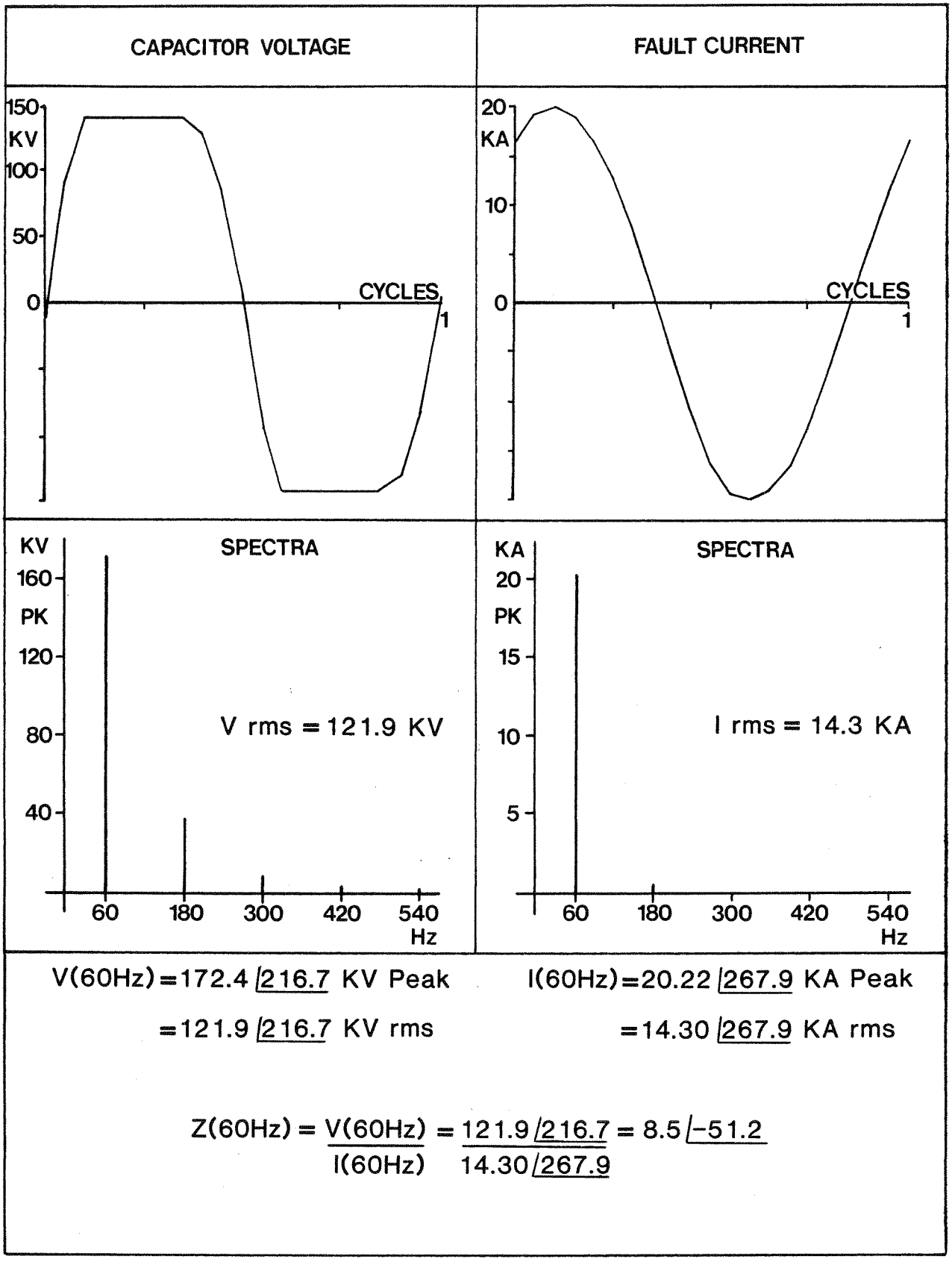


Fig 2 Example of Results of Transient Analysis

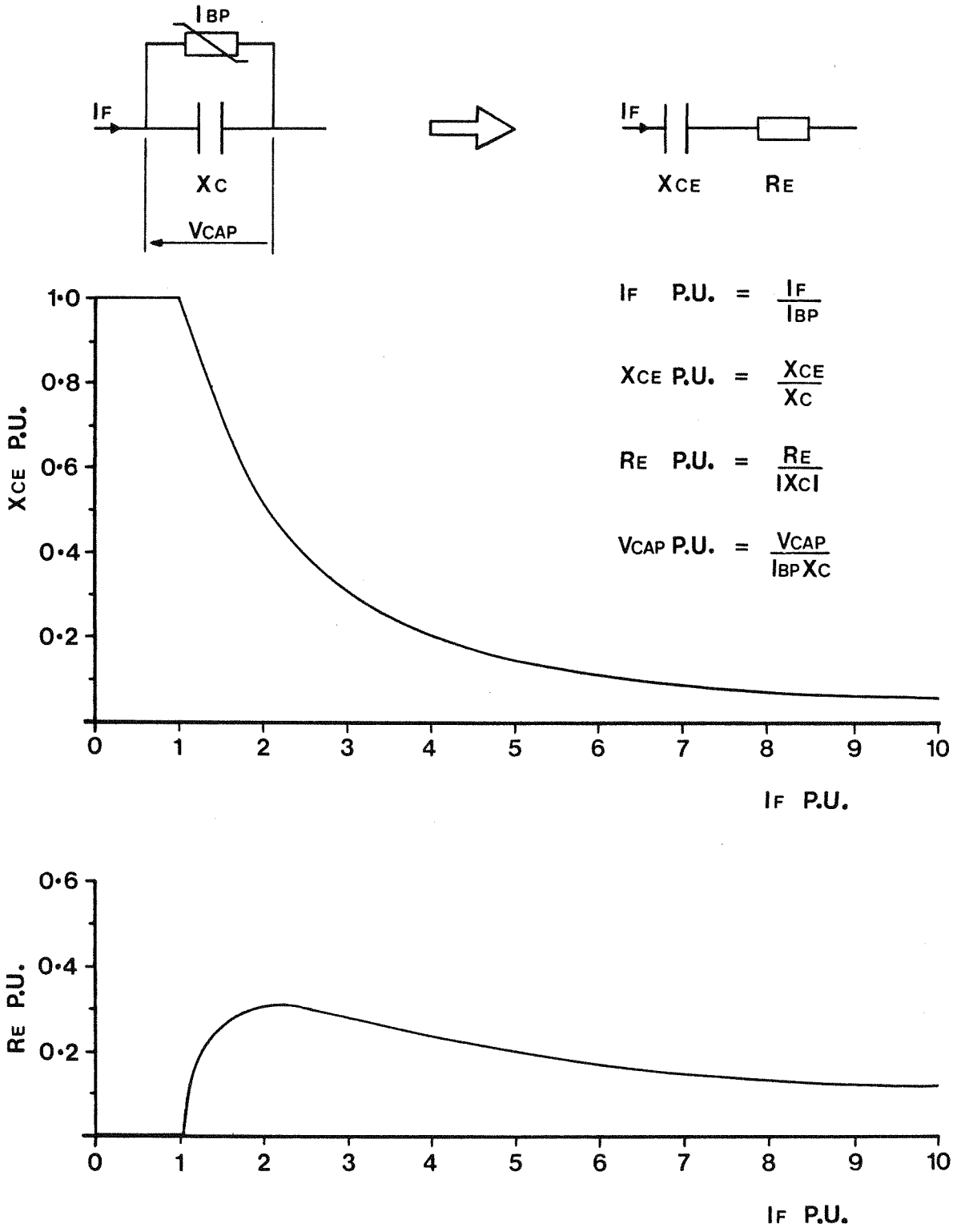


Fig 3 Equivalent Series Impedance of Capacitor with Varistor

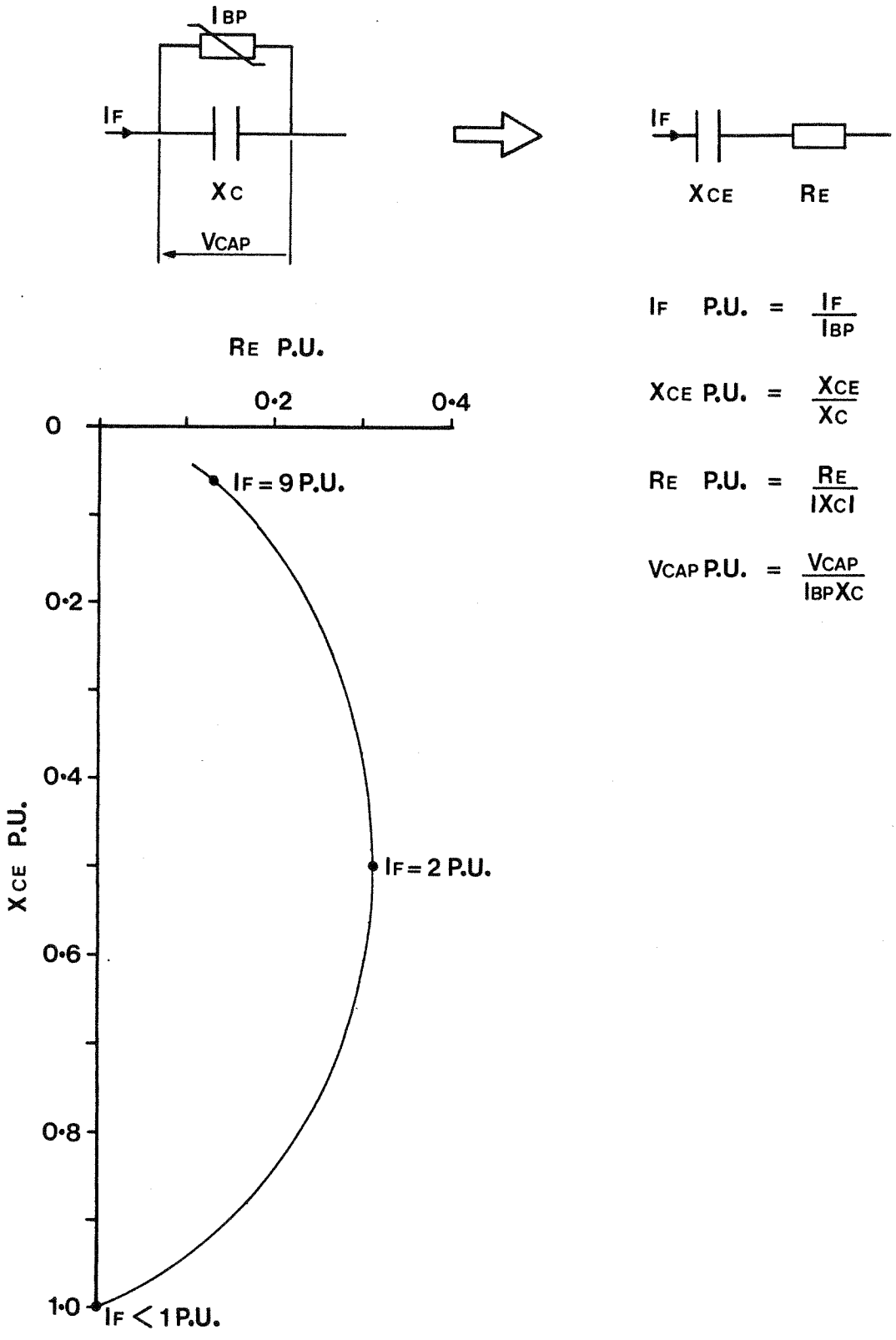


Fig 4 Equivalent Series Impedance of Capacitor with Varistor

Fig 5a

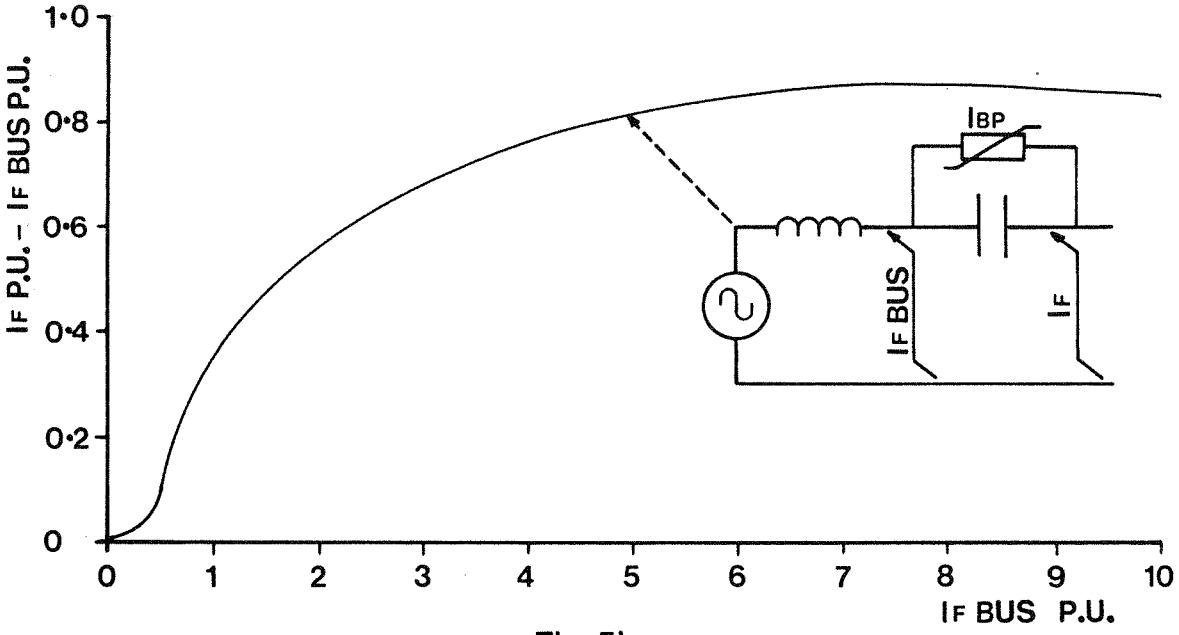


Fig 5b

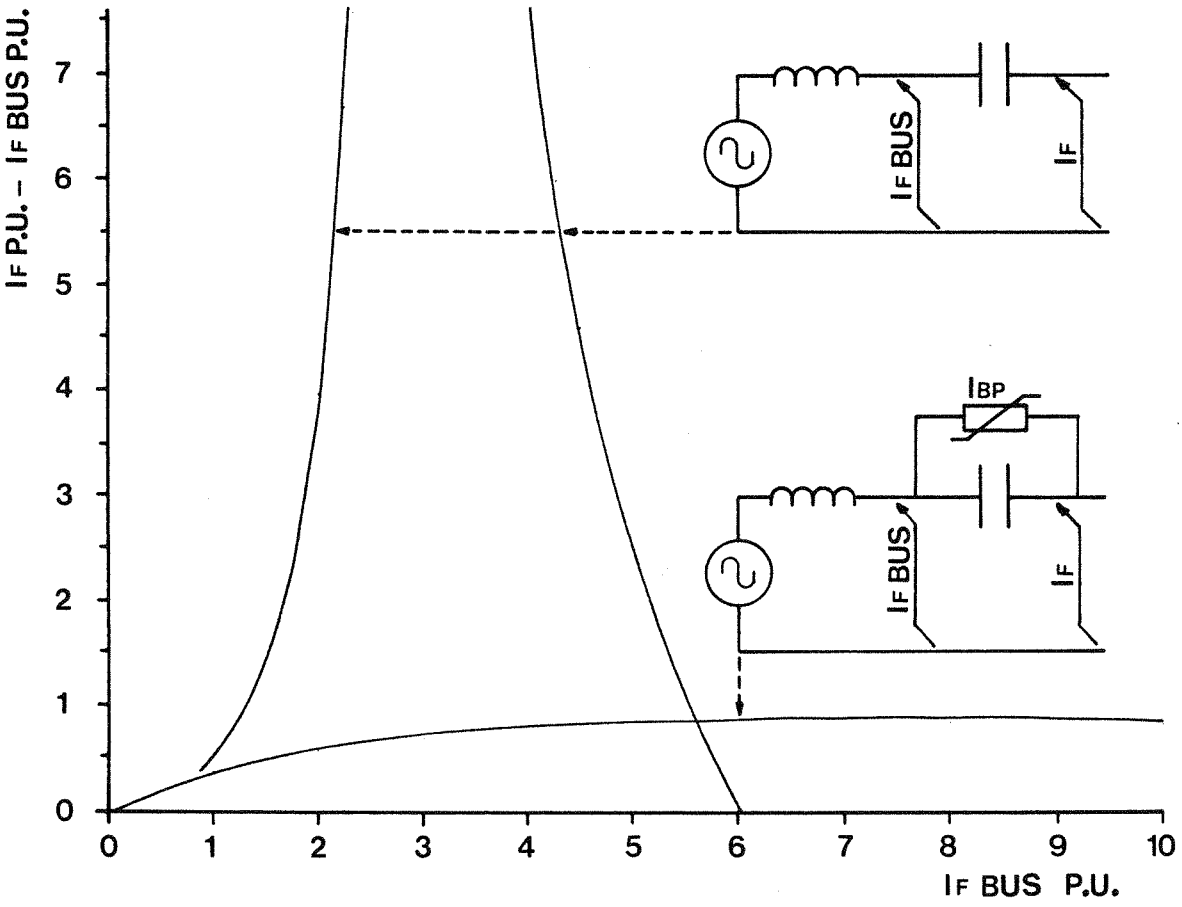
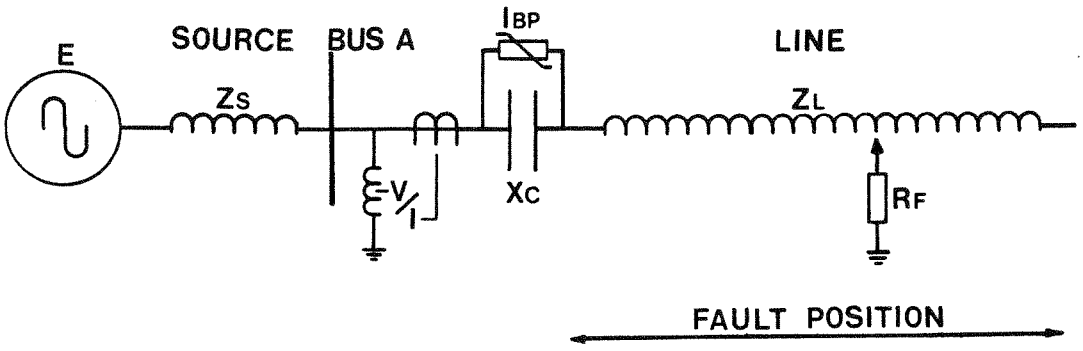


Fig 5 Diagram Illustrating Current Boost Created by Capacitor

Single Line Diagram



Impedances Seen at Measuring Location for Line Faults

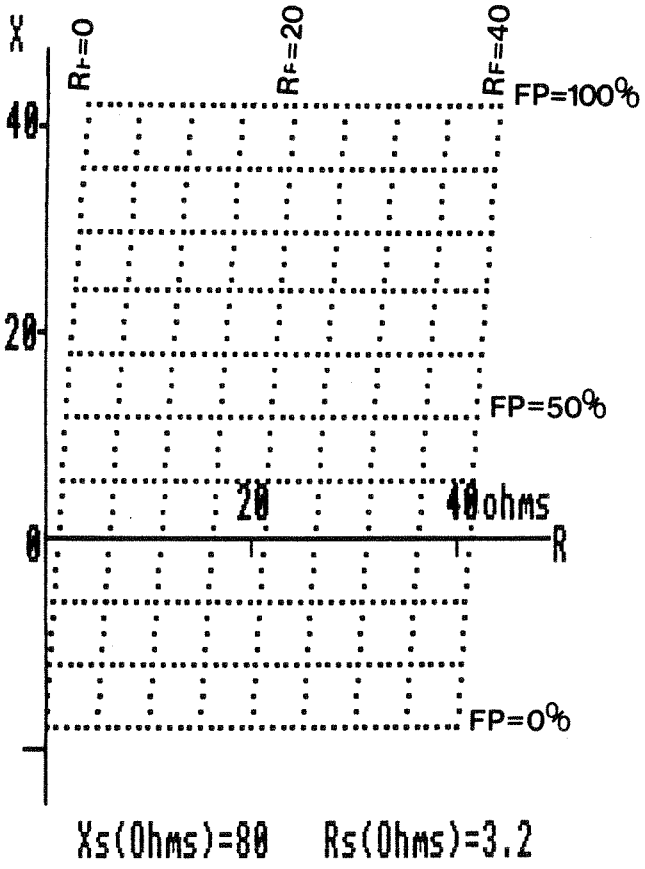
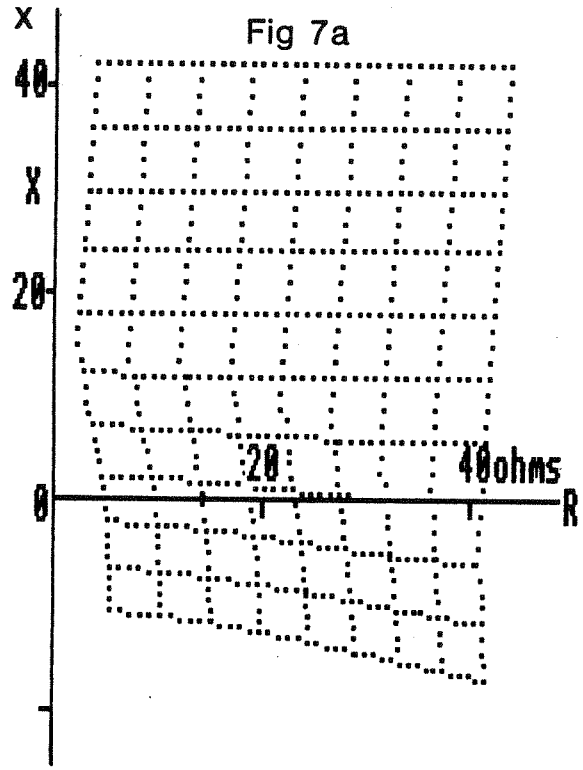
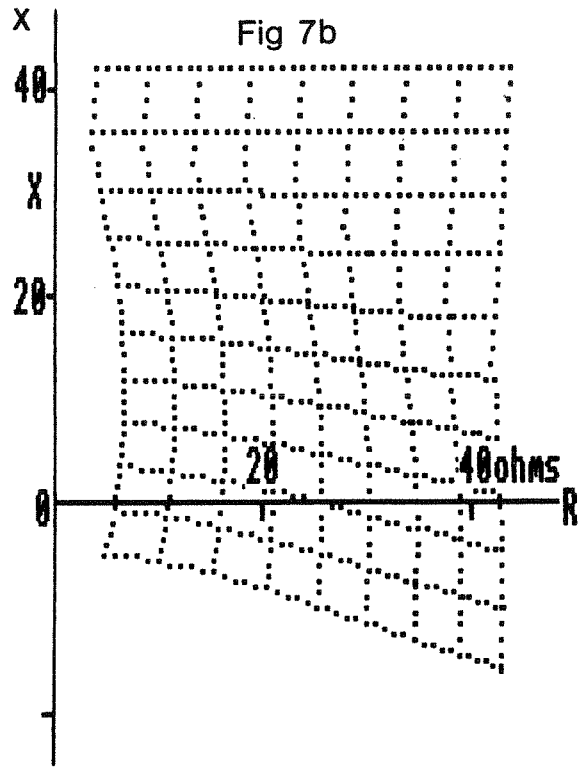


Fig 6 Line End Compensated Scheme

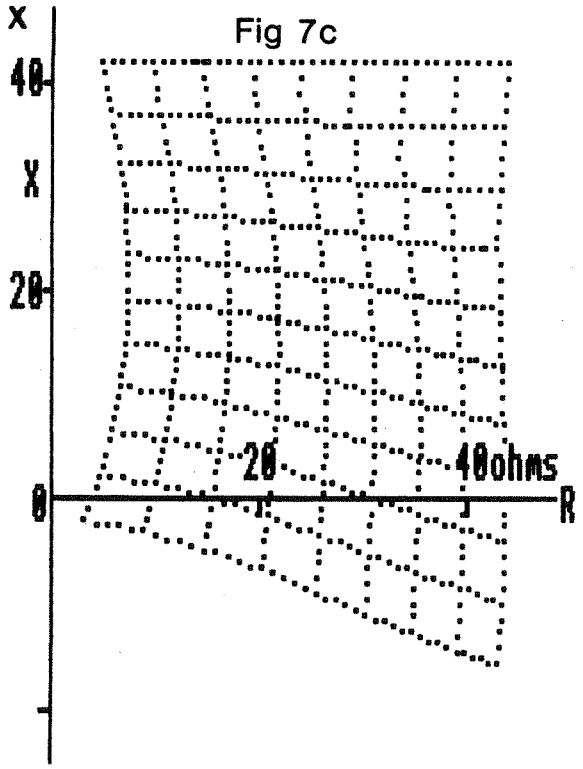
Example Plot with ZL=4 + j60, Xc=−j18, Ibp=5.6 KA, E=525 KV



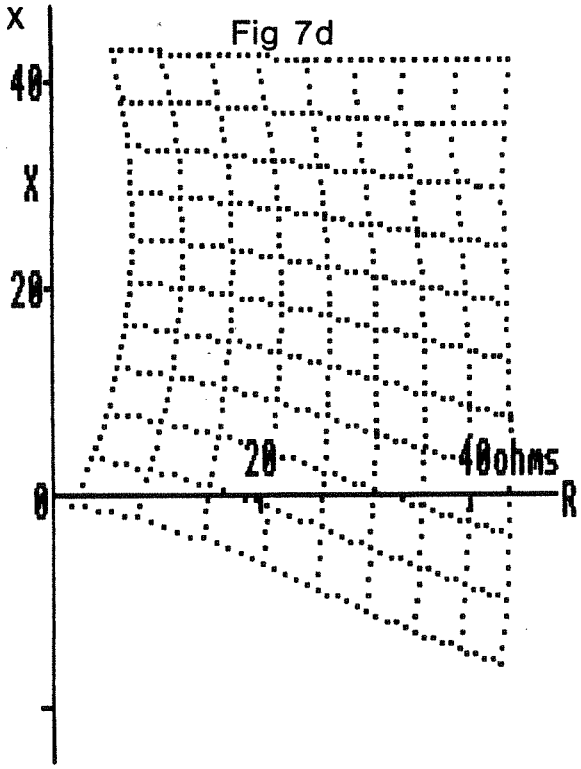
Xs(Ohms)=40 Rs(Ohms)=1.6



Xs(Ohms)=20 Rs(Ohms)=0.8



Xs(Ohms)=10 Rs(Ohms)=0.4



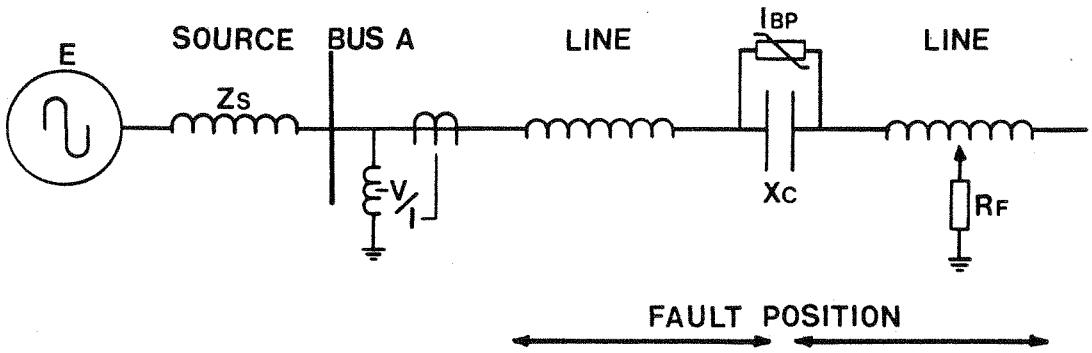
Xs(Ohms)=5 Rs(Ohms)=0.2

Fig 7 Line End Compensated Scheme

Details as Fig 6

Impedances Seen at Measuring Location for Line Faults

Single Line Diagram



Impedances Seen at Measuring Location for Line Faults

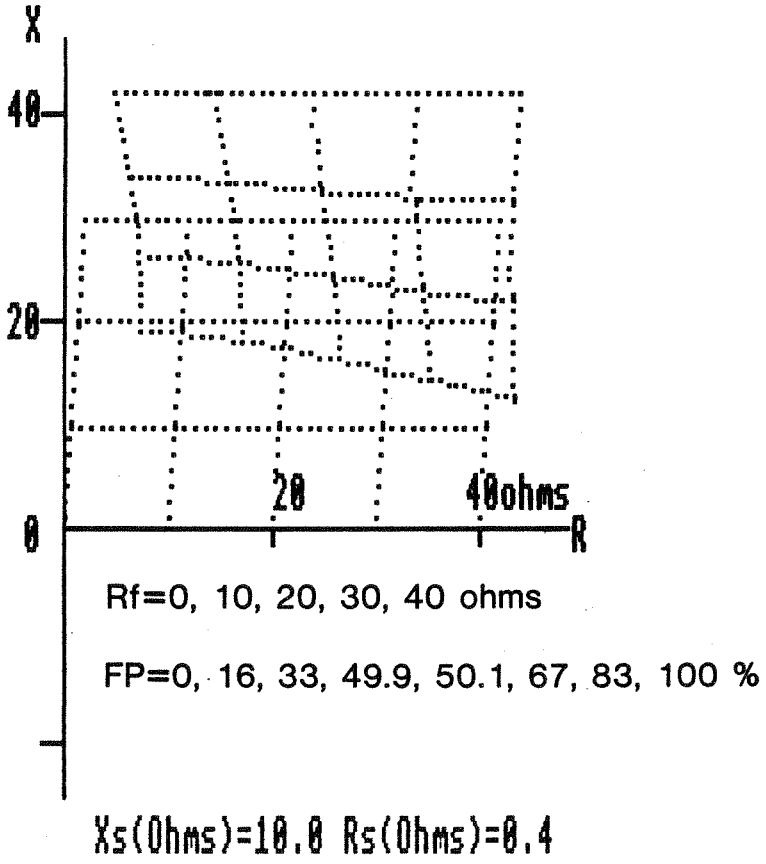
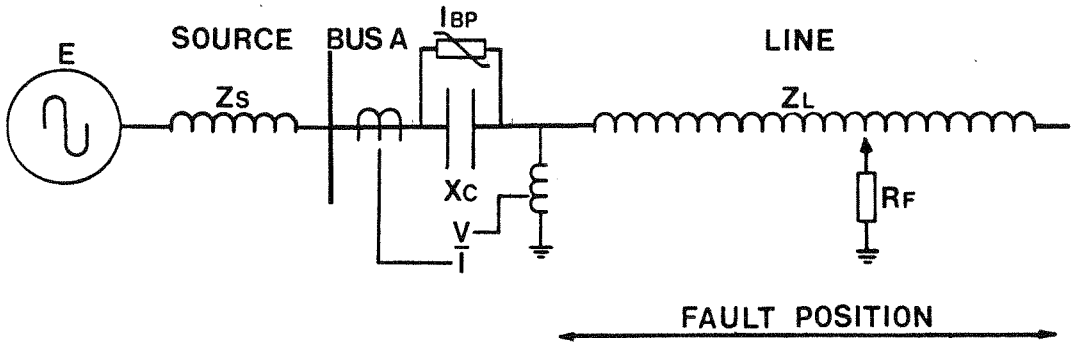


Fig 8 Mid-Line Compensated Scheme

Example Plot with ZL=4 + j60, Xc=-j18, Ibp=5.6 KA, E=525 KV

Single Line Diagram



Impedances Seen at Measuring Location for Line Faults

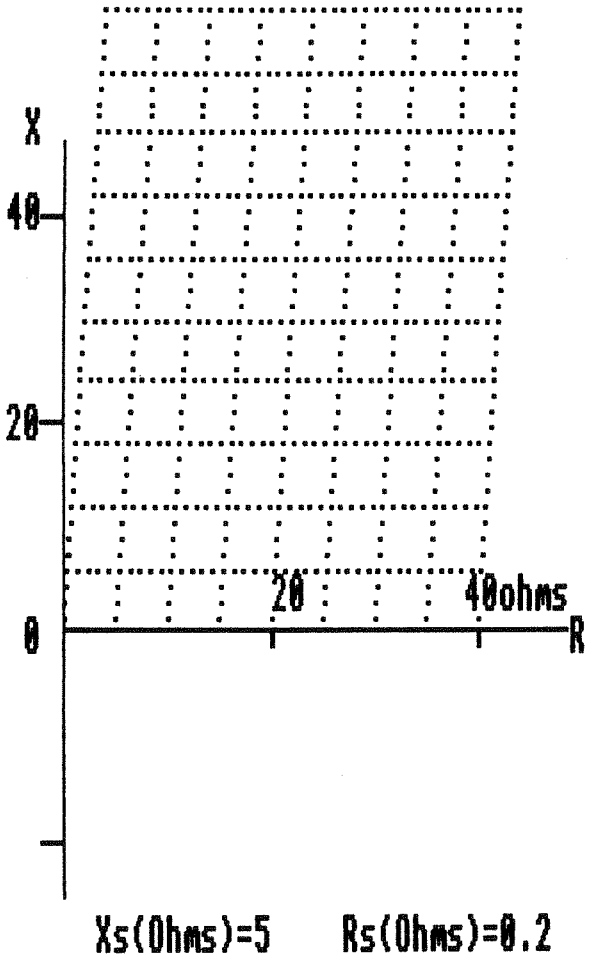


Fig 9 Line End Compensated Scheme with Split Measuring Locations

Example Plot with ZL=4 + j60, Xc=−j18, Ibp=5.6 KA, E=525 KV