SECONDARY TRANSIENT VOLTAGE PROBLEMS ON A 115 kV FUSELESS SHUNT CAPACITOR BANK

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Old Capacitor Bank Design (see figure 1):
Avista Corp (formerly Washington Water Power Co.), has applied 115 kV shunt capacitor banks for voltage support for over 25 years. The bulk of these installations has used two 24 Mvar banks. Each bank consisted of 5 series groups of 8 parallel 200 kvar, 13.8 kV capacitor units per phase. Each capacitor unit was fused with a 25T fuse. Both banks were fed from a 115 kV breaker with a Circuit-Switcher connected to the second bank. The capacitors were switched primarily by SCADA with voltage control as a backup. The protection normally consisted of time and instantaneous overcurrent for high magnitude faults. These relays were connected to the breaker CTs and tripped for faults in either bank. We also used voltage differential relays that tripped whenever the voltage became unbalanced across the 5 series groups and 1 of the groups had 110% or more voltage on it. The voltage relays usually compared the voltage across the last series group to neutral to the bus potential transformer voltage. The relay on bank #2 would trip the Circuit Switcher and on bank #1 would trip both the breaker and Circuit-Switcher. See figure 1.

The breakers used were originally oil breakers but these were replaced with SF_6 breakers in 1991 simply because the oil breakers wore out from overuse. Neither the oil nor the SF_6 breakers limit the voltage transients (such as with the zero voltage crossing method). As a result, we have experienced around 30 instances of a voltage transient being generated on the system and creating a line to ground fault where a line would be open. Sometimes we have had a microprocessor relay pinpoint the distance to the fault right at the open point. The Circuit-Switchers used either pre-insertion resistors or inductors and did not create any noticeable primary voltage transients.

New Capacitor Bank Design (see figure 2):
In 1998 Avista determined we needed about 100 Mvar of shunt capacitor banks in downtown Spokane. We studied several different designs and sizes of capacitor banks and had an Electromagnetic Transients Program (EMTP) study run to determine a design that would minimize the primary voltage transients. We finally decided to use two 50 Mvar fuseless capacitor banks. Each bank consisted of 7 series groups of 4 parallel 600 kvar, 9.96 kV capacitor units per phase. Even more significant than the fuseless design is the fact that we used one SF_6 breaker to connect to two independent Circuit-Switchers feeding to the capacitor banks. That means the breaker will only be operated for faults and won't be used to do any capacitor bank switching. All of the switching would be handled by the Circuit-Switchers and these were equipped with pre-insertion inductors with 40 mH inductance and 81 ohms resistance. This will eliminate or at least limit any primary voltage transients when the capacitor is switched on. The primary switching is again from SCADA with voltage control as a backup. The capacitor banks went into service early in the summer of 1999.

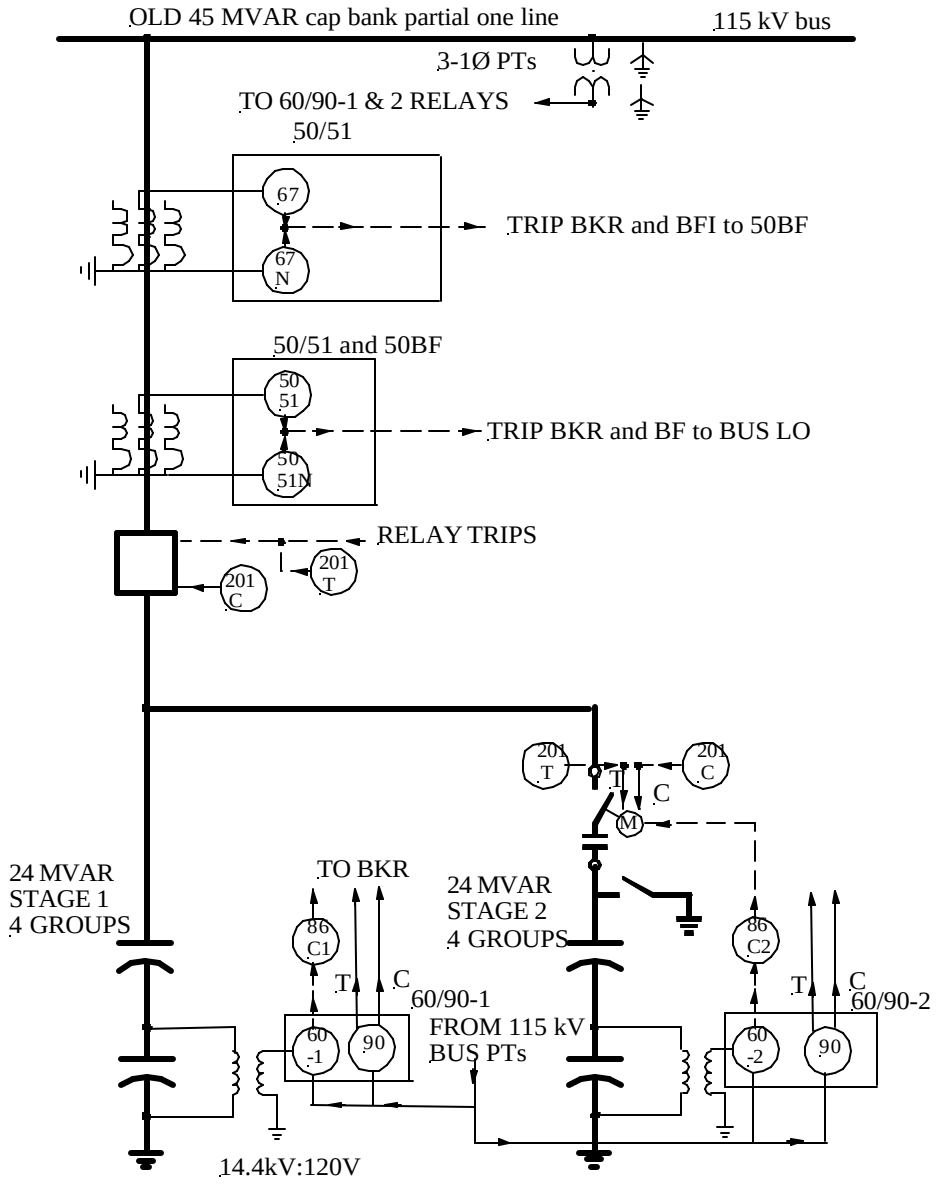

Figure 1. Old Shunt Capacitor Bank Design One Line.

New Capacitor Bank Design (continued)

There is time and instantaneous overcurrent protection on the breaker and voltage differential relaying on each bank. All relays are microprocessor based. Since each bank is now independent, either voltage differential relay can trip its respective Circuit-Switcher and the other bank is unaffected. The voltage differential relays are comparing the bus potential voltage to the capacitor bank voltage. The voltage from each capacitor bank is from two paralleled 825 volt, 167 kvar capacitors connected in the neutral of each phase. There is about 480 volts dropped across these capacitors and there is then a 5:1 step-down PT that provides the voltage to the relays. The PTs are rated 1250/250 V,

75 VA as CL03 and have a 100 ohm resistor in the primary. They have a thermal rating at 30° C of 500 VA. The relay voltage correction factor between the bus PTs and capacitor bank PTs is 0.71. The relay differential (after ratio correction) is set for 1.96 V with 10 seconds delay and the high set differential is set for 2.5 V and 30 cycles delay.

Each capacitor bank is single point grounded but the ground points are connected to one another with 250 MCM copper cable and have several connections to the ground grid. The PT cables are rated 600 volt, single point grounded out at the capacitor banks, unshielded and are about 300 feet in length. They are enclosed in a TRENWA trench with other cables.

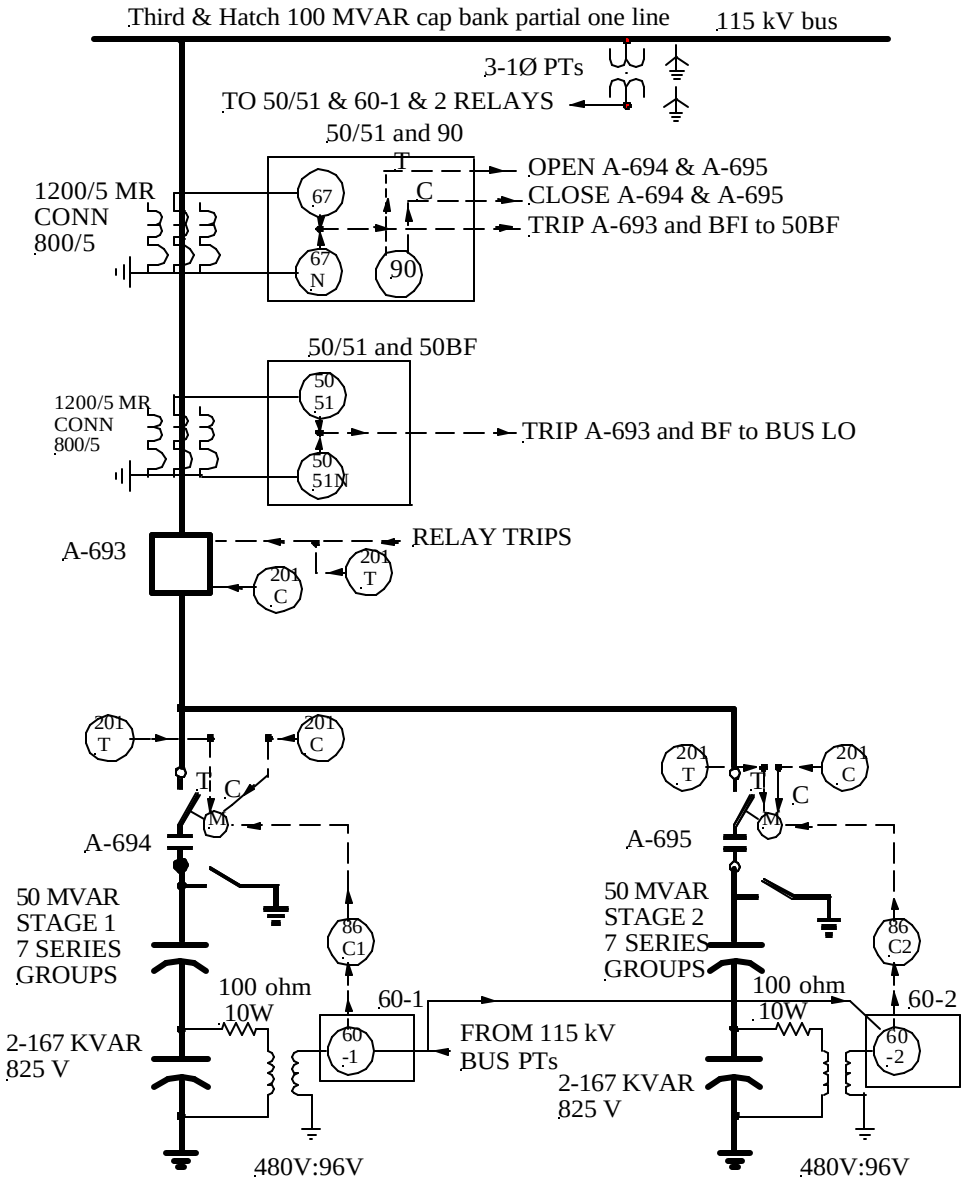

Figure 2. New Shunt Capacitor Bank Design One Line.

First Problem (see Figure 3):

We thought our voltage transient problems had been solved, at least until December 11, 1999. That morning I received a call from one of the System Operators. He said he had just closed in bank #1 and immediately tripped bank #2 which was already on line. I went to the office and called the voltage balance relay on bank #2. The event report showed zero voltage on phase A from the capacitor bank PTs. At the time we didn't know if the PT was opened, a fuse was blown or if something was wrong at the relay. When we investigated, we found that the A phase PT input to the relay was open. This is very unusual. We replaced the relay with a spare and sent the relay in for repairs. Of course we suspected voltage transients as the cause of the open input but wanted to wait for the manufacturer's report before we started anything. We got the relay back a few days later and the report stated that the problem was a possible 'component problem'. We placed the original relay back in service. We decided not to take anymore action at that time but promised to closely monitor the situation.

```
=>EVE 1

3HT/A-695/CAP2/         Date: 12/11/99    Time: 07:10:34.358

  Voltage PHASOR COMPONENTS, volts secondary      Relay Word      Outputs  Inputs
                                                                  TAAAAAA  RLRLEE
  VAX      VBX      VCX      VAY      VBY      VCY     R1R2 R3R4 R5R6  P12345L  EEEETT
                                                                           112212

 -14.25    62.91   -48.94     0.03    89.41   -69.47   0008 0000 83C0  .......  ......
 -64.72    20.03    44.53    -0.03    28.59    63.69   0008 0000 83C0  .......  ......
  14.31   -62.94    48.91    -0.03   -89.44    69.44   0008 0000 83C0  .......  ......
  64.69   -20.00   -44.56     0.03   -28.56   -63.72   0008 0000 83C0  .......  ......

 -14.34    62.97   -48.88     0.03    89.50   -69.41   0008 0000 83C0  .......  ......
 -64.66    19.94    44.59    -0.03    28.47    63.75   0008 0000 83C0  .......  ......
  14.38   -62.94    48.84    -0.03   -89.50    69.38   0008 0000 83C0  .......  ......
  64.66   -19.91   -44.63     0.03   -28.41   -63.78   0008 0000 83C0  .......  ......

 -14.44    62.91   -48.81     0.00    89.50   -69.34   0008 0000 83C0  .......  ......
 -64.66    19.91    44.66     0.00    28.34    63.84   0008 0000 83C0  .......  ......
  14.50   -62.94    48.78     0.00   -89.50    69.28   0008 0000 83C0  .......  ......
  64.66   -19.88   -44.69     0.00   -28.28   -63.88   0008 0000 83C0  .......  ......

 -14.53    62.97   -48.75     0.00    89.50   -69.25   0008 0000 83C0  .......  ......
 -64.66    19.84    44.72     0.00    28.25    63.91   0008 0000 83C0  .......  ......
  14.56   -63.00    48.72     0.00   -89.56    69.22   0008 0000 83C0  .......  ......
  64.59   -19.78   -44.75     0.00   -28.19   -63.97   0008 0000 C3C0  *......  ......

 -14.56    63.00   -48.69     0.00    89.59   -69.16   0008 0000 C3C0  *......  ......
 -64.59    19.72    44.75     0.00    28.13    64.00   0008 0000 C3C0  *......  ......
  14.59   -62.97    48.72     0.00   -89.59    69.13   0008 0000 C3C0  *......  ......
  64.63   -19.72   -44.81     0.00   -28.06   -64.00   0008 0000 C3C0  *......  ......

 -14.66    63.00   -48.69     0.00    89.59   -69.13   0008 0000 C3C0  *......  ......
 -64.59    19.69    44.88     0.00    28.03    64.03   0008 0000 C3C0  *......  ......
  14.69   -63.03    48.59     0.00   -89.59    69.09   0008 0000 C3C0  *......  ......
  64.59   -19.66   -44.84     0.00   -28.03   -64.09   0008 0000 C3C0  *......  ......

 -14.75    63.03   -48.59     0.03    89.63   -69.03   0008 0000 C3C0  *......  ......
 -64.59    19.63    44.88    -0.03    27.97    64.16   0008 0000 C3C0  *......  ......
  14.78   -63.03    48.56    -0.03   -89.63    68.97   0008 0000 C3C0  *......  ......
  64.59   -19.56   -44.94     0.03   -27.91   -64.19   0008 0000 C3C0  *......  ......

 -14.78    63.06   -48.50     0.03    89.63   -68.94   0008 0000 C3C0  *......  ......
 -64.59    19.50    44.94     0.00    27.88    64.19   0008 0000 C3C0  *......  ......
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```
 14.84  -63.09   48.50   -0.06  -89.69   68.94  0008 0000 C3C0  *......  ......
 64.56  -19.47  -44.94    0.00  -27.78  -64.22  0008 0000 C3C0  *......  ......

-14.91   63.09  -48.50    0.03   89.69  -68.91  0008 0000 C3C0  *......  ......
-64.53   19.47   44.97    0.00   27.72   64.28  0008 0000 C3C0  *......  ......
 14.91  -63.09   48.47    0.00  -89.69   68.84  0008 0000 C3C0  *......  ......
 64.53  -19.44  -45.00    0.00  -27.69  -64.34  0008 0000 C3C0  *......  ......

-14.94   63.09  -48.44    0.00   89.72  -68.78  0008 0000 C3C0  *......  ......
-64.53   19.38   45.03    0.00   27.63   64.38  0008 0000 C3C0  *......  ......
 15.00  -63.09   48.41    0.00  -89.72   68.75  0008 0000 C3C0  *......  ......
 64.50  -19.34  -45.03    0.00  -27.56  -64.41  0008 0000 C3C0  *......  ......

-15.03   63.09  -48.41    0.00   89.72  -68.72  0008 0000 C3C0  *......  ......
-64.47   19.34   45.06    0.00   27.53   64.44  0008 0000 C3C0  *......  ......
 15.06  -63.13   48.38    0.03  -89.75   68.69  0008 0000 C3C0  *......  ......
 64.44  -19.28  -45.13    0.00  -27.50  -64.47  0008 0000 C3C0  *......  ......

Event   :TRIP  TARGETS: EN,87A
```

Figure 3. Relay event report for December 11, 1999 Trip.

Second Problem:
On December 21, 1999 we again failed the A phase input to the same relay. The event report essentially looks identical to the one above on December 11, 1999. This time it was when we closed bank #2 with #1 already on. With this failure there was no doubt that we had a bad voltage transient problem and would have to solve it. We once again sent the relay in for repairs. This time the manufacturer gave us a replacement relay and they kept the old relay for further analysis. The failure cause was listed as a probable insulation breakdown on the primary winding wire due to an over voltage condition on the PT input. This caused the winding to fuse open.

First Monitor:
We needed a way to record what was happening when the capacitor banks were being switched. Earlier, we had placed a Digital Fault Recorder on the circuits but did not record any high voltage transients during switching because the sampling rate of the recorder wasn't high enough. We talked to our Power Quality Engineer who had a couple of recorders that were capable of recording fast transients. One was being used at the time but we were able to borrow the second one. This recorder was normally used to analyze harmonics but also had a feature that would plot and print out impulse voltages. However, it has a maximum voltage rating of only 2,000 volts.

We installed the monitor on January 10, 2000 and left it in service until January 28, 2000. We took various snapshots of the voltage at fifteen minute intervals and triggered the recorder on voltage going high or low. We only obtained a couple of impulse recordings and these were cut off at around 750 volts. Basically the recordings we were getting weren't telling us what we really needed to know.

In early February we went out to change some recorder parameters and do some testing. We made the changes and then closed bank #2 with bank #1 already on. We really didn't obtain a very useful record from that test either because we opened the C phase input to the recorder.

Second Monitor:
Fortunately, by this time the other recorder had become available. This recorder was rated for 6,000 volts and would provide good waveforms along with printed impulse magnitudes. The recorder has four channels and automatically adjusts the record to capture the highest transient. We installed this monitor on February 3, 2000. We were monitoring all 3 phases to neutral on bank #2 PTs and A phase to neutral on bank #1 PTs. We left the new monitor connected overnight and planned on going back the next day to do more testing.

February 4, 2000 Records:
At 5:32 AM on February 4th, the System Operators closed bank #2 with bank #1 already on. From this action we obtained some very good records. We measured severe transients on all 4 channels. Refer to Appendix A, Figures 1 through 6. The values were:

- A phase – neutral on bank #2 = -2247 V.
- B phase – neutral on bank #2 = -2532 V.
- C phase – neutral on bank #2 = -2081 V.
- A phase – neutral on bank #1 = 3132 V.

At 9:20 AM we opened bank #2 with bank #1 still on. We did this to monitor the transients when a bank was being opened. Refer to Appendix A, Figure 7. The values were:

- A phase – neutral on bank #2 = 167 V.
- B phase – neutral on bank #2 = 226 V.
- C phase – neutral on bank #2 = 160 V.
- A phase – neutral on bank #1 = -276 V.

At 9:22 AM we closed bank #2 again with bank #1 already on, which was the same action as at 5:32 AM. We obtained almost identical results as the close at 5:32 AM. Refer to Appendix A, Figure 8. The values were:

- A phase – neutral on bank #2 = -2194 V.
- B phase – neutral on bank #2 = -2632 V.
- C phase – neutral on bank #2 = -2102 V.
- A phase – neutral on bank #1 = 3139 V.

We then opened both banks. Then at 11:16 AM we closed bank #1 with bank #2 off. We again obtained severe transients but these were considerably smaller than with the back-to-back switching. However, we did measure transients on bank #2 which was open. Refer to Appendix A, Figure 9. The values were:

- A phase – neutral on bank #2 = -648 V.
- B phase – neutral on bank #2 = -780 V.
- C phase – neutral on bank #2 = -648 V.
- A phase – neutral on bank #1 = -2203 V.

Observations from the February 4, 2000 Tests:

- We experienced severe voltage transients on both capacitor bank PT secondary circuits every time we closed a capacitor bank.
- The most severe transients occurred on bank #1 when bank #2 was closed. Later, the most severe transient occurred on bank #2 when we closed bank #1.
- The transients experienced were more severe when the banks were closed back-to-back.
- When we switched back-to-back, the voltage transients were almost identical with identical switching.
- We experienced some transients when the Circuit-Switcher pre-insertion inductors were inserted but the worst transients occurred when the inductors were bypassed.
- We experienced 3 separate transients on every monitored conductor when each phase inductor was inserted and then bypassed even if the other bank was open.
- The first transient to occur during the bypass was always the most severe.
- There was only a small transient present when a capacitor bank was opened.
- Each inductor insertion was close (about 10 ms total time) but was random. For example at 5:32 AM the closing sequence was B, C, A and at 9:22 AM it was B, A, C. This is within tolerance and is no problem.
- Each transient lasted about 1.5 to 2.0 ms when the capacitor banks were switched back-to-back. When we energized just one bank, the transient lasted about 0.4 ms.
- The transients were of a high frequency that was difficult to measure.

Bus PT Tests on February 8th:

We went back to do more testing on February 8th because we never recorded any transients on the bus PT secondary. Since we were using the pre-insertion inductors, we felt we shouldn't be getting much of a transient on the bus PT secondary but we wanted to prove it. We left the first 3 channels connected to bank #2 but connected the 4th channel 'D' to the bus PT A phase. At 11:52 AM, we closed bank #2 with bank #1 off. We measured voltage transients on the bank #2 PTs but got a zero voltage impulse on the bus PT. Refer to Appendix A, Figures 10 and 11. We then opened bank #2 and closed it again a little while later again with bank #1 off. We still didn't get any impulses on the bus PT, but since the capacitor bank hadn't discharged yet, we obtained a distorted waveform on B phase on bank #2. Refer to Appendix A, Figure 12.

Observations from the February 8th Tests:

- We were not getting any voltage transients on the bus PT secondaries. This is very important since it means the transient problem is confined to the capacitor bank PT secondaries.

Steps to Solving the Problem:

After the tests of February 8th, we discussed several possible actions which included:

- Separating the banks (not practical).
- Adding 115 kV bus inductors ahead of each Circuit-Switcher.
- Adding MOVs to the primary and/or secondary of the PTs.
- Adding burdens to the PTs.

- Adding transient suppression in the form of secondary shunt capacitors and resistors.
- Contacting some manufacturers for advice.

We decided to contact some manufacturers for advice before proceeding. We wrote a letter outlining our circuits and what we had measured. We expressed our thoughts about possible solutions and asked if they had any other ideas about what to do. We sent the letter to two manufacturers. Basically the replies suggested that we could try some of the solutions we had already discussed such as adding burdens, secondary arrestors, bus reactors etc. and even had some suggestions on MOV ratings etc. However, these were all general suggestions and they would need to perform EMTP studies to determine the actual cause of the transients and the best way to mitigate them.

We decided we would contract with one of the manufacturers to perform the EMTP studies and recommend a specific solution to the problem. This would take some time however, so we approached the System Operators and asked if they could refrain from operating the capacitor banks for the next few months until a solution could be determined and put in place. The System Operators said they could leave the banks in most of the time and agreed to at least minimize the number of operations. We then started proceedings to contract for an EMTP study.

In late April I decided to check on the number of capacitor bank operations that had actually been occurring. I called the microprocessor relay on the breaker because it used an internal Sequential Events Recorder and was monitoring the Circuit-Switchers. I discovered we had 28 capacitor bank operations (open and close) in the last 63 days, but the worst part was that starting April 1st, we had at least one operation per day. I was afraid at that rate we would be damaging more equipment again shortly.

Temporary Solutions:
We decided we would have to take some type of action on a temporary solution until the EMTP studies could be completed and a final solution determined. We again discussed several options and decided we would simply add burden resistors to the PTs and test the circuit. If it lessened the transients to a level we thought we could live with, we would leave them in place. If it didn't lessen the transients, then we could try other methods. I did some calculations on the burdens and voltage drops and we decided to install 200 ohm resistors. At 96 V this would give us about 0.48 amps and the burden would be about 48 VA or 64% of the PT rating. I calculated the additional voltage drop to be less than the voltage differential setting of 1.96 V so we left the setting at 1.96 V.

The Setup and Test (See Figure 4):
We went to Third & Hatch and added the resistors to bank #1. We didn't add any resistors to bank #2 partly because we wanted to see any differences in transient magnitudes. We left the PT ground out at the PTs but we connected the monitor to measure A phase to neutral and also neutral to ground on both banks. We were sure we would detect almost the same transient from neutral to ground as from phase to neutral. We left bank #2 in service and then closed bank #1.

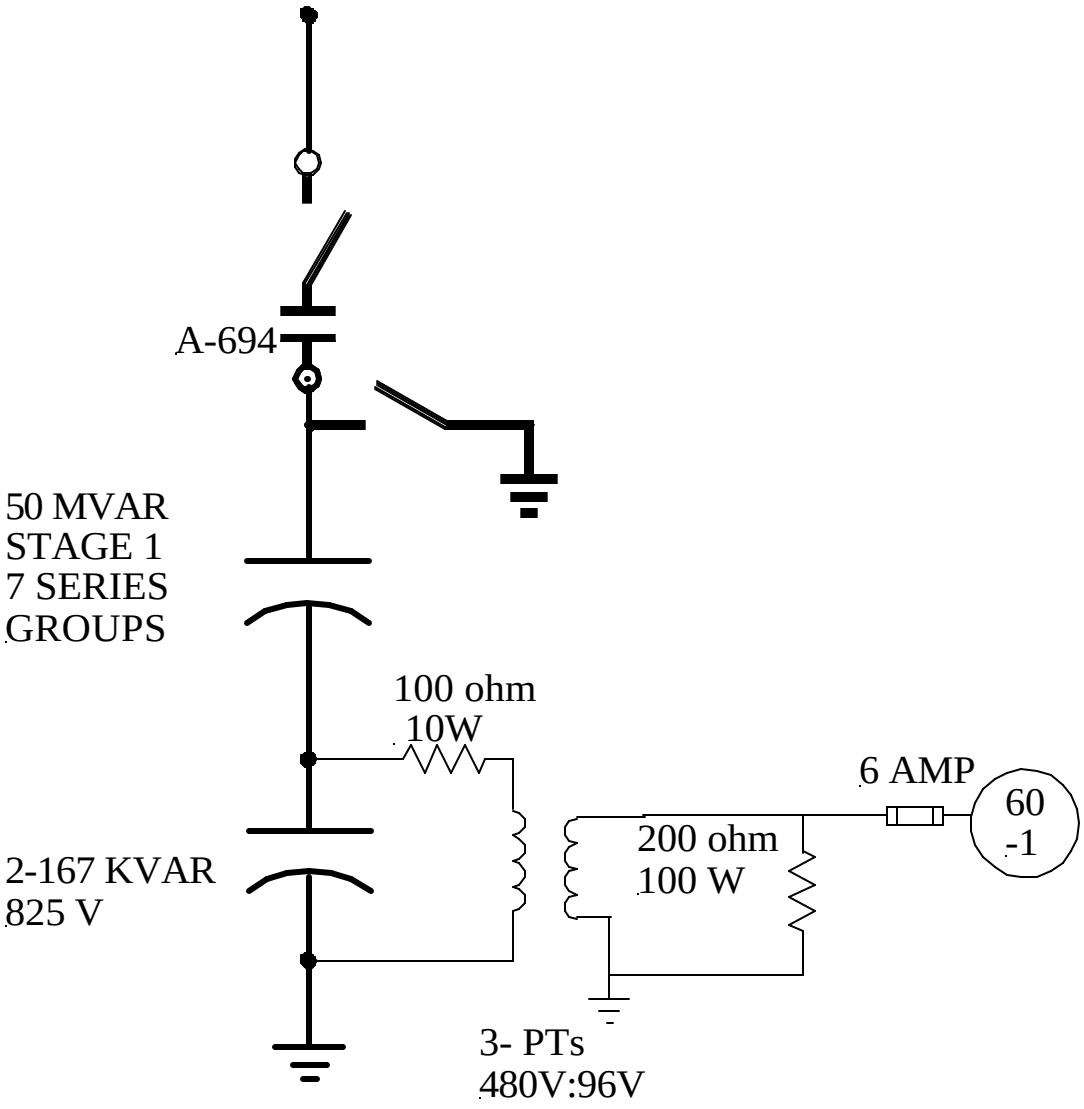


Figure 4. The 200 W Resistor Setup.

The Test Results:
We heard a 'POP' and bank #2 tripped quickly. Ten seconds later we tripped bank #1. We quickly removed the resistors from bank #1 and placed it back in service. When we looked at the equipment, we found that the A phase fuse had blown and the C phase input to the relay had opened on bank #2. Either of these actions would trip the relay by high set voltage differential. We then replaced the fuse and relay and placed bank #2 back in service.

Transient Recording Results (See Appendix A Figures 13 through 16):
When we looked at the transient recording results we discovered we had the following:

- A phase to neutral bank #1 = -2054 V.

- Neutral to ground bank #1 = 5089 V.
- A phase to neutral bank #2 = -5420 V.
- Neutral to ground bank #2 = -4704 V.

These were the highest voltages we had measured to date. It's no wonder we caused damage to the fuse and relay input on bank #2. It also confirmed that we were experiencing severe transients from neutral to ground in the panel house. When we looked at the bank #1 relay event report, we found a voltage difference of 2.07 volts while our setting was at 1.96 V. One of the Protection Engineers that worked for me recalculated the voltage drop and concluded that I had made an error in my voltage calculations so the trip was proper.

Observations from the Test Results:

- Adding a resistor burden alone on the capacitor bank PT secondary circuit did not reduce the voltage transients seen on that PT circuit at all. In fact the transients were the worst we had measured.
- The transients seen from neutral to ground were as severe as from phase to neutral.

Manufacturer's Temporary Solution Recommendation (See Figures 5 and 6):

The next day I called Terry Bellei at S&C, explained the situation and asked for a specific recommendation on what we could do for a temporary solution until the EMTP study could be completed.

- He said the 200 ohms of burden would probably have eventually burned up the PTs on bank #1 if we hadn't tripped it since the PTs are rated 250 V. We should use the rating of 76 VA÷250 V = 0.3 amps.
- He also recommended we install 1500 ohm burden resistors in parallel with 1.8 µf, 250 V capacitors to shunt the transient to ground. The capacitive reactance would be about 1÷(377*1.8µF) = 1474∠-90° Ω. The total PT burden from the surge suppression circuit will be about 1051∠-45° Ω. Starting with 480 V on the primary, the secondary current is: (480÷5)÷1051 = 0.091 Amps.
- The voltage split will be: 100 Ω (primary) with 1051∠-45° Ω (secondary). Reflecting the secondary impedance to the primary yields 100∠0° vs. 26275∠-45°. The voltage divider is: [100∠0°÷(100∠0°+26275∠-45°)]*480V = 1.82∠-45° primary. Reflect this to the secondary and the voltage drop is 1.82÷5 = 0.36 V. This is well below the relay differential pickup of 1.96 V.

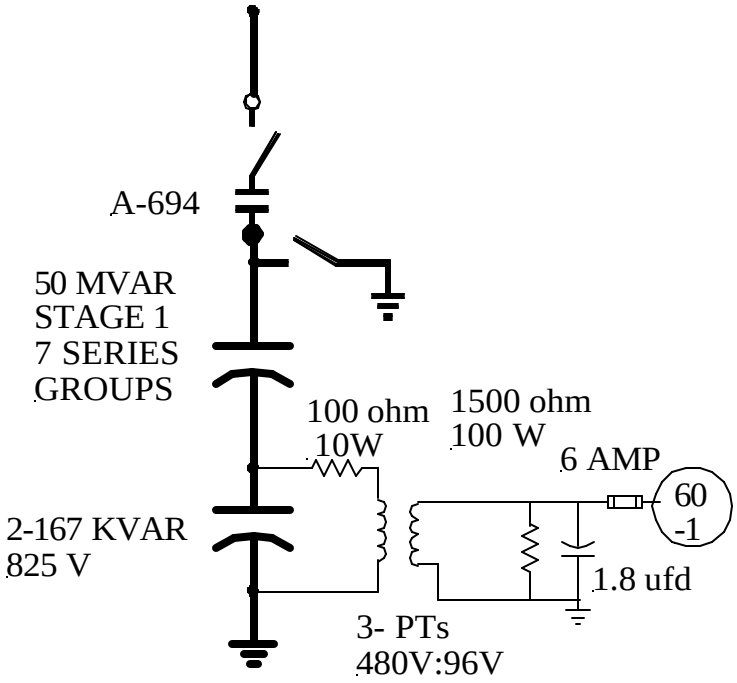


Figure 5. Surge Suppression Circuit and PTs Grounded in Panel House.

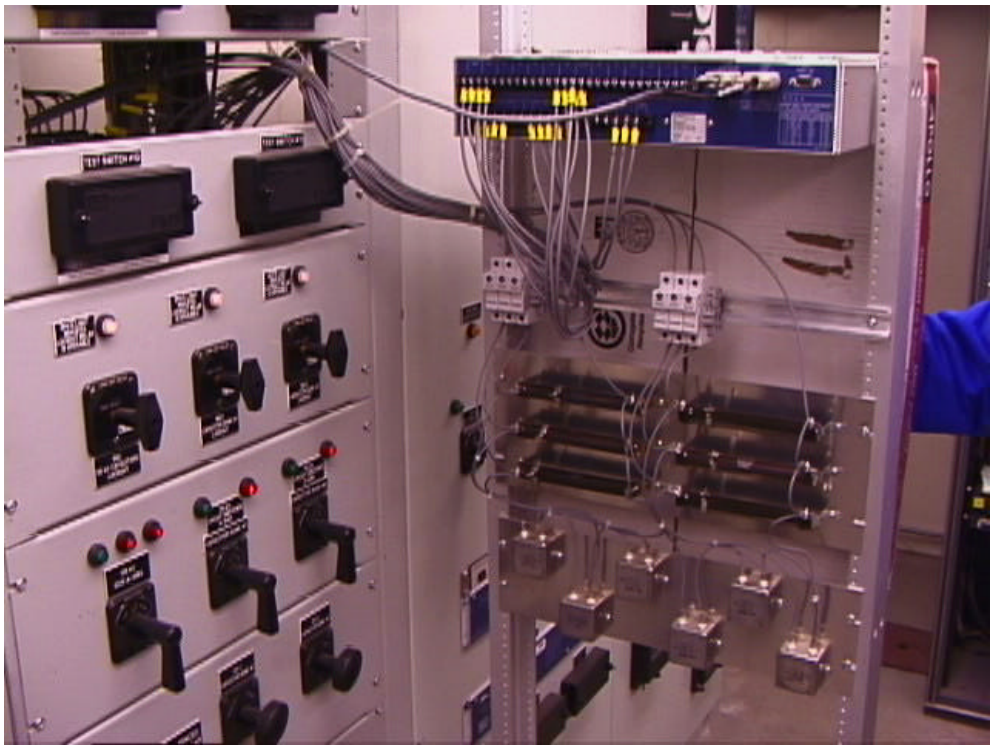


Figure 6. Resistor-Capacitor Surge Suppression Circuit.

The Next Test (See Appendix A, Figures 17 through 19):
On May 2nd we went back to Third & Hatch to perform additional tests. We connected the surge suppression circuits to both banks and moved the PT grounds into the panel house. We fused the surge suppression circuits separately from the relays. We again measured A phase to neutral and neutral to ground on both banks. We started with both banks open and closed bank #1 (see Appendix A, Figure 17). All we saw was a little bit of distortion from phase to neutral. There was no voltage impulse at all. Then we closed bank #2 with bank #1 already on (which would be the worst case). Again there was no voltage impulse. The transients were being completely shunted to ground and the voltage differential relays were protected. This of course still did not protect any equipment in the yard such as the capacitor PTs or the PT cables.

Test of the Old Capacitor Bank Configuration (See Appendix A, Figures 20 through 25):
We also wanted to see how bad the voltage transient problem was on our older capacitor bank configuration. On May 10, 2000 we moved the testing equipment to our Otis Orchards substation. We monitored A phase to neutral on the bus PTs, bank #1, bank #2 and neutral to ground on bank #1. Here we have to close bank #1 first with the breaker and then the bank #2 Circuit-Switcher. At Otis the Circuit-Switcher uses pre-insertion inductors and the breaker doesn't use any transient suppression. When we closed bank #1 we measured voltage impulses on each of the circuits as follows:

- Bus PT A phase – N = 244 V.
- Bank #1 A phase – N = -898 V.
- Bank #2 A phase – N = -720 V.
- Bank #1 neutral – ground = 2159 V.

This shows we also have a transient problem on the older configuration. However, these transients are not as severe as what we measured at Third & Hatch. As expected, we did measure an impulse on the bus PT secondary where there was no impulse at Third & Hatch. Also, the neutral to ground impulse was worse than any of the A phase impulses so the highest impulse actually occurred on either B or C phase.

When we closed the Circuit-Switcher to bank #2 we measured the following:

- Bus PT A phase – N = 0 V.
- Bank #1 A phase – N = -166 V.
- Bank #2 A phase – N = 244 V.
- Bank #1 neutral – ground = 876 V.

This shows that we still have impulses from the capacitor bank PTs (although considerably reduced), but the bus PT secondary doesn't have an impulse. This is consistent with the measurements at Third & Hatch and means there is no primary transient being created when we close with a Circuit-Switcher that uses a pre-insertion inductor.

Observations from the Test Results:

- There is a transient present from neutral to ground as well as from phase to neutral.

- The capacitor-resistor surge suppression circuit and grounding the PT secondaries in the panel house effectively reduced all capacitor bank PT secondary voltage transients to zero at that location.
- The older capacitor bank configuration also has a voltage transient problem.
- The transients on the old capacitor bank configuration are more severe when the breaker is closed.
- There is a transient on the bus PT secondary on the old capacitor bank configuration when the breaker is closed but not when the Circuit-Switcher is closed.

Protection Group Recommendations:

- That we keep the temporary surge suppression circuit at Third & Hatch at least until other voltage transient protection could be installed and proved.
- The relays will be the weakest link in the capacitor bank PT secondary circuit. Therefore, the priority of protection should have the relays first and then the 600 V cable and PT.
- Even though the Third & Hatch relays are now being protected by the surge suppression and are the first priority, the control cable and capacitor bank PTs could still be subjected to the transients and possibly damaged over time. Therefore, we still need to investigate the problem further until we are satisfied that this equipment is also protected.
- That we install the surge protection beyond the PT fuses to the relays. That way if the resistor or capacitor experiences a short circuit, the fuse will blow and we will trip the capacitor bank.
- That we make it a standard practice to ground all capacitor bank PTs in the panel house to reduce any possibility of high neutral to ground voltages in the panel house.
- That we conduct a study to determine if we wanted to make it a standard practice to ground all PT and CT circuits in the panel house. NOTE: This study has not yet been completed.
- That we contract with S&C to perform an EMTP study to maximize the surge protection. We contacted S&C and requested bids on performing EMTP studies for both the old capacitor bank configuration and the new fuseless capacitor bank configuration. Basically the questions we wanted answered were:
  - Where are the secondary voltage transients being started from?
  - What configuration, values, rating, materials, etc. for surge suppression do they recommend? This should be answered for the fuseless capacitor bank configuration and also for the older configuration.
  - Should we add any other protection such as MOVs?
  - If the surge suppression is placed beyond the PT secondary fuses to the relays, will the continued operation of the capacitor bank and subsequent voltage transient surge suppression deteriorate the fuse to a point that it could open falsely?
  - If the surge suppression is located in the panel house (as initially recommended), will the 600 volt control cable experience damaging voltage transients?

- Would it help the PTs and control cable to have surge suppression located out at the PTs in the switchyard? Would this be in addition to the panel house surge suppression?
- If we changed the control cable length, PT style, size of capacitor bank (and subsequently the voltage divider neutral capacitors) or placement in the Avista system, would this change the recommended surge suppression package? That is, would we need to change the package or run additional studies whenever we make changes to the bank?
- The existing PT control cable is not shielded. What would be the effect of shielding this cable?

The Contract:
In September 2000, Avista entered into two contracts with S&C whereby S&C would perform EMTP studies on the fuseless capacitor bank configuration and the older configuration. They would then provide recommendations on solving the voltage transient problems. These studies were both completed by March 2001.

EMTP Studies:
When back-to-back-connected capacitor banks are energized, severe inrush currents occur due to the discharge from the already-energized capacitor bank(s) to the bank being energized. If no transient mitigation is applied, these inrush currents can have magnitudes on the order of tens of kiloamperes, and frequencies on the order of tens of kilohertz. The very high rates of change of current can result in very high induced voltages in control and measurement circuit wiring if these are not properly shielded. Although pre-insertion inductors practically eliminate these transient inrush currents during insertion, the transient inrush currents that occur during bypass (when the pre-insertion inductor is switched out of the circuit) can be sufficiently large to create severe induced voltages in circuit wiring which is not properly shielded. Similar or more severe inrush currents will also occur with controlled closing circuit breakers closing within 1 millisecond of voltage zero or circuit breakers with pre-insertion resistors. The severity of the induced voltages will depend on the magnitude and frequency of the inrush currents involved, as well as the mutual coupling (inductive and capacitive) between the high-voltage circuit conductors and the control or measurement circuit wiring.

EMTP Equivalent Circuit Model:
In order to determine the source of the transients occurring in the PT secondary circuits during energization of the 115 kV, 50.4 Mvar capacitor banks at Third and Hatch Substation, an equivalent circuit of the substation was developed for EMTP simulation. See Figure 7. The equivalent circuit focused on the simulation of induced voltages in the PT secondary circuit of capacitor bank #1; therefore only the PT secondary circuit of this bank is included in the model. The three-phase equivalent circuit included a 115 kV source with source impedance and damping resistance in parallel, which represents the surge impedance of transmission lines connected to the substation bus. Also included in the equivalent circuit is an approximation of the substation load, bus inductances, capacitor bank equivalent capacitances, capacitances of the bank neutral voltage divider

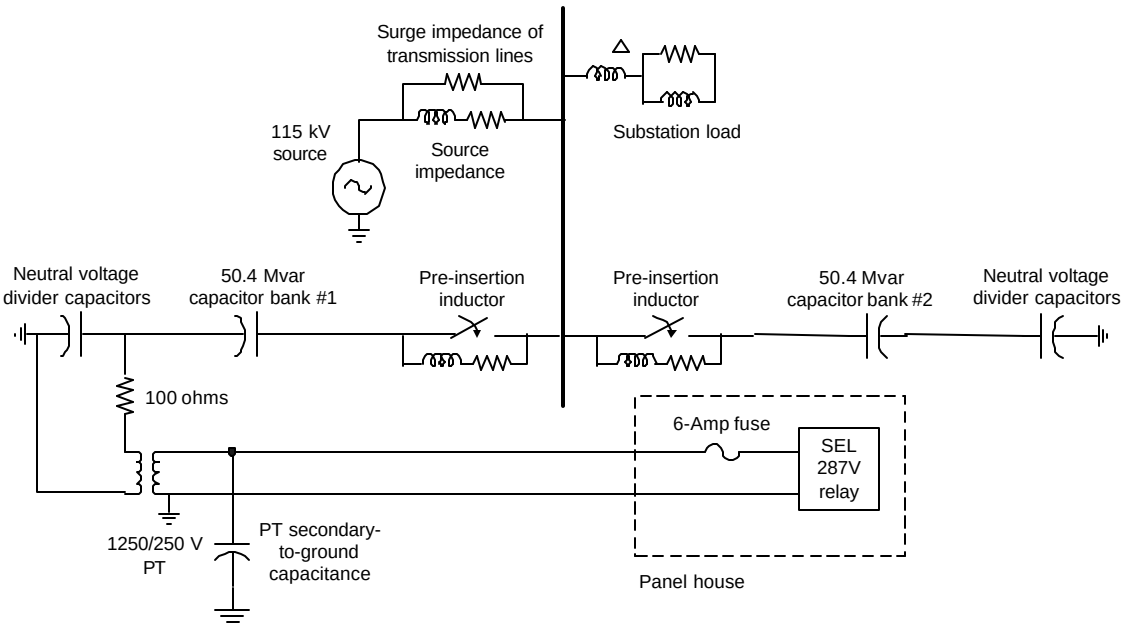


Figure 7. Single-Line Diagram of Equivalent Circuit for EMTP Simulation.

capacitors, 1250/250 V, 75 VA PTs, PT secondary cables, and fuses. Equivalent circuit parameters are summarized in Table 1.

Table 1: Summary of Equivalent Circuit Per-Phase Parameters Used in EMTP Simulations.

Parameter Description	Value
115 kV positive-sequence source impedance (based on specified available fault currents)	L = 8.318 mH, R = 0.49 ohm
115 kV zero-sequence source impedance (based on specified available fault currents)	L = 16.89 mH, R = 0.956 ohm
Substation load (assumed)	50 MW, 50 MVAR
Equivalent capacitance of 115 kV, 50.4 Mvar capacitor bank	9.168 μF
Equivalent capacitance of neutral voltage divider capacitors	1302 μF
Inductance and resistance of pre-insertion inductors	L = 40 mH, R = 81 ohms
PT rated primary voltage	1250 Volts
PT rated secondary voltage	250 Volts
PT rated VA	75 VA
PT primary-side series resistance	100 ohms
PT primary inherent resistance	48.673 ohms
PT secondary inherent resistance	0.675 ohm
PT inherent reactance	40.2 ohms
PT secondary-to-ground capacitance	20 nF

Inductive and capacitive coupling between the high-voltage bus conductors and the individual conductors in the PT secondary cable were represented using mutually-coupled RLC pi-equivalent circuits for the PT secondary cable of capacitor bank #1 only. Based on the configuration of the 115-kV bus conductors and the PT secondary cable, this mutual coupling was represented for three sections of the PT secondary cable:

- Length of PT secondary cable of capacitor bank #1 directly adjacent to the high-voltage phase conductors for capacitor bank #1 (length of approximately 45.8 ft in main cable trench approximately 25 ft from bank center phase)
- Length of PT secondary cable of capacitor bank #1 directly adjacent to the high-voltage phase conductors for capacitor bank #2 (length of approximately 45.8 ft in main cable trench approximately 25 ft from bank center phase)
- Remaining length of PT secondary cable of capacitor bank #1 from end of capacitor bank #2 to panel house (length of approximately 458 ft). Coupling in this length of cable was represented only between the three phase conductors and the neutral conductor of the PT secondary cable.

The average height of the 115-kV phase conductors was assumed to be 14.2 ft above ground, with an average phase spacing of 8 ft. Conductor resistance and self-inductance were based on parameters for 556 MCM aluminum cable. The PT secondary cable is direct buried at 18 inches below ground. Individual conductor resistance and self-inductance were based on parameters for #9 wire. For mutual inductance and capacitance calculations the ground mat, assumed to be located 24 inches below ground, was considered to represent an infinitely large conducting plane. Thus, all conductor heights were specified relative to the ground mat for these calculations.

EMTP Simulations:

Based upon the measurements previously performed by AVista, the following EMTP simulations were performed:

- Case 1: Energizing capacitor bank #1 with capacitor bank #2 already connected and with 200 ohm burden resistors connected in each phase near the SEL 287V relay connections for capacitor bank #1. The PT secondary neutral was grounded in the switchyard. The closing instants of the three poles of the Mark V Circuit-Switcher when the pre-insertion inductors are bypassed were selected to agree with those instants measured during the test conducted on April 26, 2000. This simulation case represents the circuit configuration during the initial tests on April 26, 2000 and also served to validate the measurements obtained from the simulation against that obtained during actual measurement.
- Case 2: Energizing capacitor bank #2 with capacitor bank #1 already connected and with parallel-connected 1.8 μF capacitors and 1500 ohm burden resistors, as recommended by S&C, connected in each phase near the SEL 287V relay inputs for capacitor bank #1. Also, as recommended by S&C, the PT secondary neutral was grounded in the panel house. The closing instants of the three poles of the Mark V Circuit-Switcher when the pre-insertion inductors are bypassed were selected to agree with those instants measured during the test conducted on May 2, 2000. This simulation case represents the circuit configuration during the tests on May 2, 2000

and also served to validate the measurements obtained from the simulation against that obtained during actual measurement.

- Case 3: Energizing capacitor bank #2 with capacitor bank #1 already connected and with parallel-connected 1.8 μF capacitors and 1500 ohm burden resistors, as recommended by S&C, connected in each phase near the SEL 287V relay inputs for capacitor bank #1. Also, as recommended by S&C, the PT secondary neutral was grounded in the panel house. 150-V rated MOVs were connected to ground from each phase and neutral at the PT secondary. The closing instants of the three poles of the Mark V Circuit-Switcher when the pre-insertion inductors are bypassed were selected to agree with those instants simulated for case 2. This simulation case served to determine the advantages gained by including surge suppression at the PT secondary when surge suppression is already applied in the panel house.
- Case 4: Energizing capacitor bank #2 with capacitor bank #1 already connected and with no surge suppression in the PT secondary circuit. The PT secondary neutral was grounded in the panel house. The PT secondary cable was shielded with 1-inch conduit grounded at 10-ft intervals. The closing instants of the three poles of the Mark V Circuit-Switcher when the pre-insertion inductors are bypassed were selected to agree with those instants simulated for case 2. This simulation case served to determine the advantages gained by shielding the PT secondary cable.

EMTP Simulation Results:

- Case 1: The EMTP simulation result for the inrush current into capacitor bank #1 during the bypass transient when the pre-insertion inductor is switched out of the circuit and with capacitor bank #2 already energized is shown in Figures 26(a) and (b) in Appendix A. The A-phase pole of the Circuit-Switcher bypasses the pre-insertion inductor at 21.1 ms, while the B and C-phase poles bypass at 26 ms.

  The peak inrush current is about 5550 A and the frequency of the inrush current is approximately 8330 Hz. Coupling between 115 kV phase conductors is evidenced by the occurrence of transients on the A-phase current waveform when the B and C-phase poles bypass the pre-insertion inductor.

  The phase-to-neutral voltage at the input of the SEL 287V relay on A phase is shown in Figures 27(a) and (b) in Appendix A. The peak voltage in this case is approximately 2230 V, which shows good correlation with the 2054 V peak recorded during the test on April 26, 2000 (see Appendix A, Figure 13). The simulated waveform shows clearly the effects of capacitive coupling initially and also the inductive coupling resulting from the inrush current.

  The neutral-to-ground voltage at the input of the SEL 287V relay is shown in Figures 28(a) and (b). The peak voltage in this case is approximately 7290 V compared to the 5089 V peak recorded during the test on April 26, 2000 (see Appendix A, Figure 14).

  The difference in the measured and simulated voltages can be attributed to the sampling rate of the Dranetz Model 658 recorder, the effective capacitance of

measurement equipment (including relays), and the actual coupling to the high-voltage conductors being less than that computed for the simulations.

- Case 2: For this simulation, the parallel-connected RC surge suppression circuit is included on each phase at the input to the SEL 287V relay, and the PT secondary neutral grounded in the panel house. Capacitor bank #2 is being energized, while bank #1 is already connected. The A-phase pole of the Circuit-Switcher bypasses the pre-insertion inductor at 15.7 ms, while the B and C-phase poles bypass at 20 ms.

  The phase-to-neutral voltage at the input of the SEL 287V relay on A phase is shown in Figure 29. The peak voltage in this case is approximately 142 V. The waveform agrees closely with that measured during the test on May 2, 2000 (see Appendix A, Figure 18). The simulated and measured waveforms show clearly the effects of the RC surge suppression circuit. Since the neutral is grounded at the panel house, the neutral-to-ground voltage at the input to the relay is negligible.

  The phase-to-ground voltage at the PT secondary terminals on A phase and neutral-to-ground voltage at this location are shown in Figures 30(a) and (b). The peak phase-to-ground voltage in this case is approximately –4140 V, and the peak neutral-to-ground voltage is approximately –4190 V. Despite the surge suppression in the panel house, it is clear that the PT secondary cable insulation will be subjected to very high transient voltages.

  For this circuit arrangement the I^2t of the PT secondary fuses was also measured to determine if the fuses might be caused to operate with the RC surge suppression circuits connected on the load side of the fuses. The highest I^2t measured in any of the three phases was approximately 2 $Ampere^2$-seconds, which is much less than the estimated minimum I^2t of approximately 31 $Ampere^2$-seconds required to operate the 6-Amp fuses.

- Case 3: For this simulation, the parallel-connected RC surge suppression circuit is included on each phase at the input to the SEL 287V relay, and the PT secondary neutral is grounded in the panel house. 150-V rated MOVs were connected at the secondary phase and neutral terminals of the PTs for capacitor bank #1 for additional surge protection. Capacitor bank #2 is being energized, while bank #1 is already connected. The A-phase pole of the Circuit-Switcher bypasses the pre-insertion inductor at 15.7 ms, while the B and C-phase poles bypass at 20 ms.

  The phase-to-ground voltage at the PT secondary terminals on A phase is shown in Figure 31 in Appendix A. The peak voltage is considerably reduced (from about –4140 V to 380 V). However, when looking at phase-to-ground voltages at points along the PT secondary cable, high transient voltages are again evident. See Figure 32.

- Case 4: For this simulation there is no surge suppression circuit in the panel house, while the PT secondary neutral is grounded in the panel house. The PT secondary

cable is shielded with 1-inch conduit grounded at 10-ft intervals. Capacitor bank #2 is being energized, while bank #1 is already connected. The A-phase pole of the Circuit-Switcher bypasses the pre-insertion inductor at 15.7 ms, while the B and C-phase poles bypass at 20 ms.

The phase-to-neutral voltage at the input of the SEL 287V relay on A phase is shown in Figure 33 in Appendix A. Since the PT secondary cable is shielded, there is almost no coupling from the high-voltage conductors. The phase-to-ground voltage at the PT secondary terminals on A phase is shown in Figure 34. Again, there is almost no coupling from the high-voltage conductors.

Similar results were obtained for transient simulations of the circuit configuration at Otis Orchards substation where the old capacitor bank configuration is used.

Conclusions and Recommendations:

The simulation results presented indicate that:

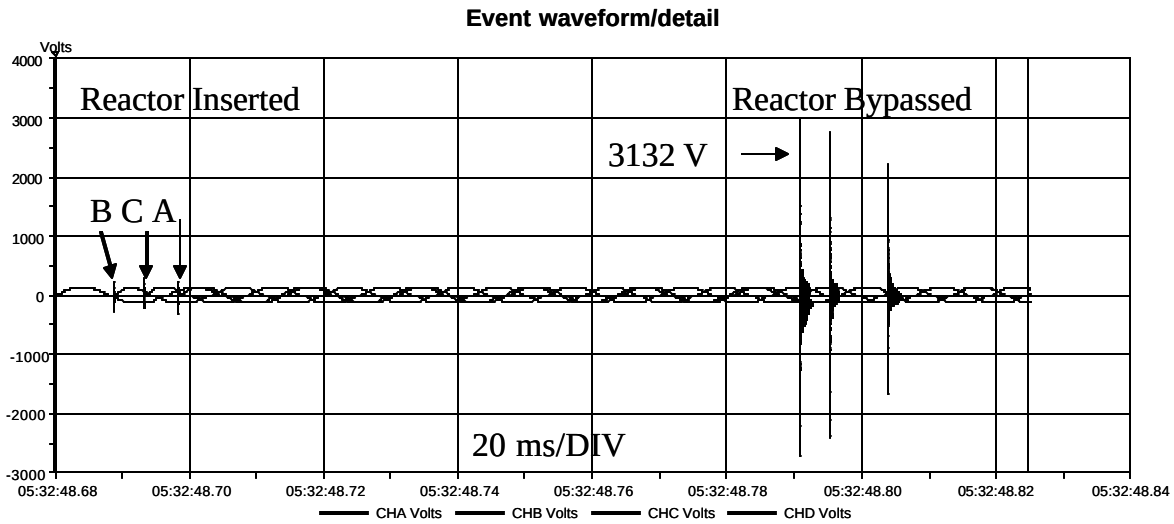
- Transient voltages measured in the PT secondary circuits are due to inductive and capacitive coupling between the high-voltage conductors and the conductors in the PT secondary cable. The transient voltages occur when the pre-insertion inductors, used for limiting back-to-back inrush currents and bus overvoltages during capacitor bank energization, are bypassed. High-magnitude and frequency inrush currents, which occur during energization of one capacitor bank with another bank already connected, induce voltage transients in the conductors of the PT secondary cables if these cables are not properly shielded.
- RC surge suppression circuits connected near the inputs of the SEL 287V relays largely mitigate the induced transient voltages at the relay inputs. Transient mitigation at this location will also limit any transient currents which may otherwise cause the PT secondary fuses to operate. However, transient voltages at the PT secondary terminals and along the PT secondary cable are not reduced when surge suppression is applied at the relay inputs. Repetitive switching of capacitor banks and magnitudes of induced voltages involved may stress PT secondary cable insulation, which may ultimately result in PT secondary cable failures.
- MOVs or other means of surge suppression at the PT secondary terminals largely reduce transient voltages at this location, but do not reduce the transient voltages that may occur along the PT secondary cables.
- Shielding of the PT secondary cables, along with grounding at 10-ft intervals, largely eliminates the occurrence of transient voltages in the PT secondary cables. No additional surge suppression circuits are required if cables are shielded.

Based on the simulation results and the above-listed conclusions, shielding of PT secondary cables will be the preferred solution. Shielding can be effected by running the PT secondary cables in 1-inch conduit and grounding the conduit at 10 ft intervals. The RC surge suppression circuit connected near the inputs to the SEL 287V relays should be viewed as a temporary solution only. As a general application guideline, the value of the capacitor should be selected such that the effective burden

does not exceed about 50% of the rated burden of the PT involved. The resistance is generally selected to be nearly equal to the reactance of the capacitor at 60 Hz. A power rating based on twice the rated circuit voltage should be adequate for the resistor. The 1.8 μF capacitor selected for this application has a capacitive reactance of approximately 1474 ohms, which represents a burden of about 56% to the 250-V, 75-VA rated PT. The resistor value of 1500 ohms is nearly equal to the reactance of the capacitor, and the recommended power rating, based on twice the circuit voltage of 96 V rms is approximately 25 W.

Transient voltages of the same type measured at Third and Hatch Substation are expected to occur at other substations (including Otis Orchards) where capacitor banks are switched back-to-back and PT secondary cables are not properly shielded. The severity of the transient voltages will depend on the magnitude and frequency of the inrush currents involved, as well as the physical arrangement of the PT secondary cables relative to the high-voltage conductors. Proper shielding of PT secondary cables at these substations would eliminate these types of transient voltages.

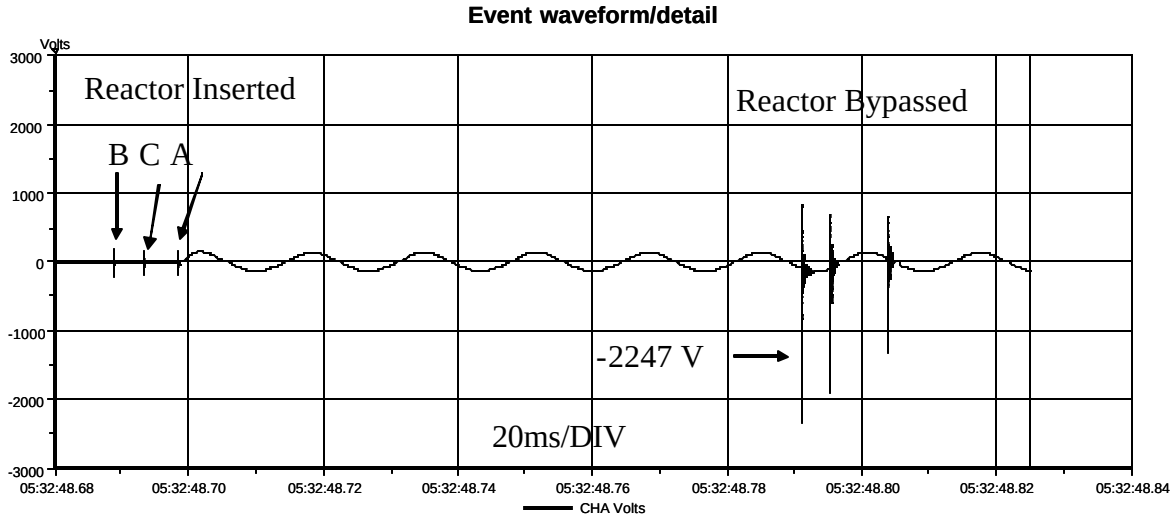
APPENDIX A



AV,BV,CV,DV Impulse event at 02/04/2000 05:32:48.68

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	0.5	95.5	-2247.0	205 deg	6
BV Volts	0.3	56.8	111.8	-2532.0	101 deg	6
CV Volts	0.0	47.2	96.9	-2081.0	336 deg	6
DV Volts	92.8	93.1	150.0	3132.0	235 deg	6

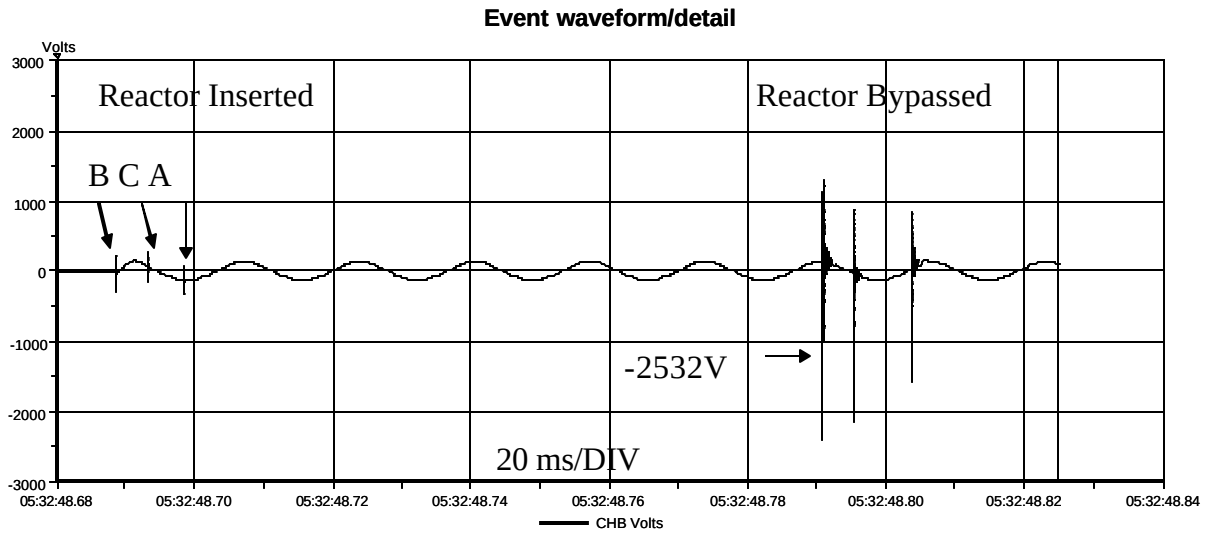
FIG 1: Third & Hatch tests of 2/4/00. Close bank 2 with bank 1 on. Show all 4 channels (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP =3,132 V on AØ-N on bank 1.



AV,BV,CV,DV Impulse event at 02/04/2000 05:32:48.68

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	0.5	95.5	-2247.0	205 deg	6
BV Volts	0.3	56.8	111.8	-2532.0	101 deg	6
CV Volts	0.0	47.2	96.9	-2081.0	336 deg	6
DV Volts	92.8	93.1	150.0	3132.0	235 deg	6

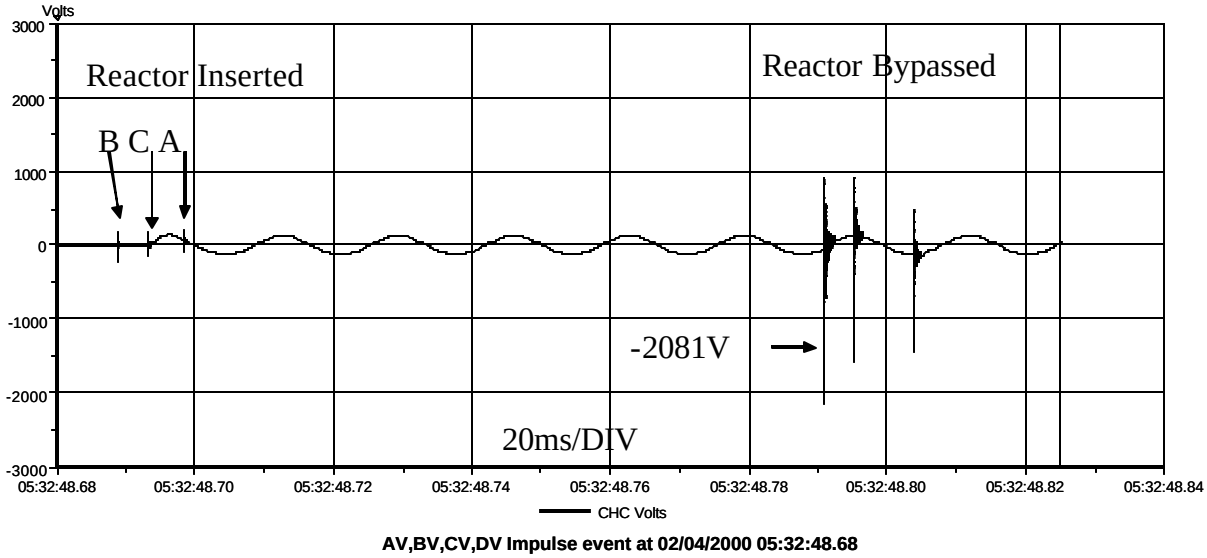
FIG 2: Third & Hatch tests of 2/4/00. Close bank 2 with bank 1 on. Show CH-A only. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP = 3,132 V on AØ-N on bank 1.



AV,BV,CV,DV Impulse event at 02/04/2000 05:32:48.68

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	0.5	95.5	-2247.0	205 deg	6
BV Volts	0.3	56.8	111.8	-2532.0	101 deg	6
CV Volts	0.0	47.2	96.9	-2081.0	336 deg	6
DV Volts	92.8	93.1	150.0	3132.0	235 deg	6

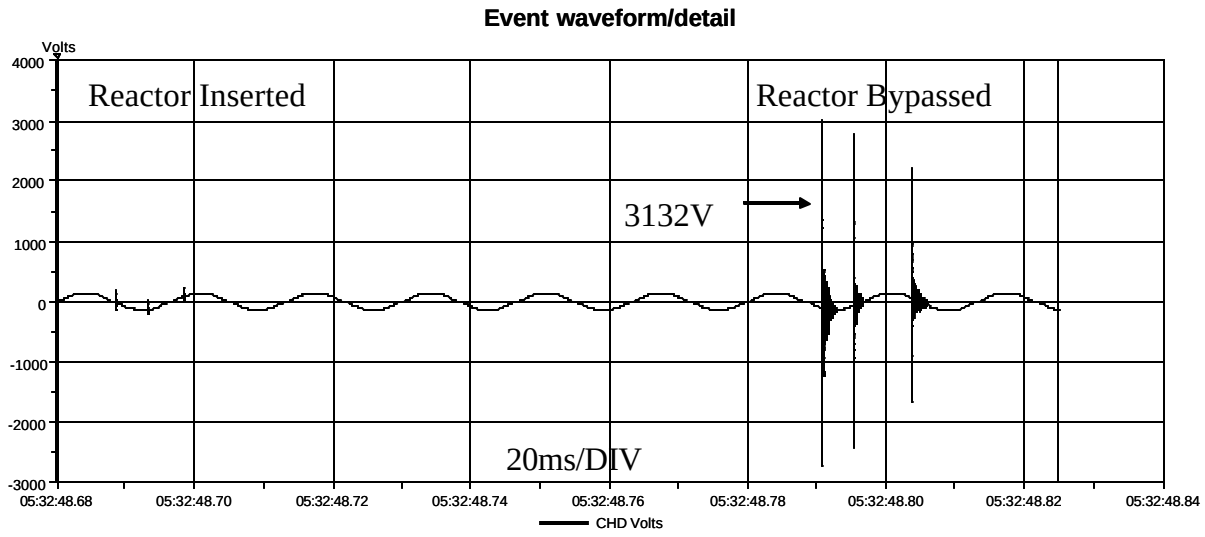
FIG 3: Third & Hatch tests of 2/4/00. Close bank 2 with bank 1 on. Show CH-B only. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP = 3,132 V on AØ-N on bank 1.



AV,BV,CV,DV Impulse event at 02/04/2000 05:32:48.68

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	0.5	95.5	-2247.0	205 deg	6
BV Volts	0.3	56.8	111.8	-2532.0	101 deg	6
CV Volts	0.0	47.2	96.9	-2081.0	336 deg	6
DV Volts	92.8	93.1	150.0	3132.0	235 deg	6

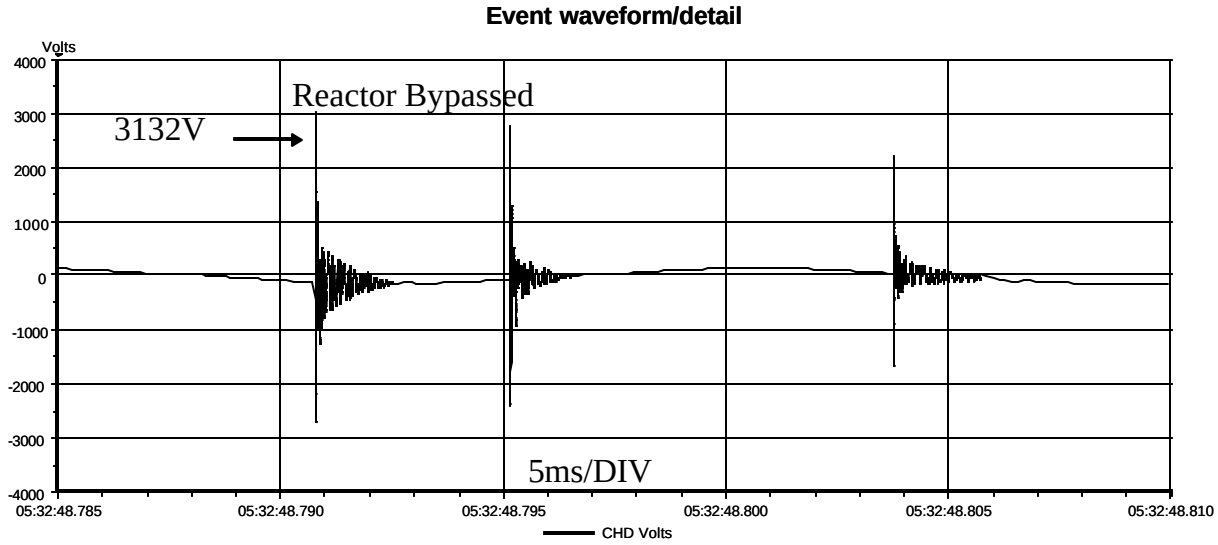
FIG 4: Third & Hatch tests of 2/4/00. Close bank 2 with bank 1 on. Show CH-C only. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP = 3,132 V on AØ-N on bank 1.



AV,BV,CV,DV Impulse event at 02/04/2000 05:32:48.68

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	0.5	95.5	-2247.0	205 deg	6
BV Volts	0.3	56.8	111.8	-2532.0	101 deg	6
CV Volts	0.0	47.2	96.9	-2081.0	336 deg	6
DV Volts	92.8	93.1	150.0	3132.0	235 deg	6

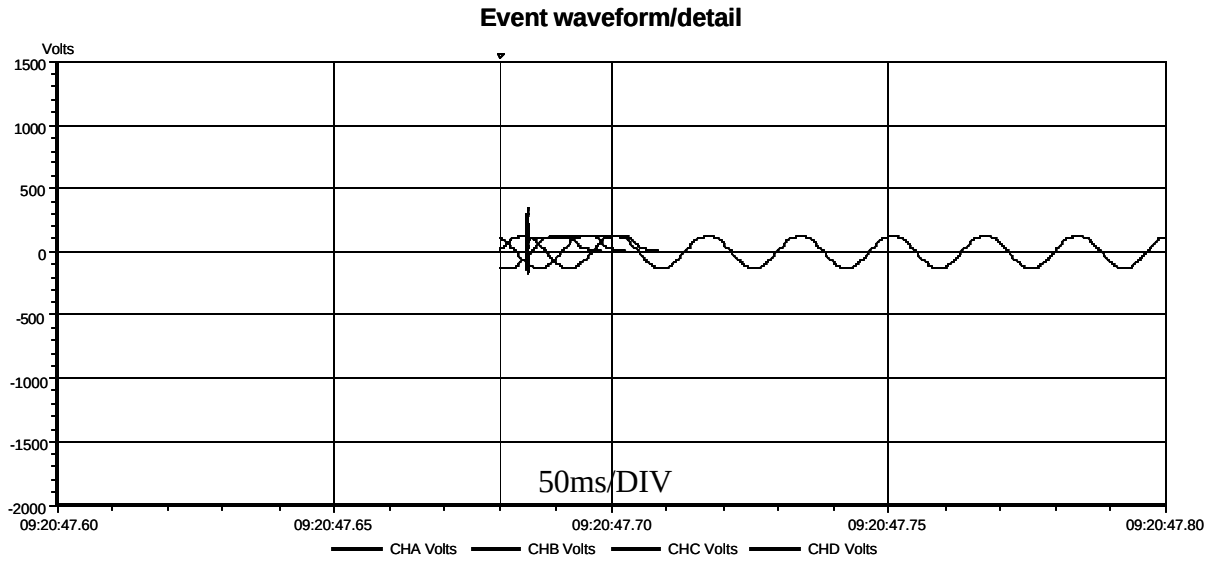
FIG 5: Third & Hatch tests of 2/4/00. Close bank 2 with bank 1 on. Show CH-D only. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP = 3,132 V on AØ-N on bank 1.



AV,BV,CV,DV Impulse event at 02/04/2000 05:32:48.68

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	0.5	95.5	-2247.0	205 deg	6
BV Volts	0.3	56.8	111.8	-2532.0	101 deg	6
CV Volts	0.0	47.2	96.9	-2081.0	336 deg	6
DV Volts	92.8	93.1	150.0	3132.0	235 deg	6

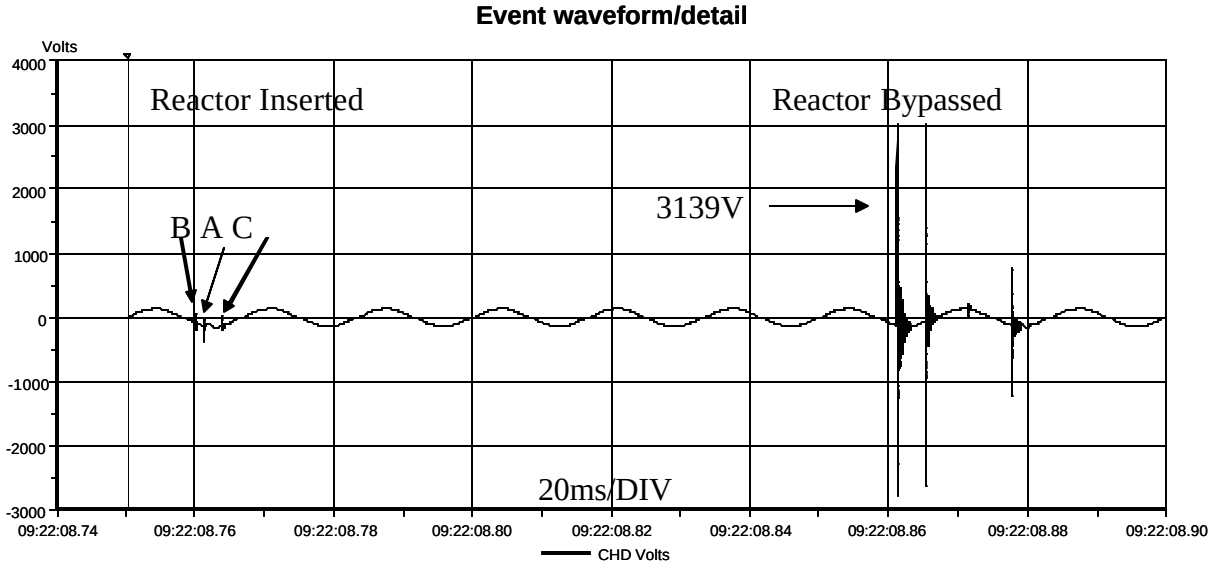
FIG 6: Third & Hatch tests of 2/4/00. Close bank 2 with bank 1 on. Show CH-D only. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP = 3,132 V on AØ-N on bank 1.



AV,BV,CV,DV Impulse event at 02/04/2000 09:20:47.68

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	94.2	0.5	87.9	167.0	72 deg	1
BV Volts	94.3	0.5	103.2	226.0	344 deg	1
CV Volts	94.1	0.2	103.4	160.0	258 deg	1
DV Volts	94.1	92.9	93.7	-276.0	102 deg	1

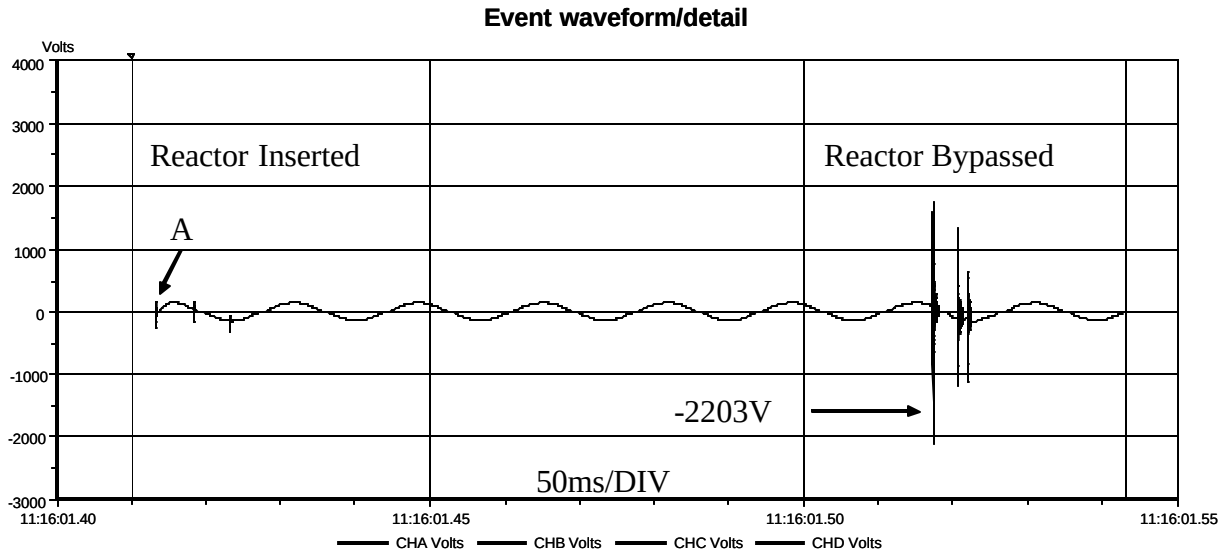
FIG 7: Third & Hatch tests of 2/4/00. Open bank 2 with bank 1 on. Show all channels. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP = -276 V on AØ-N on bank 1.



AV,BV,CV,DV Impulse event at 02/04/2000 09:22:08.75

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	67.3	97.1	-2194.0	252 deg	6
BV Volts	0.5	40.7	97.5	-2632.0	135 deg	6
CV Volts	0.1	31.7	97.4	-2102.0	6 deg	6
DV Volts	93.4	93.7	109.2	3139.0	240 deg	7

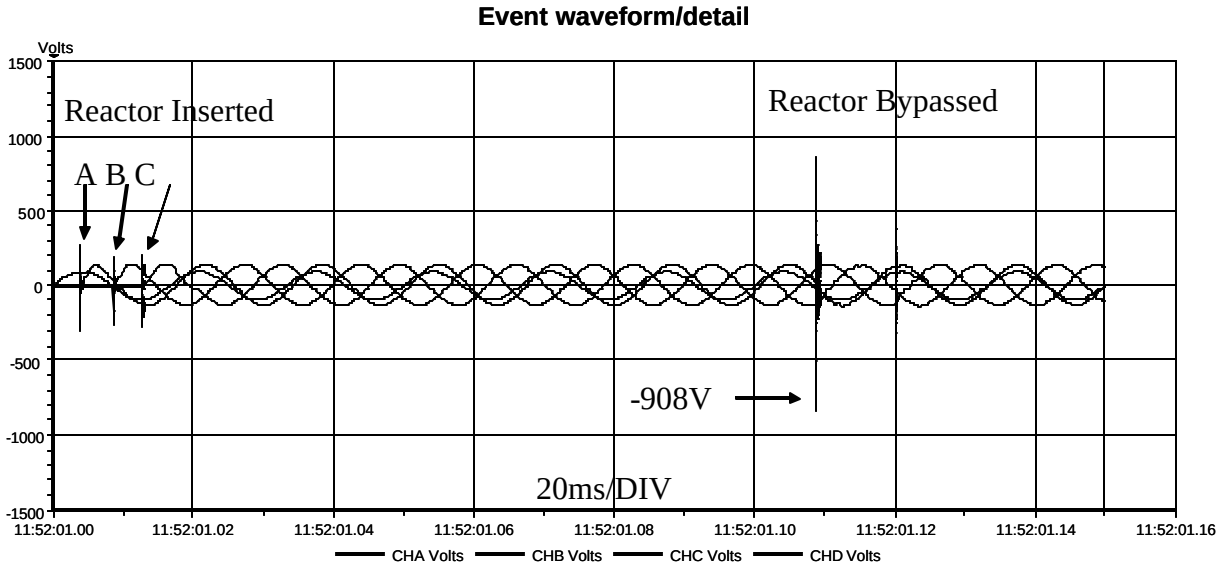
FIG 8: Third & Hatch tests of 2/4/00. Close bank 2 with bank 1 on. Show CH-D only. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP = 3,139 V on AØ-N on bank 1.



AV,BV,CV,DV Impulse event at 02/04/2000 11:16:01.41

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	0.1	1.5	-648.0	267 deg	3
BV Volts	0.5	0.3	2.4	-780.0	267 deg	3
CV Volts	0.0	0.2	1.8	-648.0	267 deg	3
DV Volts	0.0	85.4	96.8	-2203.0	136 deg	6

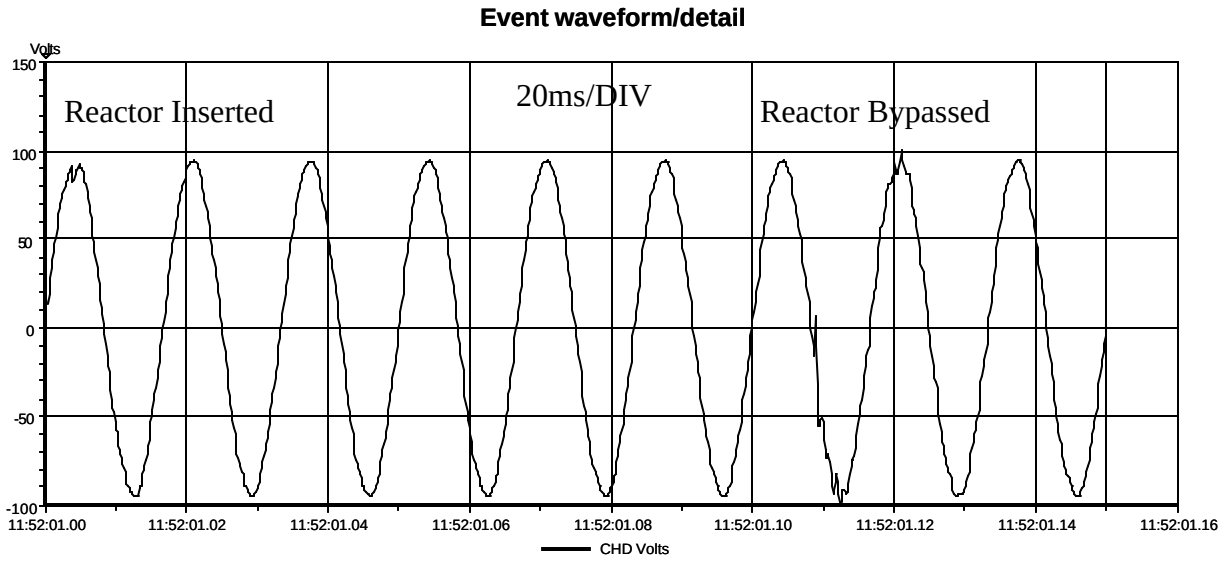
FIG 9: Third & Hatch tests of 2/4/00. Close bank 1 with bank 2 off. Show all channels. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on bank 1). Worst V IMP = -2203 V on AØ-N on bank 1.



AV,BV,CV Impulse event at 02/08/2000 11:52:01.00

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	82.9	96.9	-730.0	171 deg	5
BV Volts	0.3	59.1	99.3	-908.0	51 deg	5
CV Volts	0.0	51.1	94.7	-714.0	291 deg	5
DV Volts	65.9	66.2	66.8	0.0	0 deg	0

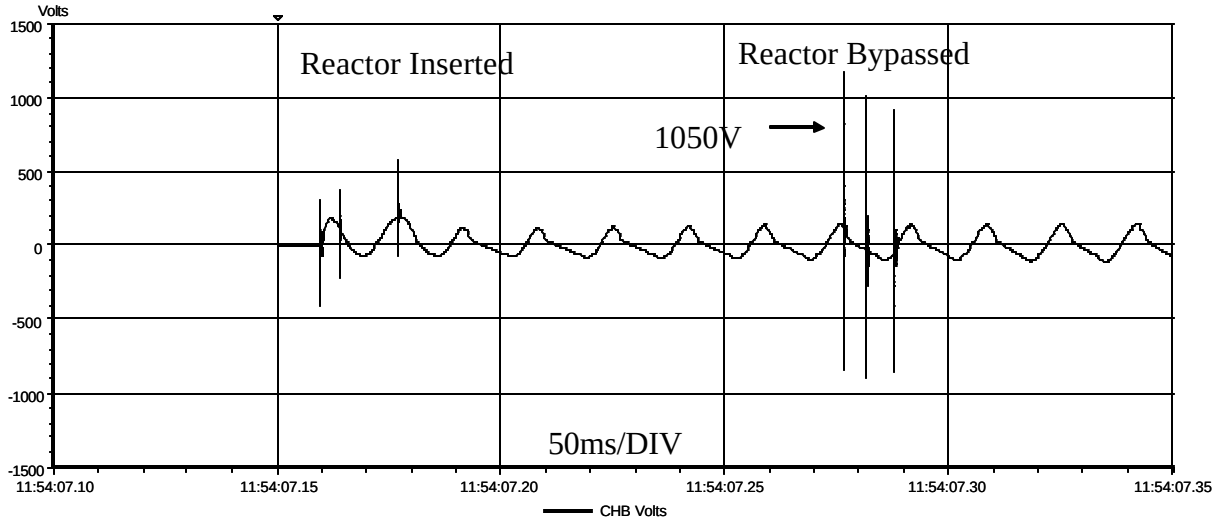
FIG 10: Third & Hatch tests of 2/8/00. Close bank 2 with bank 1 off. Show all channels. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on Bus PT's). Worst V IMP = -908 V on BØ-N on bank 2. Bus PT AØ-N V IMP = 0.



AV,BV,CV Impulse event at 02/08/2000 11:52:01.00

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	82.9	96.9	-730.0	171 deg	5
BV Volts	0.3	59.1	99.3	-908.0	51 deg	5
CV Volts	0.0	51.1	94.7	-714.0	291 deg	5
DV Volts	65.9	66.2	66.8	0.0	0 deg	0

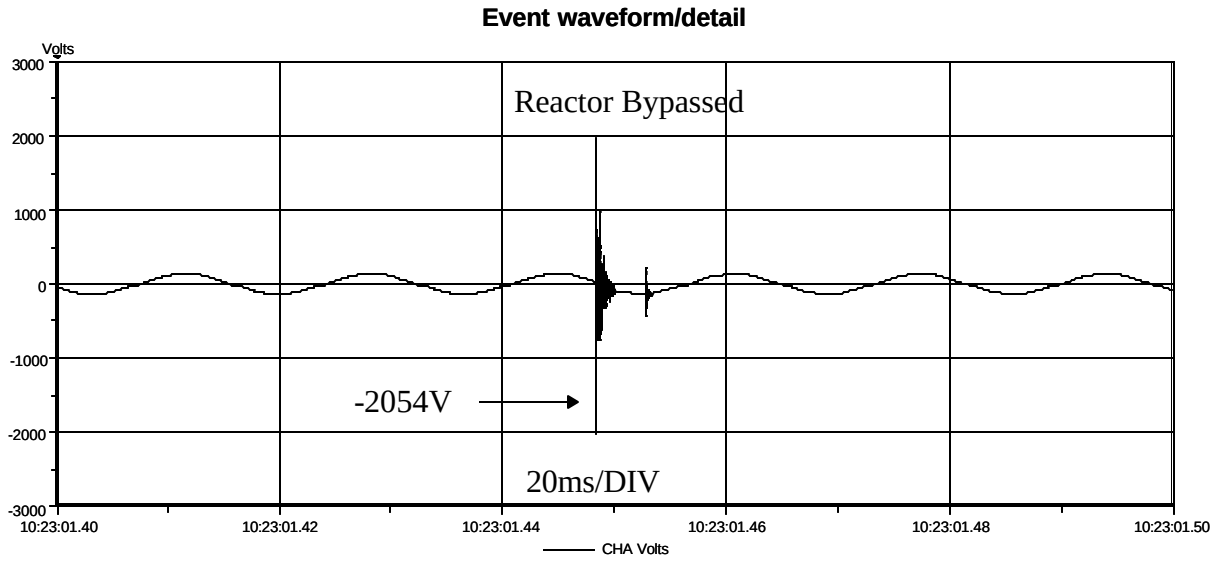
FIG 11: Third & Hatch tests of 2/8/00. Close bank 2 with bank 1 off. Show CH-D only. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on Bus PT's). Worst V IMP = -908 V on BØ-N on bank 2. Bus PT AØ-N V IMP = 0.



AV,BV,CV Impulse event at 02/08/2000 11:54:07.15

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.0	3.0	90.4	850.0	351 deg	6
BV Volts	0.5	57.7	109.0	1050.0	90 deg	6
CV Volts	0.0	57.1	105.3	871.0	327 deg	6
DV Volts	65.7	65.4	66.4	0.0	0 deg	0

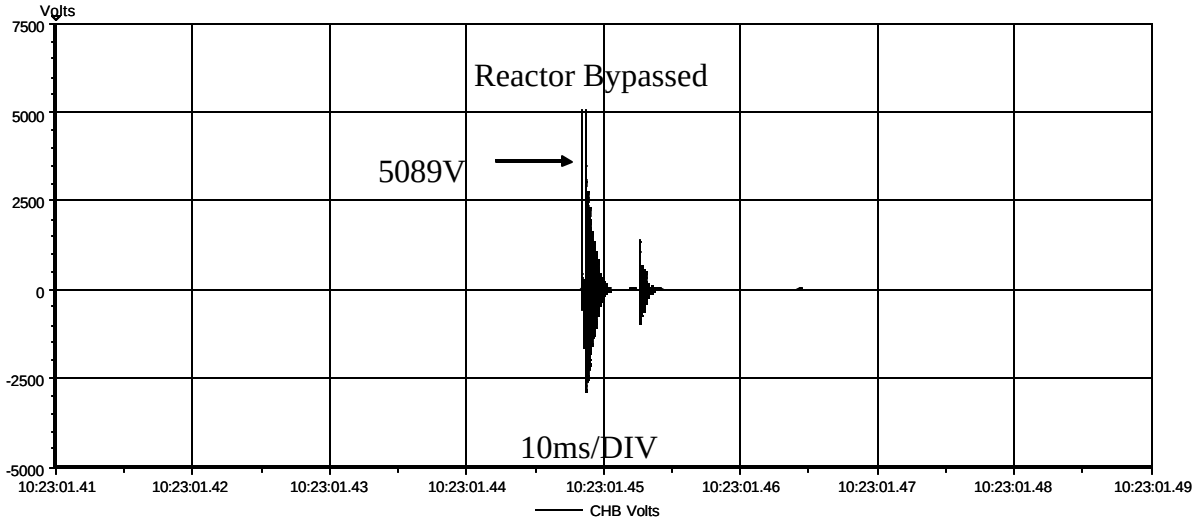
FIG 12: Third & Hatch tests of 2/8/00. Close bank 2 with bank 1 off. Show CH-B only. (AV=AØ-N, BV=BØ-N, CV=CØ-N on bank 2) / (DV=AØ-N on Bus PT's). Worst V IMP = 1050 V on BØ-N on bank 2. Bus PT AØ-N V IMP = 0. BØ-N is distorted.



AV,BV,CV,DV Impulse event at 04/26/2000 10:23:01.34

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.3	67.4	91.1	-2054.0	162 deg	5
BV Volts	1.5	0.6	8.1	5089.0	282 deg	5
CV Volts	93.7	0.0	94.6	-5420.0	183 deg	5
DV Volts	1.3	0.5	8.3	-4704.0	284 deg	5

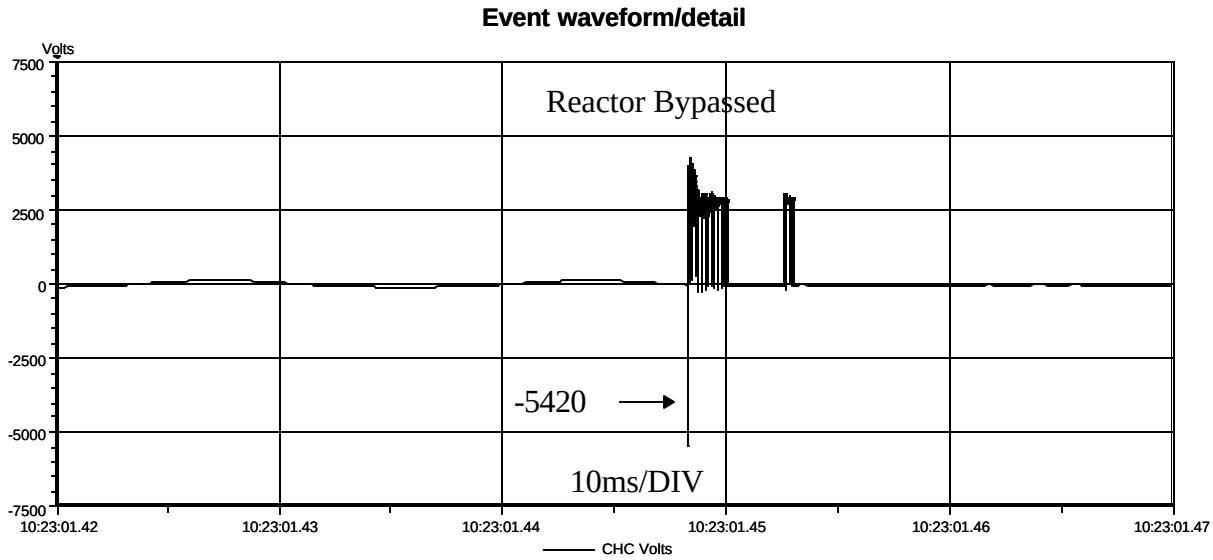
FIG 13: Third & Hatch tests of 4/26/00. Close bank 1 with bank 2 on. Show CH-A only. (AV=AØ-N, BV=N-GND on bank 1) / (CV=AØ-N, DV=N-GND on bank 2). Worst V IMP = -5420 V on AØ-N on bank 2.



AV,BV,CV,DV Impulse event at 04/26/2000 10:23:01.34

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.3	67.4	91.1	-2054.0	162 deg	5
BV Volts	1.5	0.6	8.1	5089.0	282 deg	5
CV Volts	93.7	0.0	94.6	-5420.0	183 deg	5
DV Volts	1.3	0.5	8.3	-4704.0	284 deg	5

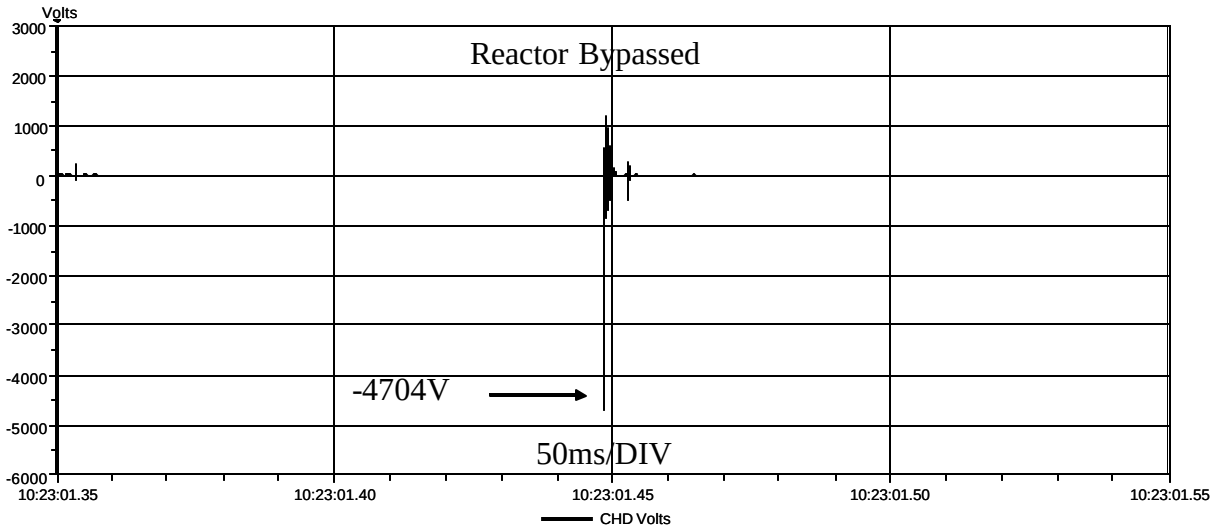
FIG 14: Third & Hatch tests of 4/26/00. Close bank 1 with bank 2 on. Show CH-B only. (AV=AØ-N, BV=N-GND on bank 1) / (CV=AØ-N, DV=N-GND on bank 2). Worst V IMP = -5420 V on AØ-N on bank 2.



AV,BV,CV,DV Impulse event at 04/26/2000 10:23:01.34

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.3	67.4	91.1	-2054.0	162 deg	5
BV Volts	1.5	0.6	8.1	5089.0	282 deg	5
CV Volts	93.7	0.0	94.6	-5420.0	183 deg	5
DV Volts	1.3	0.5	8.3	-4704.0	284 deg	5

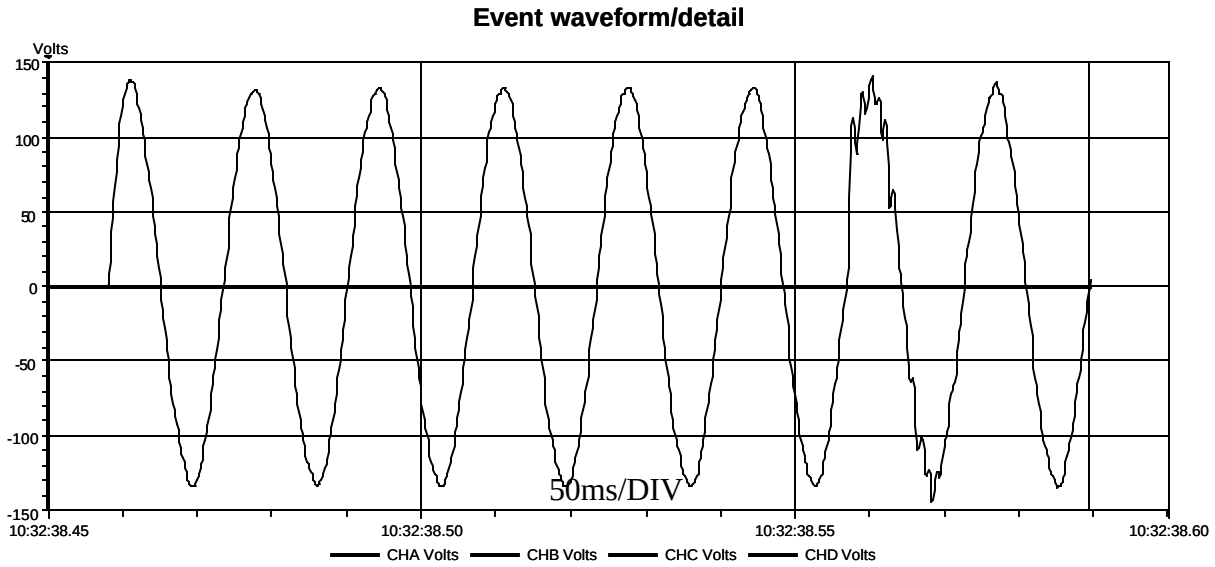
FIG 15: Third & Hatch tests of 4/26/00. Close bank 1 with bank 2 on. Show CH-C only. (AV=AØ-N, BV=N-GND on bank 1) / (CV=AØ-N, DV=N-GND on bank 2). Worst V IMP = -5420 V on AØ-N on bank 2.



AV,BV,CV,DV Impulse event at 04/26/2000 10:23:01.34

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	0.3	67.4	91.1	-2054.0	162 deg	5
BV Volts	1.5	0.6	8.1	5089.0	282 deg	5
CV Volts	93.7	0.0	94.6	-5420.0	183 deg	5
DV Volts	1.3	0.5	8.3	-4704.0	284 deg	5

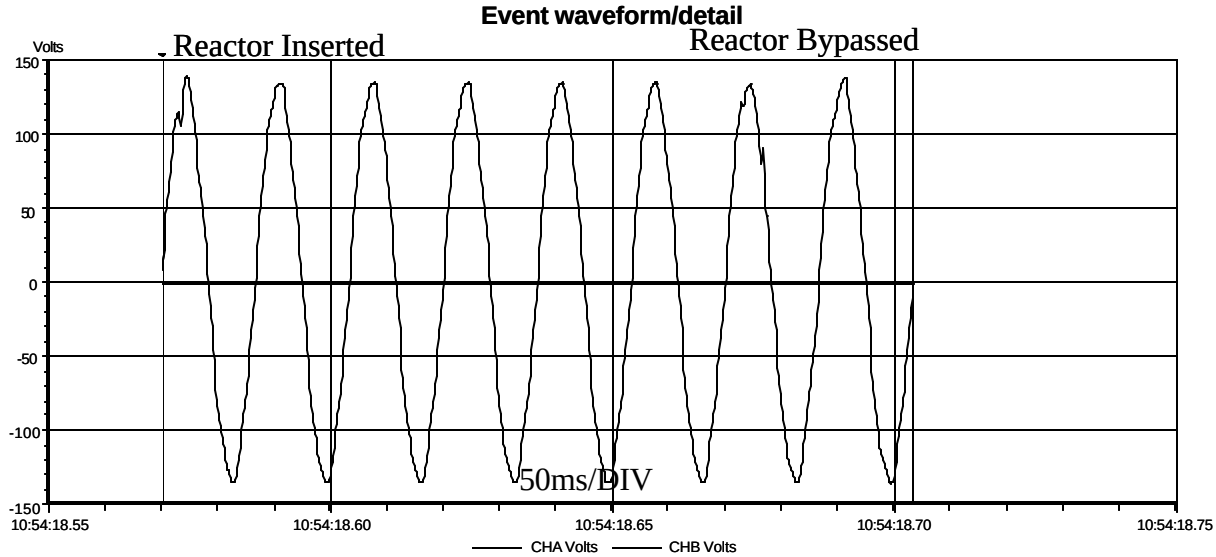
FIG 16: Third & Hatch tests of 4/26/00. Close bank 1 with bank 2 on. Show CH-D only. (AV=AØ-N, BV=N-GND on bank 1) / (CV=AØ-N, DV=N-GND on bank 2). Worst V IMP = -5420 V on AØ-N on bank 2.



Waveform event at 05/02/2000 10:32:38.45

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase
AV Volts	0.0	64.2	96.1	0.0	0 deg.
BV Volts	0.0	0.0	0.0	0.0	0 deg.
CV Volts	0.0	0.0	0.0	0.0	0 deg.
DV Volts	0.0	0.0	0.0	0.0	0 deg.

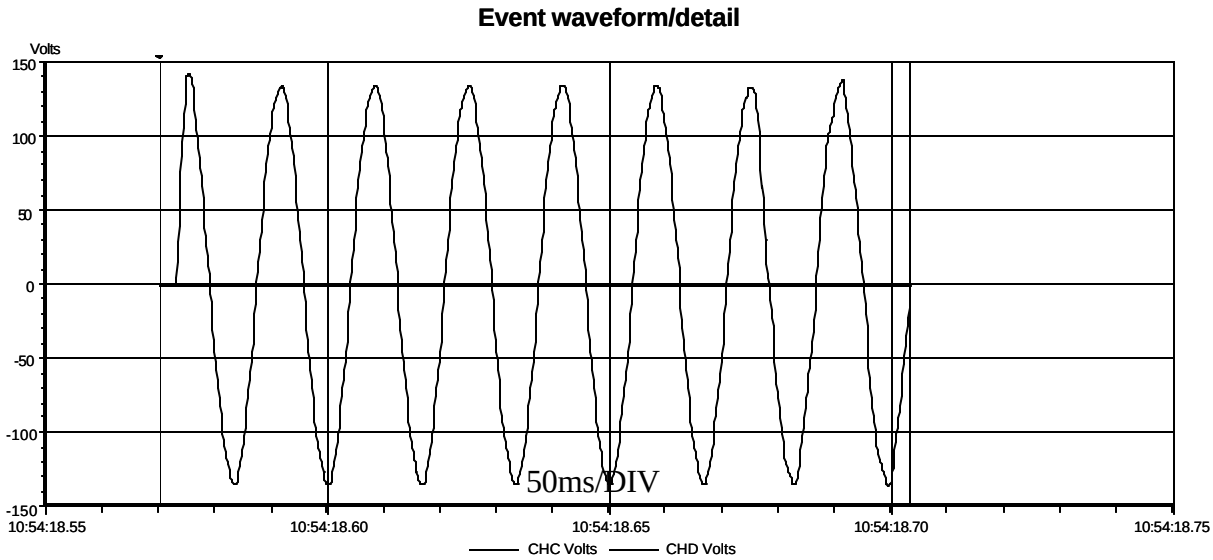
FIG 17: Third & Hatch tests of 5/2/00. Close bank 1 with bank 2 off. Show all channels. (AV=AØ-N, BV=N-GND on bank 1) / (CV=AØ-N, DV=N-GND on bank 2). Worst V IMP = 0.



Waveform event at 05/02/2000 10:54:18.57

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase
AV Volts	93.9	93.9	94.6	0.0	0 deg.
BV Volts	1.4	0.2	0.2	0.0	0 deg.
CV Volts	0.0	89.4	96.4	0.0	0 deg.
DV Volts	0.0	0.0	0.0	0.0	0 deg.

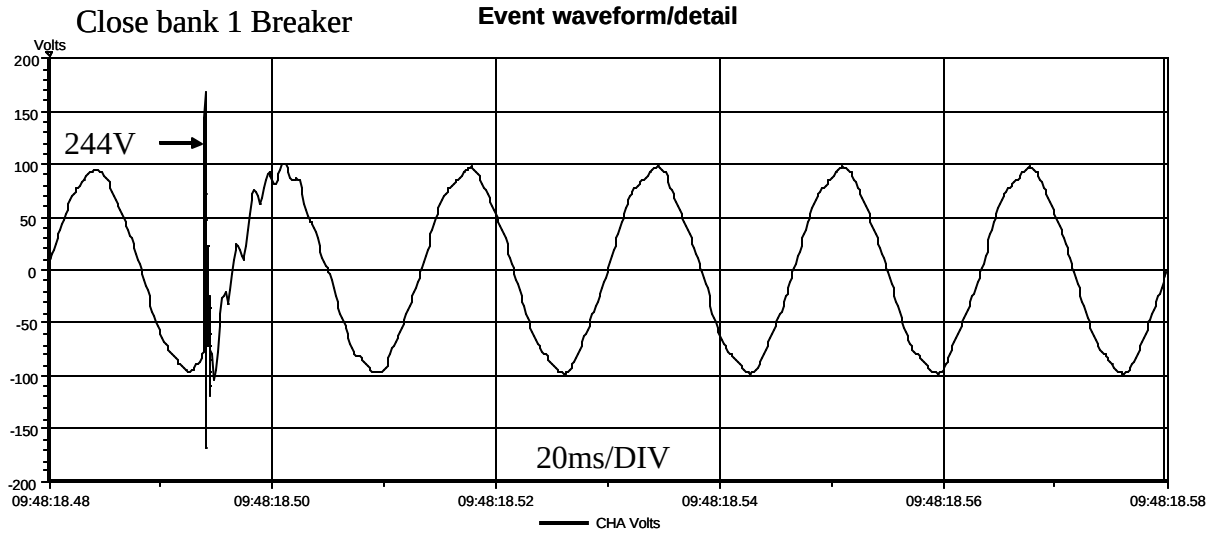
FIG 18: Third & Hatch tests of 5/2/00. Close bank 2 with bank 1 on. Show CH-A & B (AV=AØ-N, BV=N-GND on bank 1) / (CV=AØ-N, DV=N-GND on bank 2). Worst V IMP = 0.



Waveform event at 05/02/2000 10:54:18.57

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase
AV Volts	93.9	93.9	94.6	0.0	0 deg.
BV Volts	1.4	0.2	0.2	0.0	0 deg.
CV Volts	0.0	89.4	96.4	0.0	0 deg.
DV Volts	0.0	0.0	0.0	0.0	0 deg.

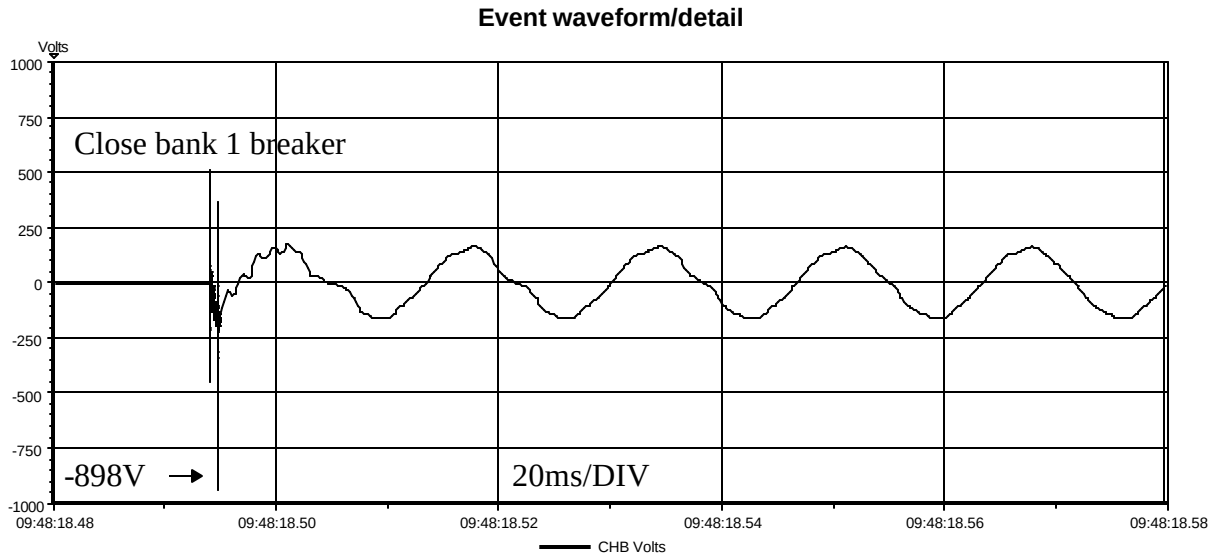
FIG 19: Third & Hatch tests of 5/2/00. Close bank 2 with bank 1 on. Show CH-C & D (AV=AØ-N, BV=N-GND on bank 1) / (CV=AØ-N, DV=N-GND on bank 2). Worst V IMP = 0.



AV,BV,CV,DV Impulse event at 05/10/2000 09:48:18.48

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	66.4	66.3	67.0	244.0	306 deg	1
BV Volts	33.8	33.4	111.8	-898.0	306 deg	1
CV Volts	2.9	0.0	2.5	-720.0	223 deg	1
DV Volts	7.3	0.1	6.4	2159.0	223 deg	1

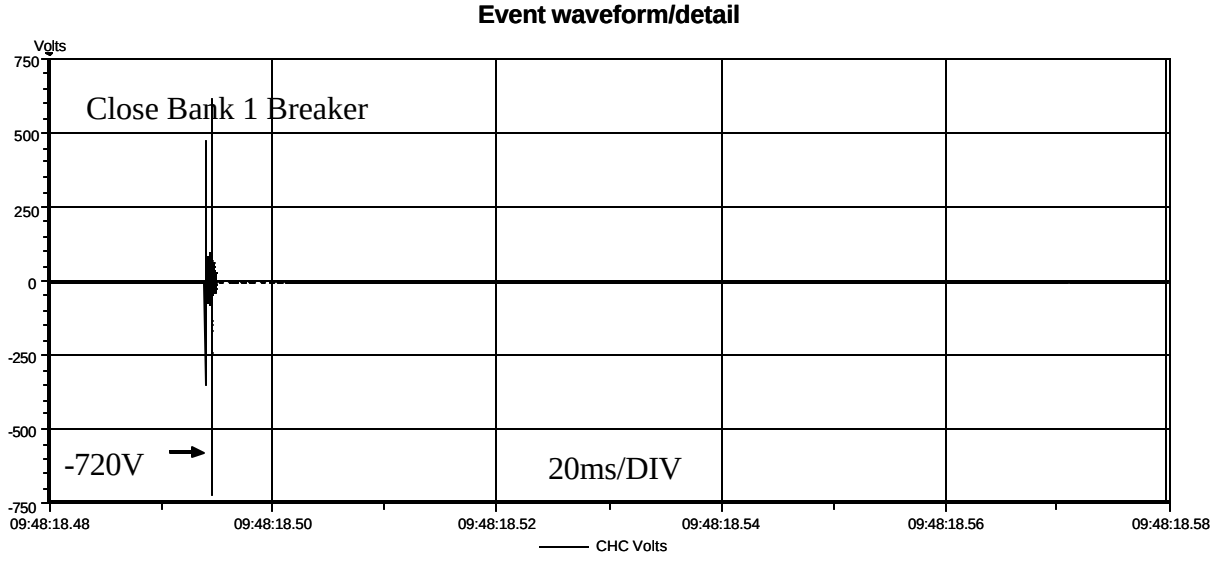
FIG 20: Otis Orchards tests of 5/10/00. Close bank 1. Show CH-A only (AV=AØ-N bus PT's, BV=AØ-N on bank 1, CV=AØ-N on bank 2, DV=N-GND on bank 1). Worst V IMP = 2159 N-GND on bank 1.



AV,BV,CV,DV Impulse event at 05/10/2000 09:48:18.48

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	66.4	66.3	67.0	244.0	306 deg	1
BV Volts	33.8	33.4	111.8	-898.0	306 deg	1
CV Volts	2.9	0.0	2.5	-720.0	223 deg	1
DV Volts	7.3	0.1	6.4	2159.0	223 deg	1

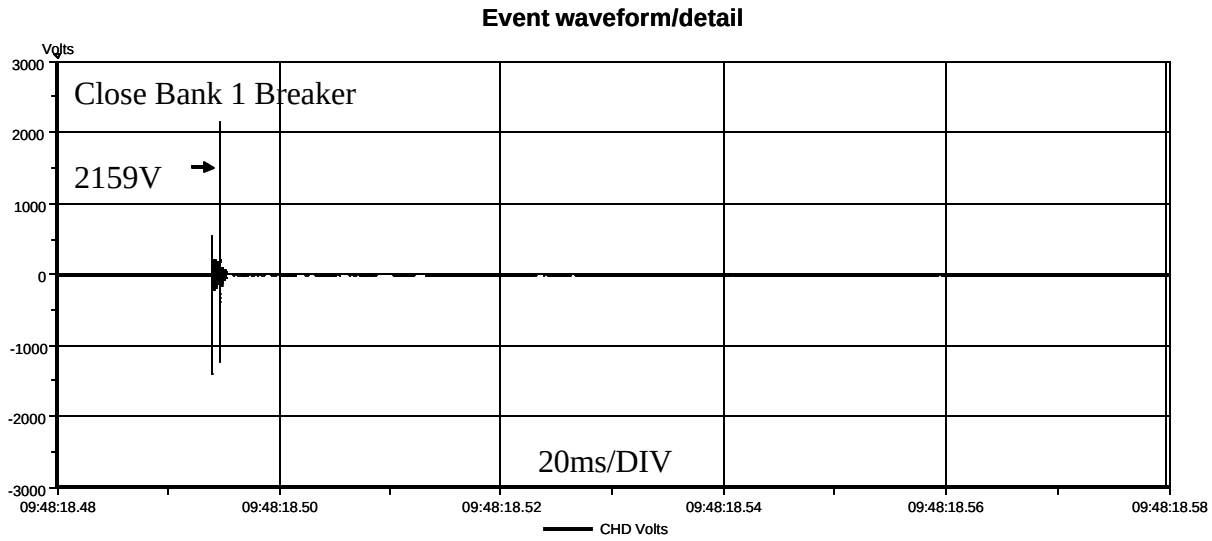
FIG 21: Otis Orchards tests of 5/10/00. Close bank 1. Show CH-B only (AV=AØ-N bus PT's, BV=AØ-N on bank 1, CV=AØ-N on bank 2, DV=N-GND on bank 1). Worst V IMP = 2159 N-GND on bank 1.



AV,BV,CV,DV Impulse event at 05/10/2000 09:48:18.48

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	66.4	66.3	67.0	244.0	306 deg	1
BV Volts	33.8	33.4	111.8	-898.0	306 deg	1
CV Volts	2.9	0.0	2.5	-720.0	223 deg	1
DV Volts	7.3	0.1	6.4	2159.0	223 deg	1

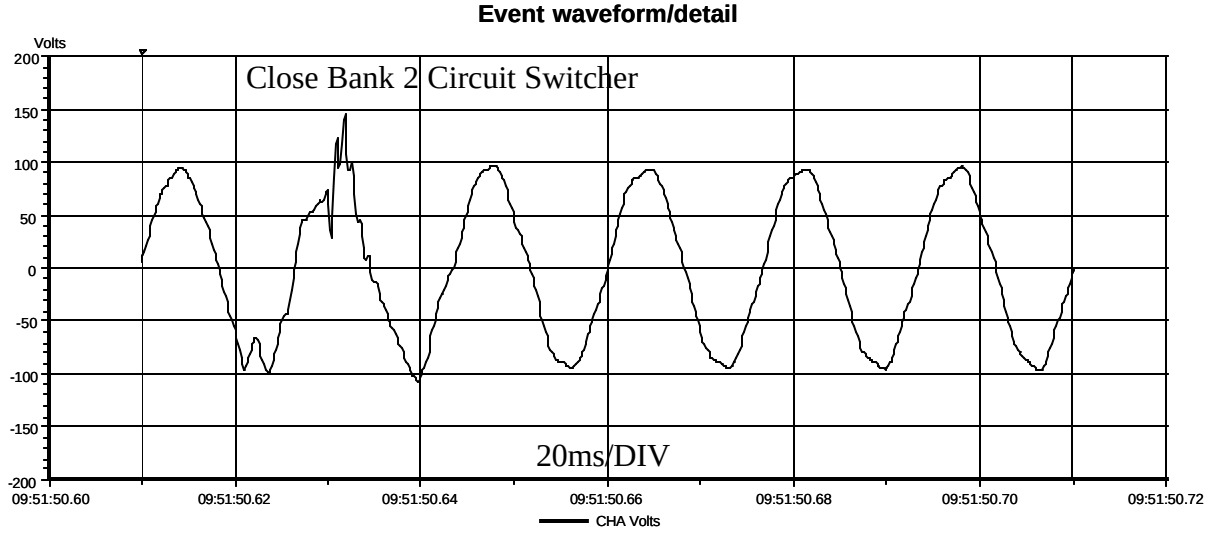
FIG 22: Otis Orchards tests of 5/10/00. Close bank 1. Show CH-C only (AV=AØ-N bus PT's, BV=AØ-N on bank 1, CV=AØ-N on bank 2, DV=N-GND on bank 1). Worst V IMP = 2159 N-GND on bank 1.



AV,BV,CV,DV Impulse event at 05/10/2000 09:48:18.48

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	66.4	66.3	67.0	244.0	306 deg	1
BV Volts	33.8	33.4	111.8	-898.0	306 deg	1
CV Volts	2.9	0.0	2.5	-720.0	223 deg	1
DV Volts	7.3	0.1	6.4	2159.0	223 deg	1

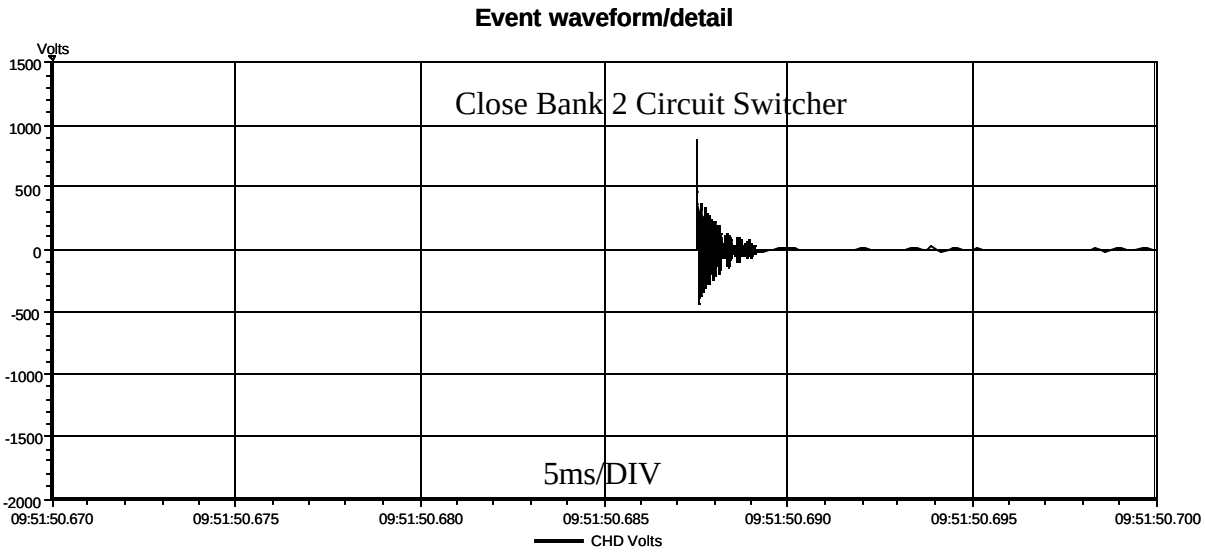
FIG 23: Otis Orchards tests of 5/10/00. Close bank 1. Show CH-D only (AV=AØ-N bus PT's, BV=AØ-N on bank 1, CV=AØ-N on bank 2, DV=N-GND on bank 1). Worst V IMP = 2159 N-GND on bank 1.



BV,CV,DV Impulse event at 05/10/2000 09:51:50.61

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	65.5	66.1	67.7	0.0	0 deg	0
BV Volts	109.4	110.3	112.5	-166.0	237 deg	1
CV Volts	0.1	0.1	112.2	244.0	237 deg	1
DV Volts	0.8	1.1	17.8	876.0	103 deg	1

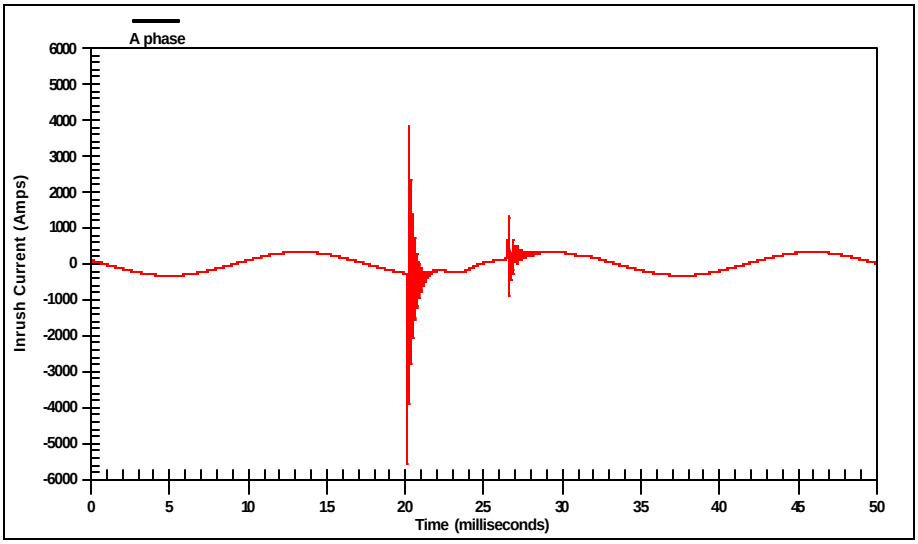
FIG 24: Otis Orchards tests of 5/10/00. Close bank 2. Show CH-A only (AV=AØ-N bus PT's, BV=AØ-N on bank 1, CV=AØ-N on bank 2, DV=N-GND on bank 1). Worst V IMP = 876 N-GND on bank 1.



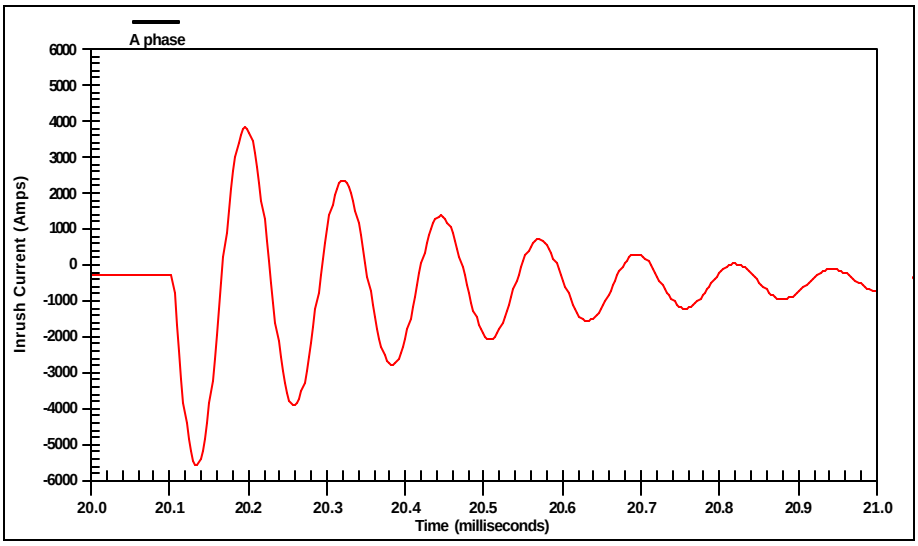
BV,CV,DV Impulse event at 05/10/2000 09:51:50.61

	PrevRMS	MinRMS	MaxRMS	WorstIMP	Phase	HFHits
AV Volts	65.5	66.1	67.7	0.0	0 deg	0
BV Volts	109.4	110.3	112.5	-166.0	237 deg	1
CV Volts	0.1	0.1	112.2	244.0	237 deg	1
DV Volts	0.8	1.1	17.8	876.0	103 deg	1

FIG 25: Otis Orchards tests of 5/10/00. Close bank 2. Show CH-D only (AV=AØ-N bus PT's, BV=AØ-N on bank 1, CV=AØ-N on bank 2, DV=N-GND on bank 1). Worst V IMP = 876 N-GND on bank 1.

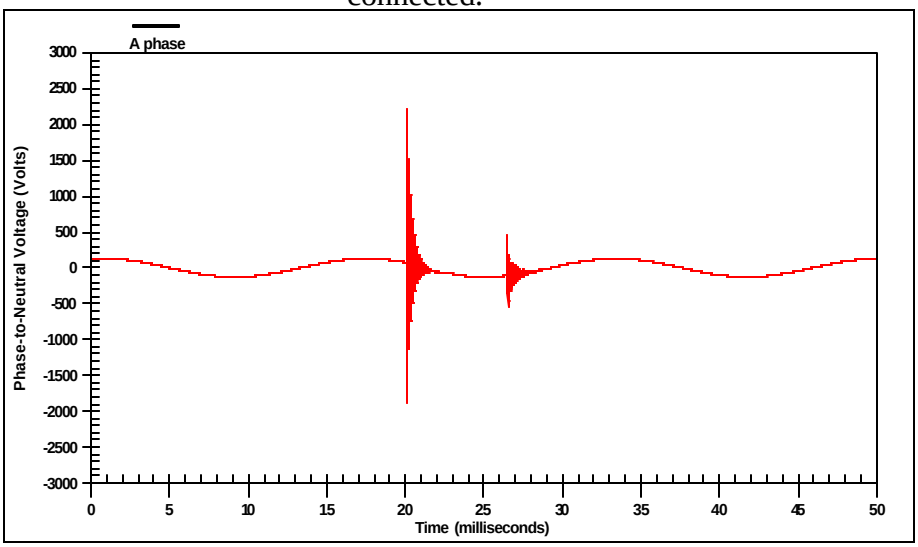


(a)

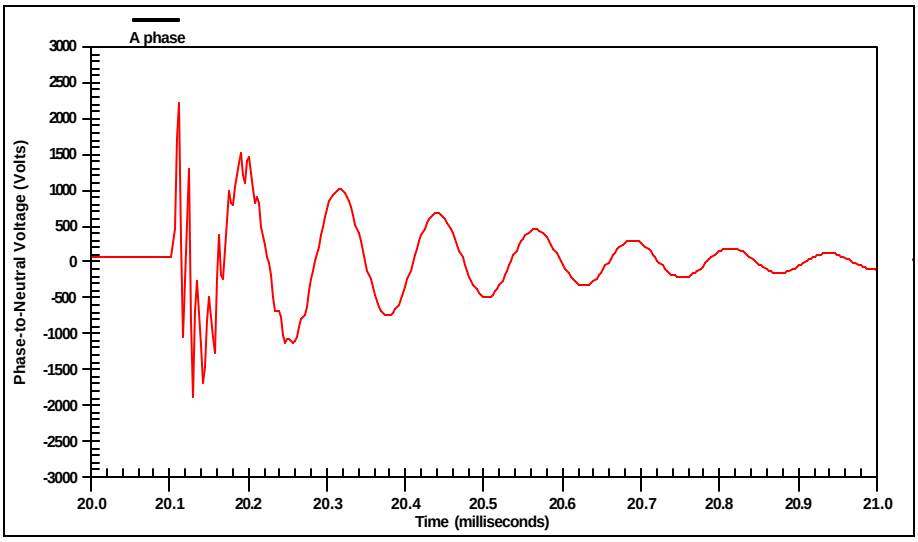


(b)

FIG 26: Inrush current into A phase of capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #1. Bank #2 is already connected.

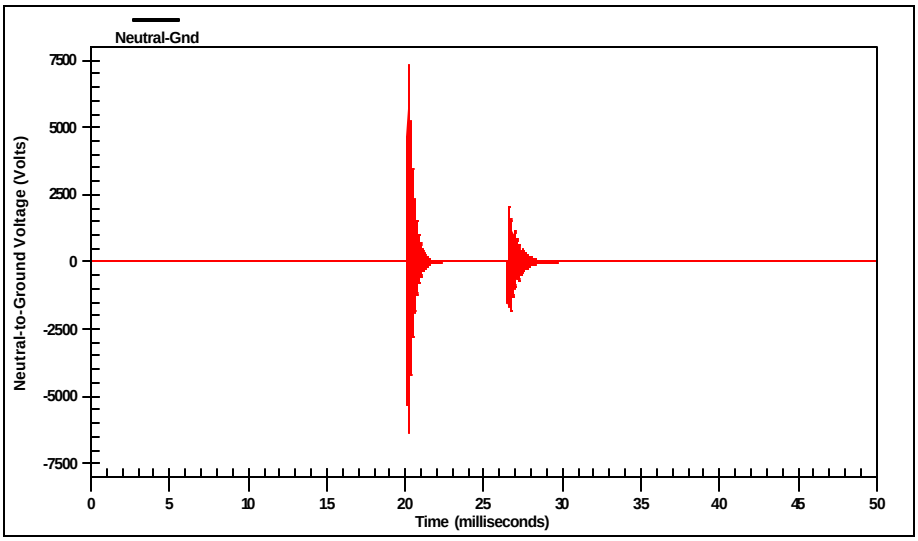


(a)

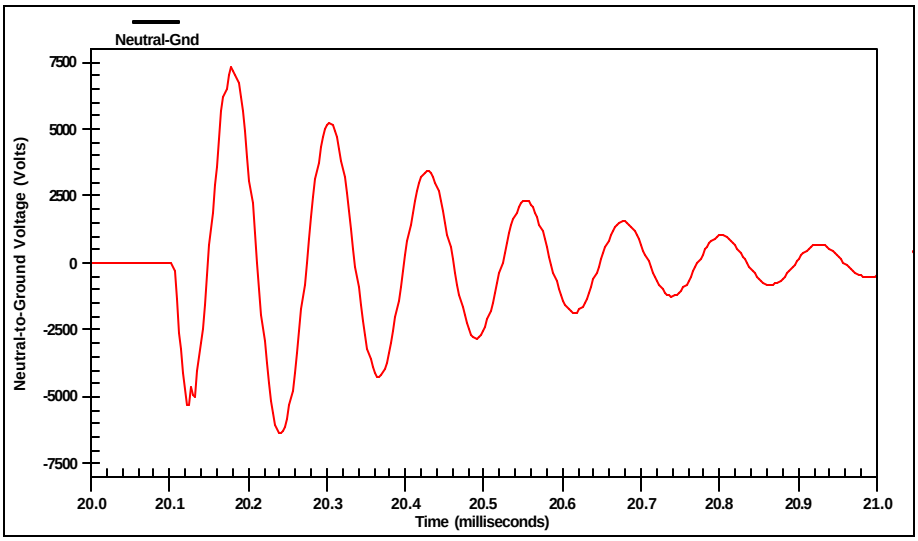


(b)

FIG 27: Phase-to-neutral voltage at input of SEL 287V relay on A phase of capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #1. Bank #2 is already connected. PT secondary neutral is grounded in the switchyard and 200 ohm burden resistors are connected to the PT secondary near the inputs to the relay. Compare waveform (a) with test recording in Figure 13.



(a)



(b)

FIG 28: Neutral-to-ground voltage at input of SEL 287V relay of capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #1. Bank #2 is already connected. PT secondary neutral is grounded in the switchyard and 200 ohm burden resistors are connected to the PT secondary near the inputs to the relay. Compare waveform (a) with test recording in Figure 14.

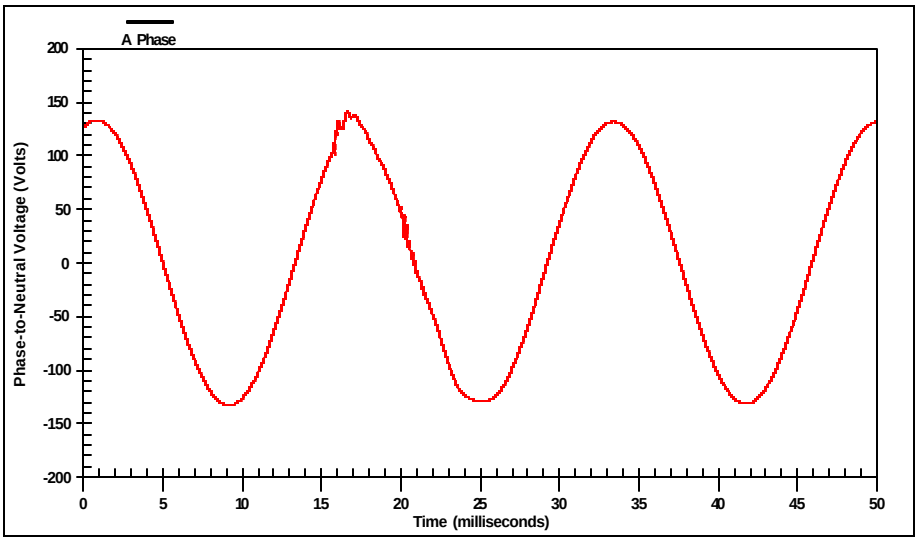
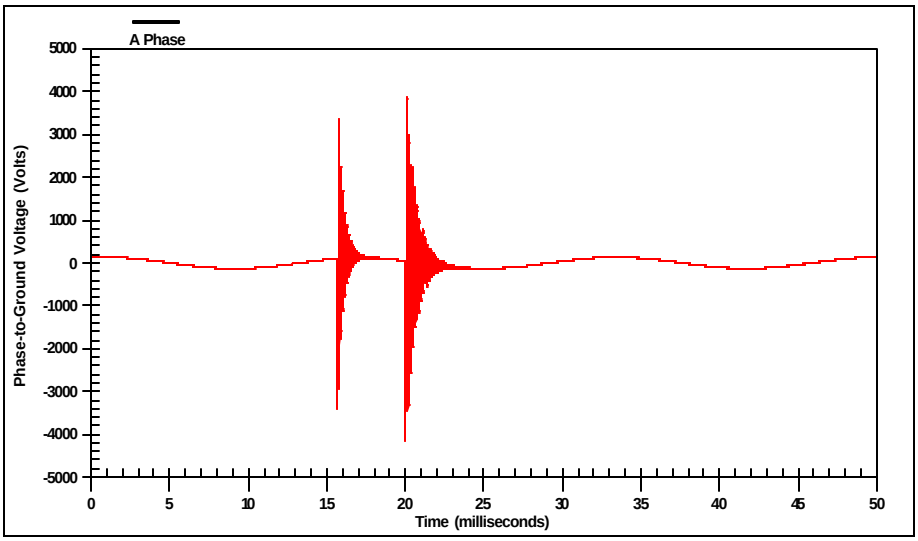
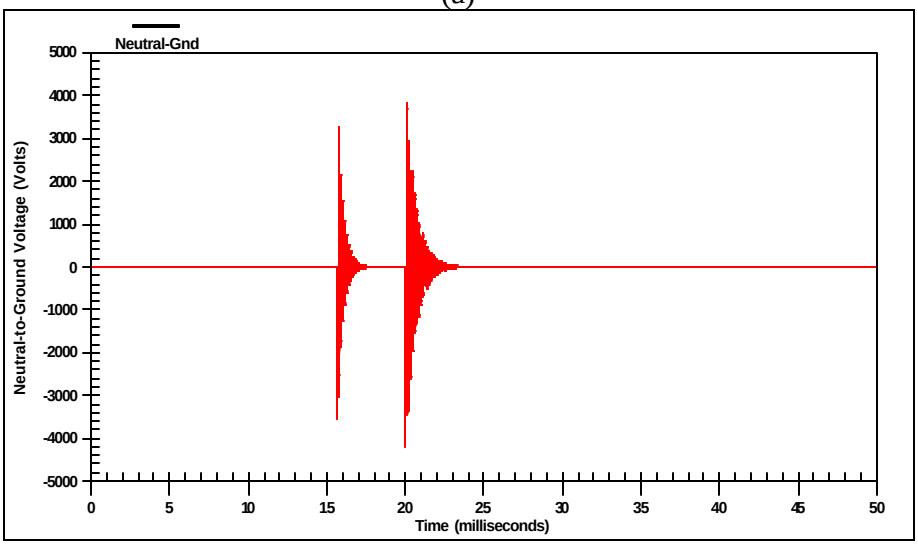


FIG 29: Phase-to-neutral voltage at input of SEL 287V relay on A phase of capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #2. Bank #1 is already connected. PT secondary neutral is grounded in the panel house and RC surge suppression circuits are connected to the PT secondary near the inputs to the relay. Compare waveform with test recording in Figure 18 when inductor is bypassed.



(a)



(b)

FIG 30: (a) Phase-to-ground voltage on A phase and (b) neutral-to-ground voltage at PT secondary terminals of capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #2. Bank #1 is already connected. PT secondary neutral is grounded in the panel house and RC surge suppression circuits are connected to the PT secondary near the inputs to the relay.

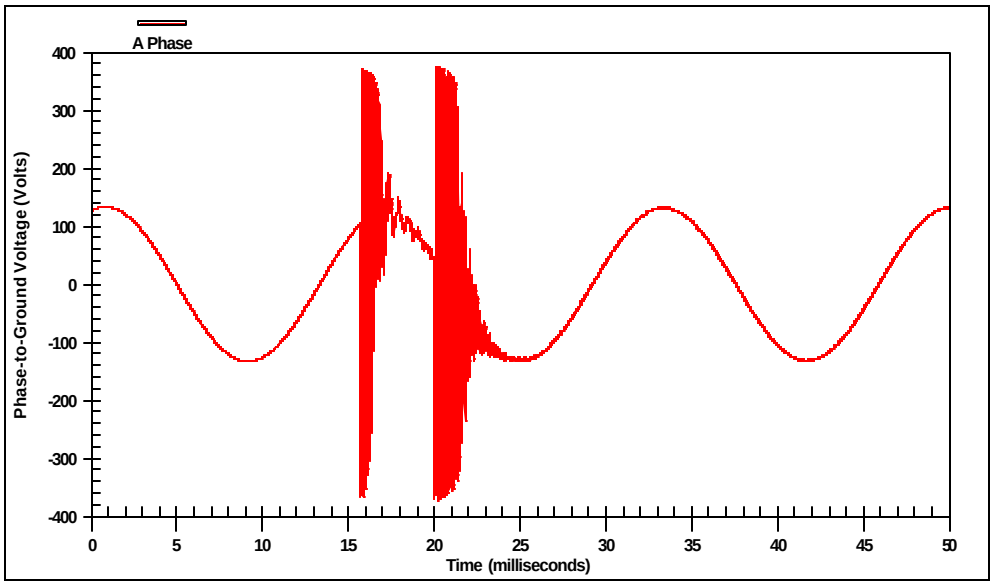


FIG 31: Phase-to-ground voltage at the PT secondary terminals on A phase of capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #2. Bank #1 is already connected. PT secondary neutral is grounded in the panel house and RC surge suppression circuits are connected to the PT secondary near the inputs to the relay. MOVs are connected to the PT secondary terminals.

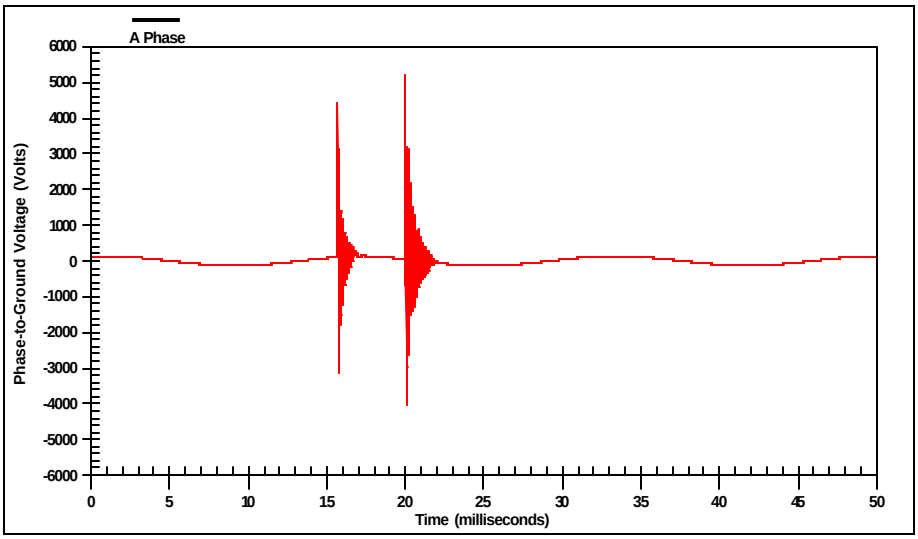


FIG 32: Phase-to-ground voltage on A phase of PT secondary cable for capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #2. Bank #1 is already connected. Voltage measured approximately 92 ft from PT secondary terminals. PT secondary neutral is grounded in the panel house and RC surge suppression circuits are connected to the PT secondary near the inputs to the relay. MOVs are connected to the PT secondary terminals.

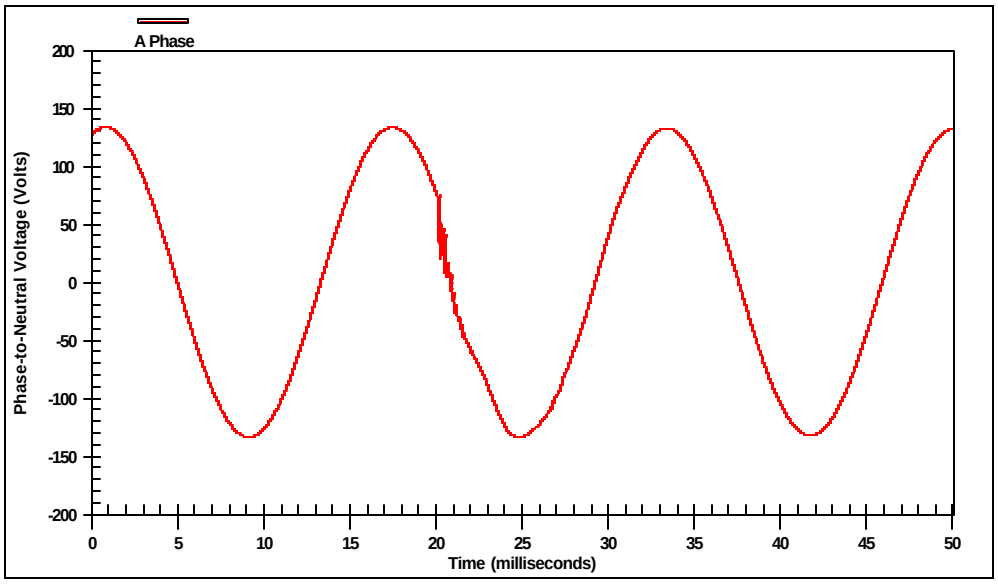


FIG 33: Phase-to-neutral voltage at input of SEL 287V relay on A phase of capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #2. Bank #1 is already connected. PT secondary neutral is grounded in the panel house. No surge suppression circuits are used. PT secondary cable is shielded with 1-inch conduit grounded every 10 ft.

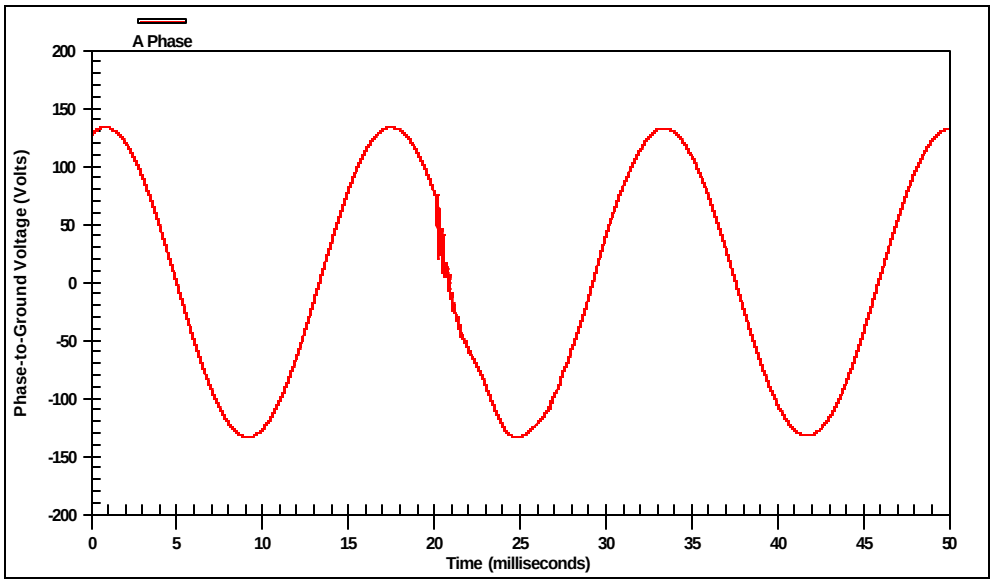


FIG 34: Phase-to-ground voltage at the PT secondary terminals on A phase of capacitor bank #1 when bypassing pre-insertion inductor during closing of Circuit-Switcher to energize bank #2. Bank #1 is already connected. PT secondary neutral is grounded in the panel house. No surge suppression circuits are used. PT secondary cable is shielded with 1-inch conduit grounded every 10 ft.