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## SUMMARY

The paper describes a microprocessor based current differential relay designed for use with digital communications systems for the protection of two ended or multi-ended feeders. The case for using the current differential method and the advantages of the relay are discussed. The requirements of digital communication systems, with the emphasis on optical fibre systems, both multiplexed and dedicated, are addressed. Considerations influencing the design of the relay, its principles of operation including digital filtering, synchronisation and tripping criteria are covered together with an outline of the hardware and operator interface. Prototype relays have been tested in field trials involving staged switching, fault throwing and error injection tests, the results of which are presented.

Figure 1. THE TYPE LFCB CURRENT DIFFERENTIAL RELAY

## 1.0 INTRODUCTION

Current differential relays can provide unit protection for simple two ended feeders or for more difficult multi-ended circuits without the restrictions associated with other forms of protection. A higher proportion of new transmission circuits and extensions are likely to involve multi-ended arrangements, due to economic and environmental considerations in transmission design and planning. The savings in land usage and overall cost which result from multi-ended connections favours their increased application.

Inherent in the current differential method of protection is the need for dependable communication channels linking the various circuit ends. This communication has traditionally been carried out using continuous metallic circuits between line ends which has limited the protected feeder length due to resistance and capacitance effects. When privately owned circuits are not available, metallic circuits, normally of speech type, have to be rented from a telecommunication company. However, with the extensive use of electronic signal repeating and multiplexing equipment in modern electronic and digital telecommunications systems, direct signalling of power frequency signals over rented circuits is becoming less feasible.

There is, therefore, a need for a new generation of current differential relays suitable for longer line application, designed to exploit the advantages of modern digital communication facilities. The advent of digital communications has also enhanced the prospects for wholly digital relays. This paper describes a microprocessor-based current differential relay for use with digital communication systems, as shown in Figure 1.

## 2.0 THE ADVANTAGES OF CURRENT DIFFERENTIAL PROTECTION

In making a general comparison between current differential and distance protection the former emerges with a number of advantages which make it an excellent alternative or complementary method to the latter. Because current differential protection does not rely on voltage measurement it does not have the problems of distance protection with CVT transients, low system impedance ratio (SIR) and three phase close-up faults. It is inherently immune to effects of power swing and mutual coupling on parallel lines and is particularly suitable for applications such as series compensated lines where reversal of line voltage can occur for some faults which may cause their distance relays to lose directional discrimination. If the differential measurement is made on a per phase basis then better phase selection for indication and single pole tripping can be obtained for close-up faults than for highly cross polarised distance relays. Furthermore the method provides a more consistent operating speed over the whole protected line than distance protection.

With respect to multi-ended circuit protection, current differential protection has additional benefits. Distance protection of the under-reach (permissive type) or over-reach (blocking type) has been successfully applied to teed circuits. However, the successful application of these schemes depends on such factors as the impedance of the individual branches, the source impedance at the feeder ends and the impedance of parallel branches, which, coupled with a high source impedance at one or more ends may result in current flowing out of one branch during an internal fault.

As an alternative to an overall scheme it is sometimes possible to sectionalise the feeder into two or three separate zones. Unless the arrangement is simple, e.g.

one where the tee connected terminal is directly on the circuit, then invariably additional current and/or voltage transformers will have to be established at some intermediate point. In addition to the extra cost involved, longer fault clearance times which may result under certain fault conditions may preclude such a scheme.

Clearly, the available protection arrangements can in some instances cause constraints on system design. There is therefore a need for a multi-ended feeder protection that can be applied to a wider variety of circuit configurations. It is considered that a modern design of current differential protection should therefore meet this requirement.

## 3.0 CURRENT PRACTICE AND TRENDS IN CURRENT DIFFERENTIAL RELAYS

Traditionally, current differential protection has been provided by schemes requiring continuous metallic circuits between line ends for the communication of a 50/60 Hz ac replica of the primary current. Such schemes are limited to primary circuits having a length of about 30 km due to the impedance of the communication circuit. These systems have provided good service for the protection of two ended circuits.

In the case of three ended applications, a design of biased current differential protection that employs a 4 wire metallic private circuit has been used. This scheme utilises summation current transformers to derive a single phase quantity, at each line end, that is a function of the three phase currents. The operating quantity of the differential relay is the vector addition of the single phase replica currents fed from each end, whilst the bias quantity is the arithmetic sum of the currents. The choice of operating and bias quantities in a teed feeder application is a critical one due to the multitude of current distributions that can occur due to different source impedances, fault position, fault types, current transformer saturation etc. It is also known that some schemes do not perform adequately for certain types of fault, such that failures to operate for some internal faults and maloperations for some external faults can occur.

The solution to correct biasing for a particular fault condition would appear to be to relay the instantaneous current information on a per phase basis and make the differential measurement for each individual phase. Recently, current differential relays of this type have become available and these generally make use of voice communication circuits. They are basically analog relays employing frequency modulation techniques to achieve the continuous comparison of instantaneous current. Whilst these relays represent a step forward in the field of multi-ended feeder protection the authors consider that an entirely digital approach will more fully exploit the benefits of modern digital communication systems.

## 4.0 DIGITAL COMMUNICATIONS SYSTEMS

The general development of high-capacity long-haul digital communication systems by telecommunications companies has made possible the introduction of such systems by power utilities. The emergence of privately and publicly-owned sections and networks has also increased the availability of digital communication systems for protection purposes and encouraged the development of digital relays.

A characteristic feature of digital communication systems is the multiplex structure leading to fixed bandwidths from basic 64 kbps channels. The CCITT standards adopted by most European systems recommend multiplexing 64 kbps channels into 2, 8, 34, 140 Mbps and even higher rate bit streams. A basic channel can be used to carry a 4 kHz bandwidth analog signal or a digital signal of 64 kbps. The standards adopted by North American systems are slightly different. The primary multiplexer typically operates at 1.544 Mbps. A basic channel, though also of 64 kbps, normally supports only 56 kbps data transmission, the remainder being used for signalling by the primary multiplexer.

Because analog voice band signals use the same bandwidth as a 56/64 kbps digital signal, the bandwidth requirements of analogue and digital relays with the same functions are different with the equivalent analogue system requiring many times the bandwidth of the digital system. It must be remembered in this context that the digital relay performs multiplexing of data for the different phases to achieve the low bandwidth requirement.

Adoption by power utilities of common standards, as used by telecommunication companies, enables standardisation of relaying hardware and software so that the facilities of privately-owned links and leased circuits are available to the power utilities and the most cost effective system configuration can be adopted. In addition this standardisation enables flexibility and availability of alternative communication routes so that in the case of failure of one path, another can be switched in.

Of the communications media presently used i.e. free space, copper and glass, it is the glass fibre-optic system that is currently receiving most attention by power utilities. Fibre-optic communications offer wide repeater spacing, wide bandwidth and noise-free signalling. The installation of fibre-optic cores associated with conductors is an obvious solution for a power utility's communications requirements. Fibre-optic cores embedded within power system ground wires is one method currently being used. In addition the helical wrapping of fibre-optic cores around phase conductors and the suspension of non-metallic optical cable between transmission towers is receiving much attention by power utilities. Such usage may enable them to use their rights-of-way for public telecommunications by leasing some of their channels to communication companies.

Whatever medium is used, the line termination equipment will in general be comprised of a pulse code modulation (PCM) system which enables data, voice, and other forms of signals to be multiplexed together. If the relay is a considerable distance from this terminal equipment, as is possible in a large electricity substation, the use of a subsidiary cross-site digital link based on fibre-optics is a possibility. This requires an interface unit to be situated close to the PCM equipment which has electrical inputs.

In addition to the multiplexed links the question of direct optical communication between relays has been considered. The use of dedicated optical fibres for current differential relaying purposes may be economic over short distances and the decision may be influenced by the need or otherwise for other traffic to share the fibre. It is considered that direct relaying over fibre

distances of around 20 km can be achieved without repeaters, provided a suitable choice of optical devices and fibre is made.

## 5.0 DESIGN CONSIDERATIONS

For digital signalling between relays it is important to select (as far as possible) a standard protocol, and as stated earlier, a suitable data rate. The HDLC protocol used in this relay is well supported with LSI controllers and is used in many computer applications. In addition, the use of Manchester coding on inter- and intra-substation dedicated links, enables clocking information to be sent without an increase in the number of communication channels. The relay is designed to work within the signalling bandwidth of a standard PCM channel, i.e. the data rate is limited to 64 kbps (CCITT systems) or 56 kbps (North American systems).

This enables power utilities who rely heavily on leased facilities from telecommunication companies to use this relay. However, the relay is capable of operating at much higher transmission rates with dedicated links. It is also capable of monitoring and self-compensating for changes in propagation delay times with leased lines.

An all-digital, microprocessor based design was the obvious choice for a relay targeted to work with a digital communication system. Analog relaying signals are sampled at regular intervals, converted into digital data, processed and transmitted through the communication link. A design problem with digital relays for unit protection is that digital data, unlike continuous analog signals, represents information at discrete time instants. Some form of synchronisation must, therefore, be provided so that digital data from different line ends can be aligned to the same instant before comparison of adequate sensitivity can take place. An external radio clock or a clock signal derived from the communication multiplexing equipment has often been proposed to synchronise the data sampling at all line ends. The radio clock approach adds cost and complexity to the relay due to the radio receiver, clock recovery and phase locking circuits concerned. It is doubtful that a suitable radio clock signal will be available to all users and even where it is available there could be serious reception problems at some locations. The derivation of a synchronised clock from the communication equipment, on the other hand, is very dependent on the actual design of the equipment, the network configuration and the control hierarchy adopted. As the relay would have to work with a variety of communication equipments, the cost of developing different clock interfaces could be prohibitive. Also a clock source may not be available if the relay is to be used over a direct non-multiplexed link. It is therefore preferable for the synchronisation to be provided internally by the relays. Then no external clock signal is required and synchronisation is independent of the type of multiplexing equipment used.

With all relay designs an important consideration is the operating speed requirement. It was decided at an early stage that an overall operating time from fault inception to trip output of around 1 to 1.5 cycles excluding channel propagation delay times, on a segregated phase basis, would provide adequate overall fault clearance times whilst still enabling the use of only one 64 kbps data channel. Faster operating times can be obtained, at the expense of a wider bandwidth requirement in the communication channels.

## 6.0 PRINCIPLE OF OPERATION

### 6.1 Data sampling and preprocessing

At each line end an internal free running clock controls the sampling of the three phase currents and the neutral current. Direct synchronisation of the samples is not therefore provided, leading to phase differences of up to one half the sampling period between the clocks at different line ends. Effective synchronisation is achieved by an alignment procedure described later.

The data samples represent the instantaneous values of current signals. These may contain d.c. offset, harmonic and high frequency components. The data is filtered and preprocessed to a form which enables the calculation of the magnitudes of differential and bias currents. The one-cycle window Fourier method is chosen for its stable transient characteristics. This algorithm can be expressed as:

$$I_S = \frac{2}{N}\left[\sum_{n=1}^{N-1} \sin n\omega\,\Delta t.\, i_n\right]$$

$$I_C = \frac{2}{N}\left[\frac{i_0}{2} + \frac{i_N}{2} + \sum_{n=1}^{N-1} \cos n\omega\,\Delta t.\, i_n\right] \quad (1)$$

where N — number of samples per cycle

$\omega$ — fundamental angular frequency

$\Delta t$ — sampling time

$i_n$ — instantaneous value of signal i sampled at time nt

$I_S$ — Fourier sine integral of signal i

$I_C$ — Fourier cosine integral of signal i

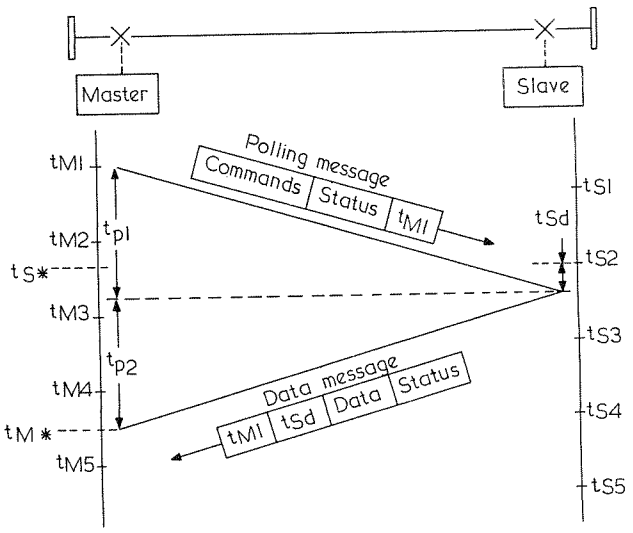
If the fundamental component of signal i is equal to $I \sin(\omega t + \theta)$, then it can be shown that:

$$I_S = I\cos\theta; \quad I_C = I\sin\theta \quad (2)$$

As the phase angle $\theta$ is related to the time reference of the data window, $I_S$ and $I_C$ are not static, but sinusoidal quantities.
The phasor $I = (I_S + jIc)$ represents a rotating vector from which the magnitude of i can be interpolated at any particular time.

### 6.2 Data Polling and the Measurement of Channel Delay Time

Consider Figure 2 which illustrates a two ended system for simplicity. Two identical relays, one defined as the 'master' and the other defined as the 'slave' are placed at the opposite ends of the line and, as previously described, perform data sampling and preprocessing. The master samples its current signals at time $t_{M1}$, $t_{M2}$ ... etc., the slave at time $t_{S1}$, $t_{S2}$ ... . Note that the sampling instants at the two ends will not, in general, be coincidental or of fixed relationship due to slight drifts in the sampling frequencies.




$t_{M1}, t_{M2}, \ldots$ — sampling instants of master relay

$t_{S1}, t_{S2}, \ldots$ — sampling instants of slave relay

$t_{p1}$ — propagation delay time from master to slave

$t_{p2}$ — propagation delay time from slave to master

$t_{Sd}$ — time between slave sampling and arrival of polling message

$t_{M*}$ — arrival time of data message at master

$t_{S*}$ — slave sampling time measured by master

Figure 2. DATA POLLING AND PROPAGATION DELAY TIME MEASUREMENT

Assume that, at time $t_{M1}$, the master decides to obtain current signal data from the slave end. A polling message containing a time tag $t_{M1}$ together with other command and status information is transmitted and arrives at the slave end after a channel propagation delay time of $t_{p1}$. The slave responds by returning the most recently sampled and filtered data back to the master. The returned data message contains the polling time tag $t_{M1}$, the time between the slave sampling and the arrival of the polling message $t_{Sd}$, the filtered $I_s$, $I_c$ data and the other status information. If the return channel delay time is $t_{p2}$, then the data message will arrive back at the master at time $t_{M*}$ where:

$$t_{M*} = (t_{M1} + t_{p1} + t_{p2}) \quad (3)$$

If the transmit and receive channels have the same propagation delay, then the channel delay time can be calculated:

$$t_{p1} = t_{p2} = \frac{1}{2}(t_{M*} - t_{M1}) \quad (4)$$

It should be noted that a new measurement of the channel delay time is carried out for each data poll and this can then be used to monitor any change on the communication link. In addition the time tag $t_{M1}$ has the effect of a random data check on the communication and helps to enhance the security of the system. Data error detection is primarily provided by cyclic redundancy checks performed by the HDLC protocol controller.

Additional checks such as length of message are also carried out in software.

Equations (3) and (4) represent a simplified view of the process. Details concerning the different delay and response times of the two relays and the transmission times of the polling message and the data message must be considered in the actual system. For a two ended system, a master-master arrangement may be adopted so that the relay can both poll and respond to a polling message at the same time. On multi-ended systems the all master arrangement allows the fastest tripping time and a greater system operation flexibility if one terminal is taken out of service for maintenance. A master-slave arrangement on multi-ended systems results in lower communication and processing requirements but slightly longer tripping times of the slave relays since the differential relaying decision is performed only by the master relay and the slaves must be intertripped in the case of an internal fault.

### 6.3 Time Alignment of Slave Data

With the measurement of the channel delay time, the sampling instant of the received slave data can be estimated from:

$$t_{S*} = t_{M*} - t_{p2} - t_{Sd} \quad (5)$$

In Figure 2, $t_{S*}$ is shown as equal to $t_{S2}$. The master should identify, therefore, that the slave data samples are taken at a time between $t_{M2}$ and $t_{M3}$. To calculate the differential and bias currents, these data samples must be time aligned to $t_{M2}$ or $t_{M3}$ respectively. As $(I_s + jI_c)$ represents a vector rotating in an anti-clockwise direction on the complex plane at angular frequency $\omega$, it is possible to interpolate the slave signals at $t_{M2}$ and $t_{M3}$ by transforming the vector information at $t_{S*}$.

Using a look-up table, the parameters, say (a + jb), to perform a phase shift corresponding to the time $(t_{M3} - t_{S*})$ can be obtained. The vector value of the slave current at time $t_{M3}$ can then be calculated as:

$$\begin{aligned} I_{S3} &= (I_S + jI_C)(a + jb) \\ &= (aI_s - bI_c) + j(bI_s + aI_c) \end{aligned} \quad (6)$$

The value of the slave current at time $t_{M2}$ can be obtained likewise by rotating $I_{S3}$ backward by a fixed angle corresponding to the sampling time period. As two data samples can be obtained from each data message, the polling process needs to be done only once every two samples, thus reducing the communication bandwidth requirement. The sampling rate chosen to be compatible with the 64 kbps data rate is 8 samples per cycle.

### 6.4 Tripping Criteria

If $I_A$, $I_B$, $I_C$ ... are the current vector signals calculated for line ends A, B, C ... of the protected circuit, then the differential current $I_{diff}$ and the bias current $I_{bias}$ are:

$$\begin{aligned} I_{diff} &= I_A + I_B + I_C + \ldots \\ I_{bias} &= \frac{1}{2}(|I_A| + |I_B| + |I_C| + \ldots) \end{aligned} \quad (7)$$

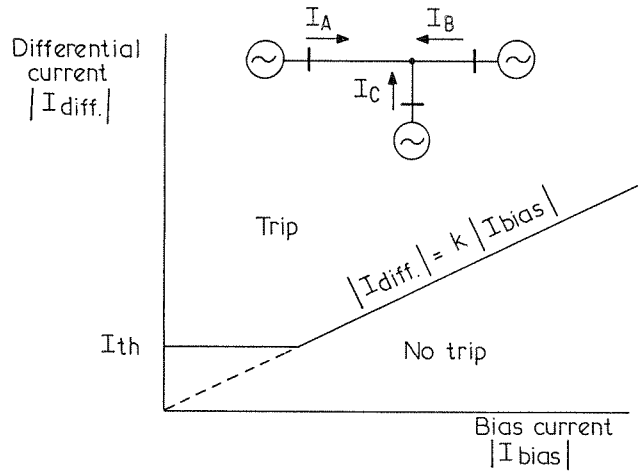



Figure 3. PERCENTAGE BIASED DIFFERENTIAL PROTECTION CHARACTERISTICS OF THE RELAY

A percentage biased differential characteristic is used (Figure 3) and the tripping criteria are:

$$|I_{diff}| > k.\ |I_{bias}| \quad (8)$$

and $|I_{diff}| > I_{th}$

where k is percentage bias setting

$I_{th}$ is minimum differential current setting

Given the vector components $I_S$ and $I_C$ of a current signal i, the amplitude $|I|$ is equal to:

$$|I| = \sqrt{I_S^2 + I_C^2} \quad (9)$$

For microprocessor implementation, a linear approximation technique may be used to calculate $|I_{diff}|$, $|I_A|$, $|I_B|$, $|I_C|$, ... from their corresponding vector components.

The relay can self manipulate the threshold and bias settings, and the sample count for trip to produce an adaptive characteristic for improved sensitivity and stability. A higher bias setting is used for example for heavy fault current, and a larger sample count is required for tripping if the communication error rate is high.

## 7.0 RELAY HARDWARE AND OPERATOR INTERFACE

The relay is housed in a 4U (177.8 mm) high case, suitable for 19 inch rack or panel mounting, containing a number of functional modules. These include a current input module which accepts signals from conventional CTs and in which analog to digital conversion takes place. Another contains hinged armature relays used for trip and alarm outputs.

A computing module based on a 16 bit microprocessor is used to process the protection algorithms. This module contains three types of memory: erasable programmable read-only memory (EPROM) where the relay programs are stored; random access memory (RAM) where data are stored temporarily and electrically erasable and programmable read-only memory (E2PROM) where selected setting values and other non-volatile information is stored.

A high performance serial communications interface provides two independent channels for signalling between relays These are based on the high level data link control (HDLC) protocol and are capable of operating at speeds up to 1 Mbps.

The relay is powered from an external battery and has been designed to have a low standing drain. It consumes 10W approximately in the quiescent state. Power supply modules are available to cover most of the common battery voltages.

Terminals and optical connectors are mounted at the rear of the case.

The operator interface, shown in Figure 4, consists of a 2 row × 16 character alpha-numeric liquid crystal display (LCD) together with a keypad of 7 push-buttons.

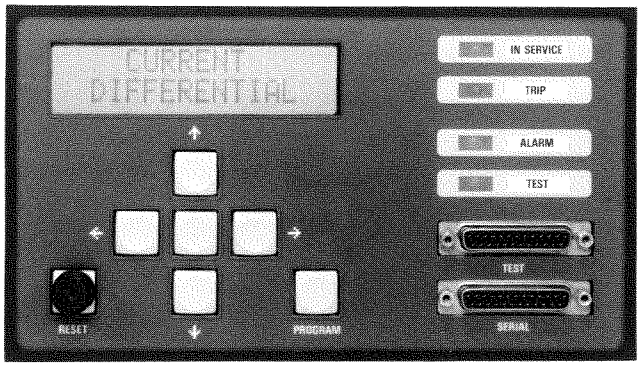



Figure 4. OPERATOR'S KEYPAD AND DISPLAYS

The information available for display includes phase, differential and through current magnitudes at local and remote ends, fault current magnitudes, alarm records, communication error statistics and setting values. Individual items are selected for display using the push-buttons which effectively act as cursor keys, driving the display in a 'menu' style familiar in digital instrumentation. For example, in order to select a setting value the keys are used to step through the range of available values. When the target value is reached a special key called 'PROGRAM' is pressed to select it as the new setting.

The relay also has two 25 pin D style sockets mounted on its front panel. One provides a serial communication port based on the RS232C standard. The other is a test port intended to assist field testing of the relay by computer based equipment.

## 8.0 FIELD TRIALS

A prototype, master-slave configured, three ended system of digital current differential protection has been installed in a field trial on a 400 kV circuit in the UK. This overhead line circuit, which has a route length of about 21 km, has had its ground wire replaced with a composite type containing an optical cable (1). Two 50/125 um multi-mode fibre in the optical cable have been connected to 34 Mbps PCM equipment located in telecommunication equipment rooms at the substations. There is a single tower-mounted regenerator located at the approximate mid point of the circuit. The telecommunication system has the capability of transmitting 480 voice/data channels although only 26

voice channels and 4 data channels have been provided at present. Access to the data channels is at 64 kbps using contradirectional signalling to CCITT recommendation G703.

The relays are located within dispersed relay rooms close to the high voltage electrical equipment and remote from the telecommunications room. In order to ensure communications free from electrical interference, and to provide electrical isolation between the hostile environment of the substation and the electrically quieter environment of the telecommunications room, cross-site optical fibres have been installed.

The location of the relays and their associated communications is shown in Figure 5. Communication between the master relay, B and slave relay C is via the 34 Mbps optical telecommunications equipment. Optical links of 650m and 250m connect the master and slave relays, respectively, to the PCM equipment via microprocessor controlled interface units. These interface units convert Manchester code on the optical side at 200 kbps to electrical AMI code at 64 kbps and are located in a separate rack close to the PCM equipment terminals.

Communication between master and slave A relays is via a dedicated optical link, about 250m long. The cross-site optical systems make use of 50/125 um fibre and SMA style connectors.

The connection to current transformers is also shown in Figure 5. The scheme has been devised so as to simulate a teed feeder arrangement. The zone for internal faults, i.e. relay operation, is shown by a heavy line.

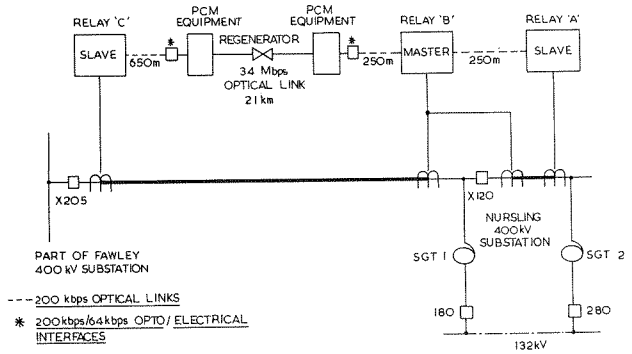



Figure 5. ARRANGEMENT FOR 400 kV CIRCUIT FIELD TRIAL

The field trial has been implemented in order to evaluate the performance of this novel design in an actual power system environment. As a part of the longer term trial the performance has been monitored during specially staged system switching and fault throwing tests. The reliability and freedom from electrical interference of the protection and its associated communication equipment has been investigated during operation of 400 kV circuit breakers and disconnectors. In addition the dynamic performance of the protection has been assessed during primary system faults internal and external to the zone of the feeder protection. The system test details are given in Table 1.

A total of ten system faults were applied to the 400 kV circuit during September 1985. Two faults involved phase-phase-ground connection whilst the remainder were of single phase-ground types, five of which were arcing faults applied to the circuit while energised from both ends. Some faults were positioned close to the telecommunication equipment (terminal and regenerator equipment) and some to the protection relays.

For faults A1, A2 and B nearly 100% dc offset of the fault current was achieved by controlling the point on wave of closure of a circuit breaker at Fawley substation. Faults C and D were also switched types but applied from the Nursling substation end. Faults E, F, G, H and I were applied to the live circuit by specially developed fault throwing apparatus. Fault G was mainly resistive by virtue of an arc length of approximately 11 metres and a 4 ohm liquid grounding resistor connected into the fault path. For Tests H and I there was a prefault load current flowing of between 100 and 200A.

The magnitude of the fault currents was relatively modest in comparison with possible system fault levels. This was a necessary result of the need to minimise the effects on system security, reduce the risk to plant and restrict voltage depressions to an acceptable level.

The objective of the field trial was to subject the relays to a power system environment, particularly the effects of electrical interference generated by fault arcs and by the operation of circuit breakers and their associated disconnectors. For faults B, F and I, the fault arc was approximately 5 metres from the master differential relay (end B) and although no quantitative figures are available, the ground fault currents of up to nearly 10 kA would have produced a relatively high transient ground potential rise. Furthermore the electromagnetic and electrostatic and radio frequency interference produced by the faults are considered to have been demanding conditions for the relays.

## 9.0 PERFORMANCE OF CURRENT DIFFERENTIAL RELAYS

A microprocessor monitoring system has also been installed with each relay to record current, voltage and relay logic signals. The recorder is arranged to trigger for system disturbances or relay logic operation and a post-incident record can be obtained.

During all the tests the performance of the relays was correct.

The threshold setting of the master differential relay was set to 1A and the bias setting to 50% for all tests except Test A2. In this test, which was a repeat of Test A1, the opportunity was taken to observe the effect of reducing the threshold setting to 0.25A. In addition, the number of consecutive tripping decisions for the relay to produce an output, was reduced from four to three for Test A2. The effect of the increased sensitivity was to produce a marginally faster operating time.

The operating time of the master relay was around 30 ms. The master to slave intertrip times were between 2 and 6 ms. The variation was caused by intertrip messages being sent at discrete sampling intervals of 5 ms only. The master end operating times were constrained by the time required to transmit the 64 kbps polling message and receive the date message. The loop delay time measured over the optical pcm link was 11 ms and this includes master-end and slave-end processing delays.

| Test No. | Fault Location | Type of Fault | | | Fault Phase Current Distribution (kA) End A | End B | End C |
|---|---|---|---|---|---|---|---|
| A1 | Mid Point | B—G | Internal | Fuse Wire | 0 | 0.3 | 8.4 |
| A2 | Mid Point | B—G | Internal | Fuse Wire | 0 | 0.3* | 8.4* |
| B | Nursling | C—G | External | Fuse Wire | 0 | 7.5 | 7.5 |
| C | Fawley | A—B—G | Internal | Solid | 5.5/5.7 | 0.3/0.3 | 0/0 |
| D | Fawley | A—B—G | External | Solid | 5.5/5.7 | 0.3/0.3 | 5.6/5.8 |
| E | Nursling | A—G | Internal | Arcing | 4.0 | 0.3 | 3.2 |
| F | Nursling | C—G | External | Arcing | 4.0 | 7.5 | 3.2 |
| G | Mid Point | B—G | Internal | Arcing | 2.9 | 0 | 4.0 |
| H | Nursling | A—G | Internal | Arcing | 4.4 | 0.3 | 5.0 |
| I | Nursling | C—G | External | Arcing | 4.4 | 9.4 | 5.0 |

* Simultaneous external fault on C phase. Phase current was 1.6 kA at ends B and C.

TABLE 1 SYSTEM TEST DETAILS

In Figure 6 the A phase and neutral current at each end is illustrated for test H, together with the relay trip outputs. For relays A and C the neutral and phase currents are similar in magnitude but for relay B, since the infeed is low and primarily zero sequence current, the neutral current is approximately three times larger than the phase current.

The performance of the current differential protection during external faults was entirely satisfactory. In Test A2 which was intended as a B phase-ground internal fault, a simultaneous C phase-ground external fault developed as a result of a switching overvoltage. It was observed that the phase segregated system stabilised on C phase whilst operating correctly on B phase.

Before the protection trial began, a number of communication trails were completed. These indicated that the errors on the digital links were low and typically in a two week period, only eight messages (120 bits at 64 kbps sent every 10 ms) were in error out of a total of $120 \times 10^6$ messages.

There were no digital errors recorded during application of faults or during 400 kV switching operations. Some errors were recorded at other times although these can be attributed to known causes.

In December 1985 a series of tests was carried out which involved the injection of bit errors into the 34 Mbps multiplexed data in order to investigate the possible effect of bit errors during operational service. Both evenly spaced and randomly spaced bit errors at varying bit error rates were applied. The highest rates were around $10^{-3}$, near which the PCM system itself is liable to be shut down by its internal monitoring circuits.

The current differential protection remained stable throughout, correctly recording the incidence of error messages. The ability of the relays to operate in the presence of similar high rate bit errors was also demonstrated when current was injected into one phase of the master relay. The relays tripped with no noticeable delay in operating time.

A two-ended 'all-master' configured system will be evaluated in a further field trial by an overseas utility.

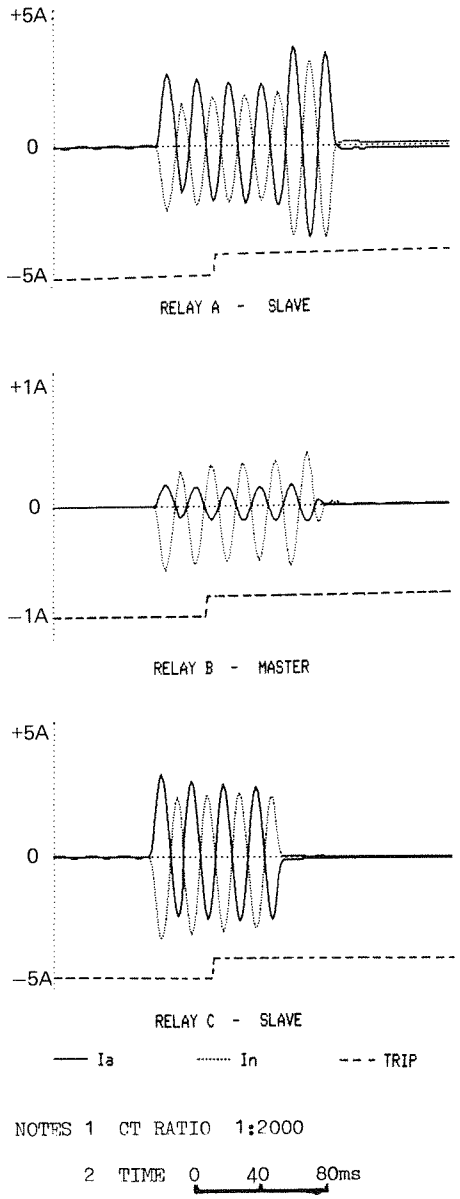



Figure 6. PERFORMANCE OF CURRENT DIFFERENTIAL RELAY DURING FAULT H

## 10.0 CONCLUSIONS

This paper has brought together those elements required to form an all-digital approach to the current differential protection of two ended and multi-ended feeders. At the centre of the scheme lie the digital communications which, in the trial installation, involves a PCM interface enabling signal multiplexing over a fibre-optic link embedded in the ground wire of a 21 km length of overhead transmission line.

The digital protection relay transmits and receives the digital representation of each phase current and hence makes a phase by phase differential measurement to indicate an imbalance caused by a power system fault.

The authors believe that the drive for digital communications will continue, fuelled primarily by parallel developments in the public telecommunications area, and will encourage a long term demand for all-digital solutions to protection problems.

The trial installation climaxed in a series of staged power system faults during Autumn 1985. The performance of the prototype digital current differential protection during 400 kV system switching and fault throwing tests was completely satisfactory. The relays operated when required for internal faults and remained stable for external faults. These prototype relays will continue to be evaluated as a part of the long term system trials.

A commercial version of the relay will be available shortly. This will be based on the 'all-master' configuration for both two ended and three ended circuits. Such arrangements improve operating speed since intertripping is not required and also improve operational flexibility on multi-ended lines. This version will operate at a higher sampling rate, 12 instead of 8 samples/cycle. An operating time of approximately one cycle is achieved.

## 11.0 ACKNOWLEDGEMENTS

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## 13.0 NOMENCLATURE

| | |
|---|---|
| CCITT | International Telegraph and Telephone Consultative Committee |
| PCM | Pulse Code Modulator |
| AMI | Alternate-Mark-Inversion |
| HDLC | High Level Data Link Control |
| LSI | Large Scale Integrated |

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