Transients (Old and New) Affect Protection Applications

Presented to
Western Protective Relay Conference 2009
Spokane, Washington, USA

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Introduction

This paper examines the impact of transients on application and setting of protective relays. It focuses primarily on unusual transients.

Many transients are already well recognized in the field of power system protection. Their effects are mitigated by application or setting of the protection systems including suitable design of the system, increased margins in settings, and suitable time delays to override transient conditions.

Other transients are not as well recognized or as frequently encountered. In this paper, the authors will share their experiences with other less widely reported transient conditions that have either required special settings or design of the protection system to mitigate them. It is the authors' hope that this paper will increase the awareness of other protection engineers of other transients which may require mitigation measures.

Background

Short circuits themselves are transients. The power system is not viable with a steady state short circuit applied. Notwithstanding their transient nature, short circuits are modeled as steady state for the purposes of calculating quantities that a relay should measure to discriminate between faults and acceptable (normal) conditions.

The challenge for protective relays then is to ignore the transients that are present, though not modeled in conventional short circuit studies, while paying full attention to the transient fundamental frequency components that are modelled in the short circuit studies.

Transients can be classified into two broad categories – those that originate in the primary power system, and those that are spurious, produced by the instrument transformers and/or secondary wiring connected to the relays. This paper designates the former as "primary" transients, and the latter as "secondary" transients. Within those two categories, infamous and insidious transients are also classified in this paper.

Primary transients

Infamous

This section is called infamous because the transients described here are well known and widely reported in the literature. They are mentioned here only for completeness and to provide references (such as [1]) for the interested reader.

Transient Offset of Fault Current.

This phenomenon is the transient offset of primary ac fault current from the zero current point. It is perhaps the most infamous of all primary transients. As shown in Figure 1, both the peak and rms values of the current will be higher when the offset is present than when it is not.

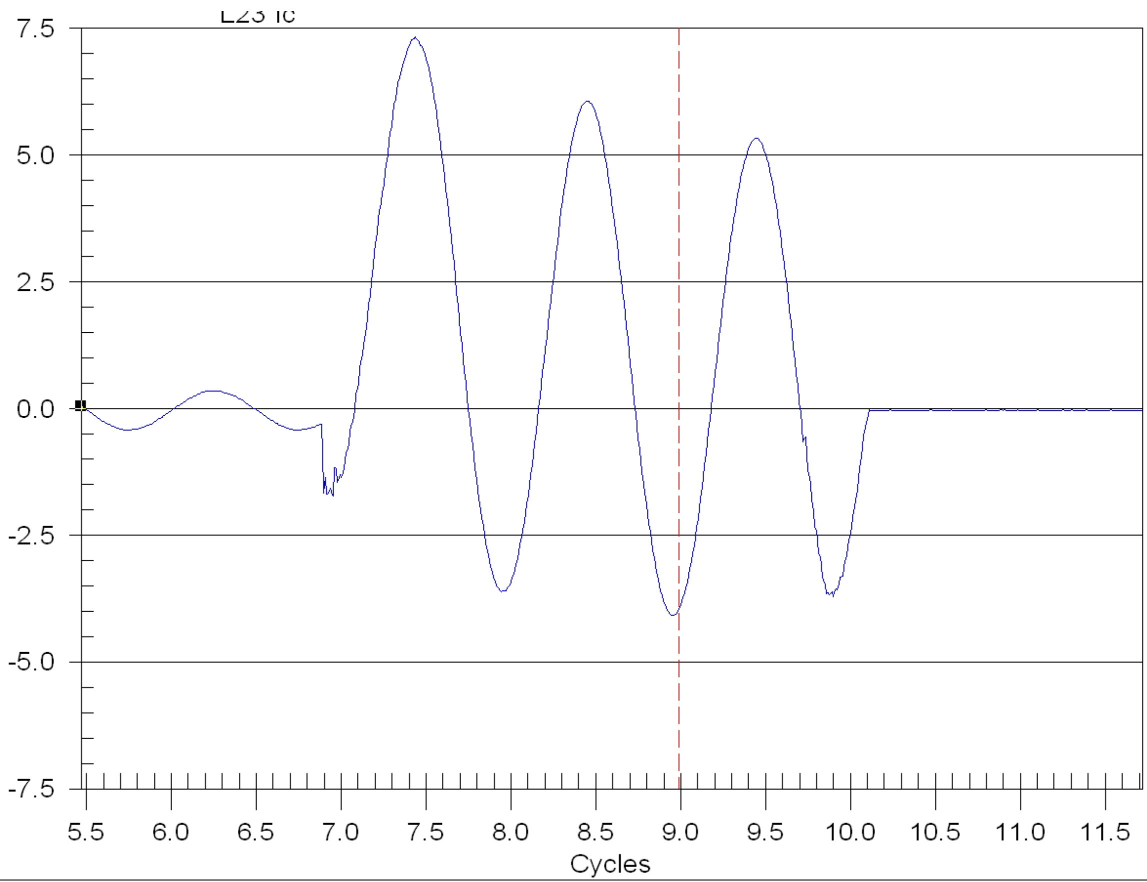

Figure 1 - Transient DC Offset

The offset appears in short circuits because there is low probability of a short circuit occurring precisely at a natural current zero. In an inductive circuit, such as a power system, current cannot change instantaneously. Therefore, if a fault occurs at any instant other than a natural current zero, the ac component of fault current will be transiently offset for a period of time depending on the X/R ratio of the system. Relays which are sensitive to peak or rms quantities may measure more current than the fundamental frequency component of fault current. This may cause them to overreach [1, 2]. The phenomenon is well recognized by relay manufacturers and users, and mitigated either by designing the protection to be sensitive only to the fundamental frequency component, or by using appropriate margins in relay settings to accommodate the transient overreach.

Harmonics

Responses of protective relays to harmonics are various [3, 4, 5]. Many relays will filter out all except fundamental frequency, however some relays use information in harmonics to operate or restrain as desired. Third harmonic currents and multiples of third harmonics are often more significant in zero sequence quantities than in phase, positive, or negative sequence quantities. Harmonics can affect the accuracy of devices measuring distorted currents and voltages. The effects of harmonics can be mitigated by designing the power system to minimize the creation of harmonics or by designing relays to respond as desired in the presence of harmonics. Ground relays for instance often include special filtering to minimize their response to triplen harmonics that do not sum to zero at fundamental frequency.

High frequency travelling waves caused by faults

The sudden appearance of a short circuit will cause a fast wave front to travel along a transmission line. This wave will be reflected from the ends of the line and appear as a high frequency distortion of the currents and voltages on the line.

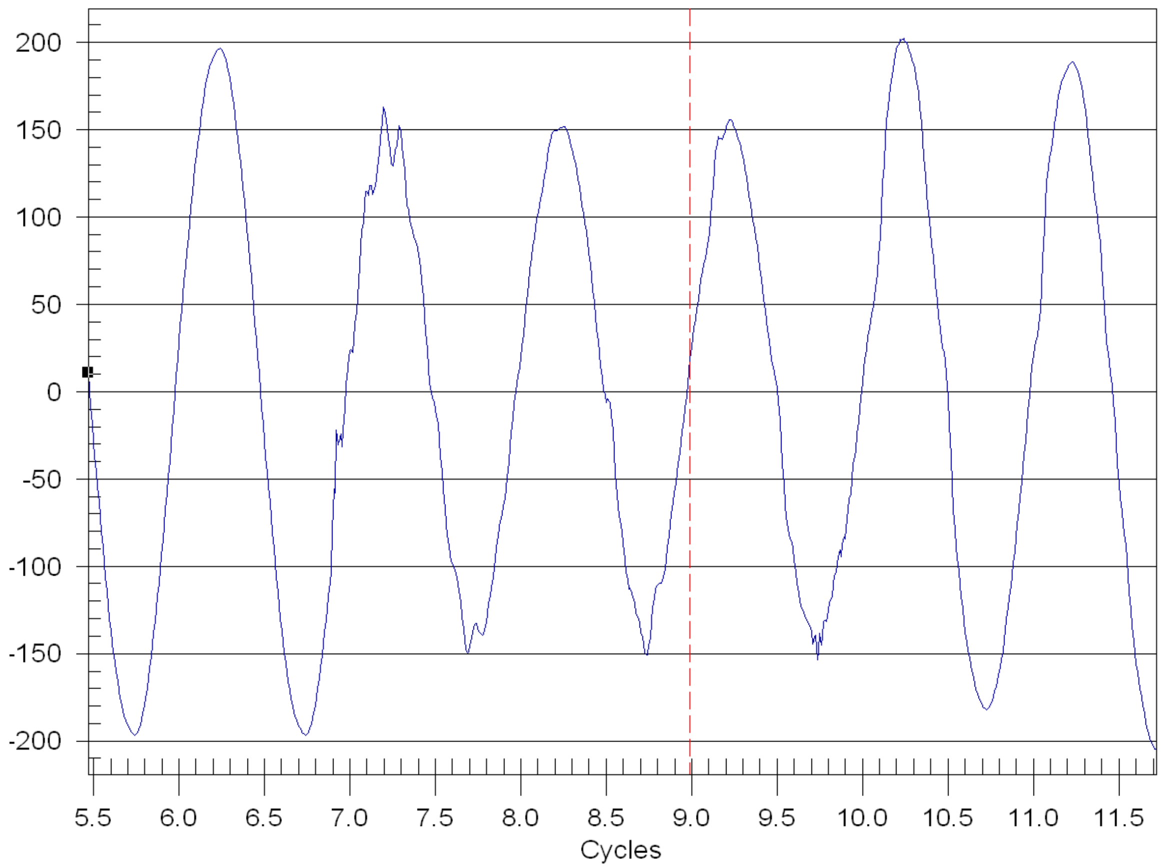

Figure 2 - High frequency distortion of voltage signal

Figure 2 shows the high frequency distortion of the fundamental frequency voltage during the first power frequency cycle of the fault. This high frequency distortion could cause difficulty for relays to accurately measure fault quantities. Relays are usually designed with suitable filtering to remove the effects of this high frequency distortion. Since the frequency of these travelling waves is significantly higher than fundamental, very narrow band filters are not required to remove them.

Low frequency due to series capacitors

The resonant frequency of a transmission line series capacitor bank is usually lower than fundamental frequency. During a short circuit, this low frequency component can cause significant challenges to protective relay filtering circuits. In order to avoid delays associated with narrow band filters, relay filters are not usually notch filters and the superimposed low frequency component can cause distance relays with conventional filters (for example to remove high frequency components mentioned above) to lose accuracy. **Error! Reference source not found.** shows the low frequency distortion of the fundamental frequency current during a short circuit on a series compensated transmission line. The distortion can most readily be observed on the unfaulted phase (A and B) currents.

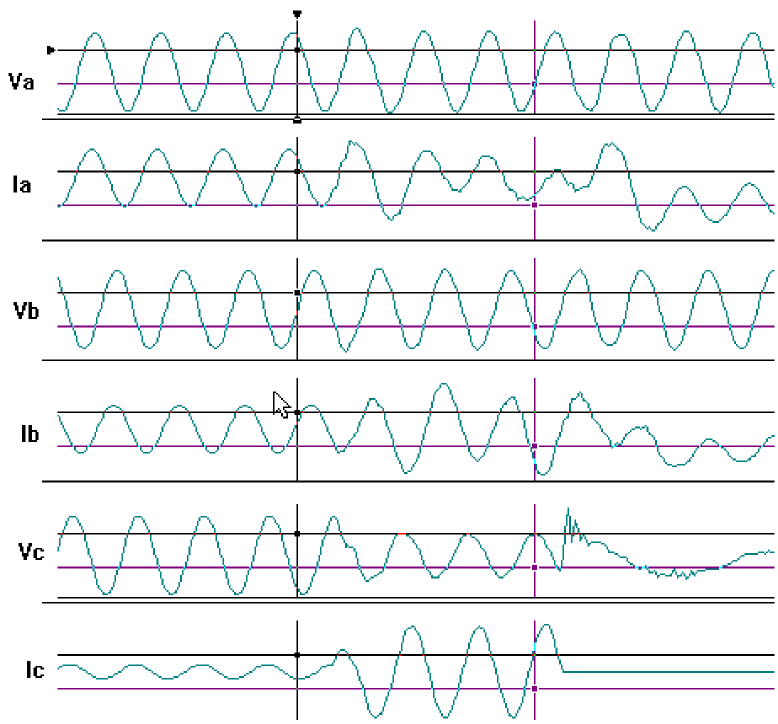

Figure 3 - Low frequency transients during fault on series compensated line

Distance relays applied on lines with or near series capacitors are either designed, or set, or both, to account for low frequency distortion of fault currents [6].

Low frequency power swings (impact on distance relays)

Power swings result in a change in apparent impedance presented to a distance relay. This changed impedance can result in relay operation, which may or may not be desirable. Out of step tripping and blocking protection is routinely applied to ensure proper performance of protection systems during power swings [7].

Frequency excursions causing improper performance of memory polarizing signals

Frequency excursions can cause unexpected operations of distance relays with memory polarizing circuits. This is because many distance relays use phase comparison principles to compare the phase relationship of an operating quantity with a polarizing quantity. During a change in frequency, an operating quantity with the present frequency will not bear the expected phase relationship to a polarizing quantity with a different memorized frequency. Modern relays employ a variety of techniques to ensure that relays do not misoperate due to frequency changes and the impact on polarizing signals. This issue may also be classified as “insidious” since it is not widely reported in the literature. However, since it seems to be well known by manufacturers, the authors decided to classify it as “infamous”.

BC Hydro experienced this problem on the power system shown in Figure 4. The tie to the integrated system was opened due to a fault, and the system shown became islanded with generation of about 72 MW compared to a total load of about 35 MW. The excess power caused the system frequency to increase rapidly, and Device 21 operated on load to trip the 8MW generator.

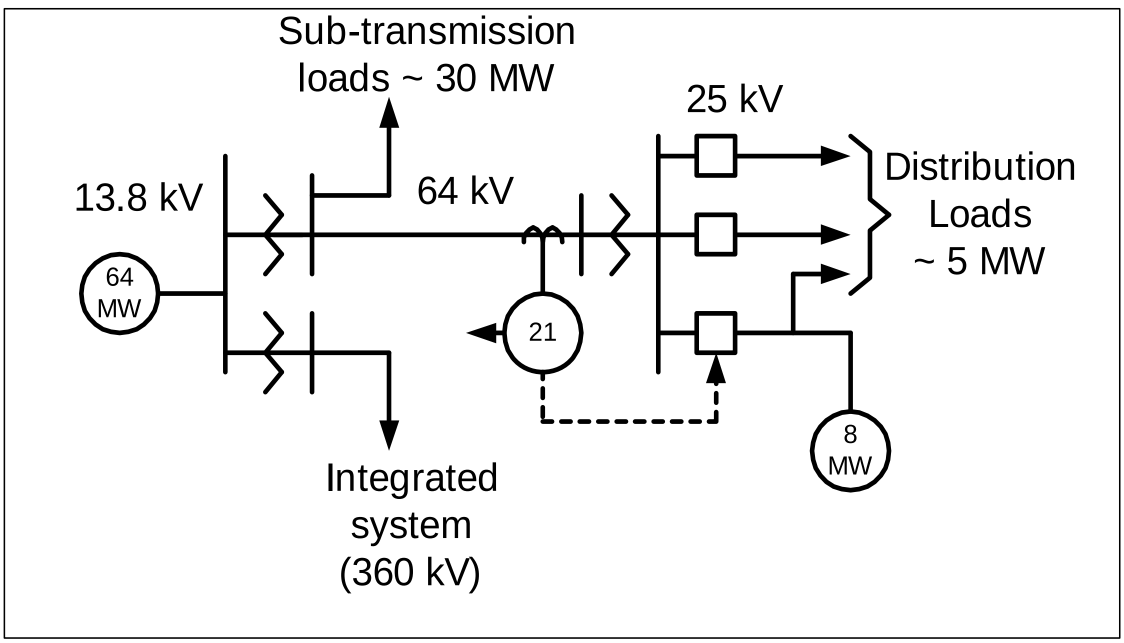

Figure 4 - Power system that experienced frequency rise

Device 21 was an early design of microprocessor distance relay that used memory polarizing continuously. In this instance, the memory voltage became out of phase with the actual voltage due to the rapid frequency rise and caused an unexpected operation of the relay.

Transformer and shunt reactor inrush currents

Power equipment with ferromagnetic cores may exhibit significant currents during energization as shown in Figure 5. Reference 8 discusses the phenomenon fully. These inrush currents can cause undesirable operation of transformer differential relays for example. Transformer differential protection systems are purpose designed to handle inrush currents without unexpected operation.

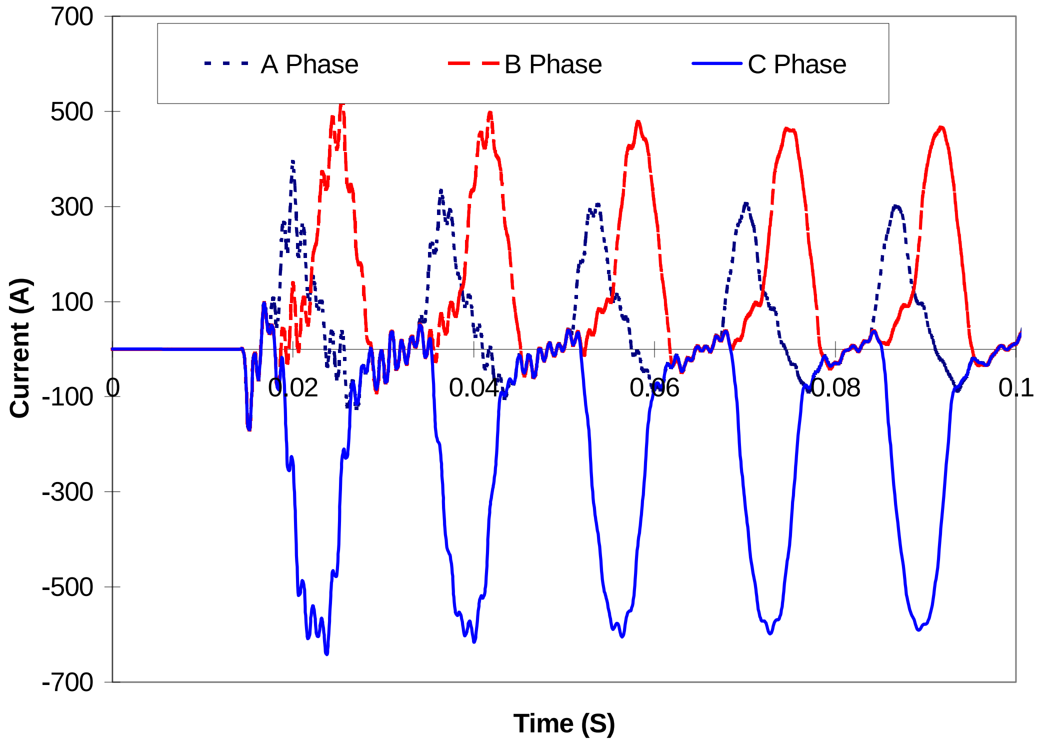

Figure 5 - Example Transformer Inrush Current

Shunt capacitor inrush and outrush currents

At the instant of energization of a shunt capacitor bank, high frequency high magnitude currents can flow as shown in Figure 6. These currents can cause overcurrent relays to operate undesirably and can also induce high energy transients on secondary control cables [9].

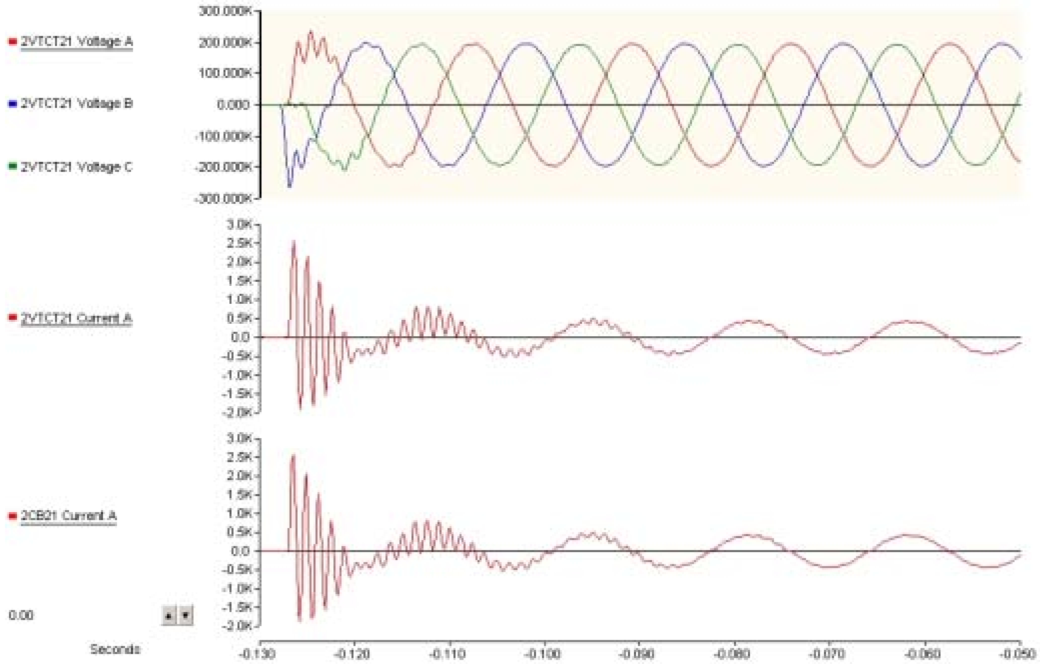

Figure 6 - Inrush current and distorted voltage during shunt capacitor energization.

The same problem with high frequency high magnitude transients can occur when capacitors discharge into nearby short circuits. This phenomenon is called capacitor outrush.

Capacitor high frequency transients are mitigated by proper filtering in protective relays and by proper surge suppression on control cables and relay inputs.

<u>Ferroresonance</u>

Ferroresonance is most commonly associated with lightly loaded, ungrounded and fuse protected distribution transformers terminating on long cables [10]. But it has also been observed in other parts of the power system. Extreme harmonic distortion in this condition can confuse protective relays, causing their mis-operation. Figure 7 shows waveform records that caused a zero sequence ground over-voltage relay to operate unexpectedly, albeit desirably, under a ferroresonant condition. This condition was instigated when a generator unit transformer was switched under no load to disconnect it from the 500 kV system. The relay was connected via three-phase wye-wye grounded voltage transformers on the 13.8 kV delta winding, which also had a long generator isolated phase bus and surge suppression capacitors connected but the generator was off-line. High harmonic distortion in the voltage signals caused the zero sequence over-voltage relay to assert, which in-turn initiated time-delayed tripping of the unit transformer. Although the relay was intended to operate for ground faults, its operation in this case mitigated possible damage to the voltage transformers or the unit transformer from sustained ferroresonant over-voltage. The most commonly used practice to avoid ferroresonance on a high impedance grounded system is to provide an additional voltage transformer winding connected in open corner delta configuration with adequate damping resistor.

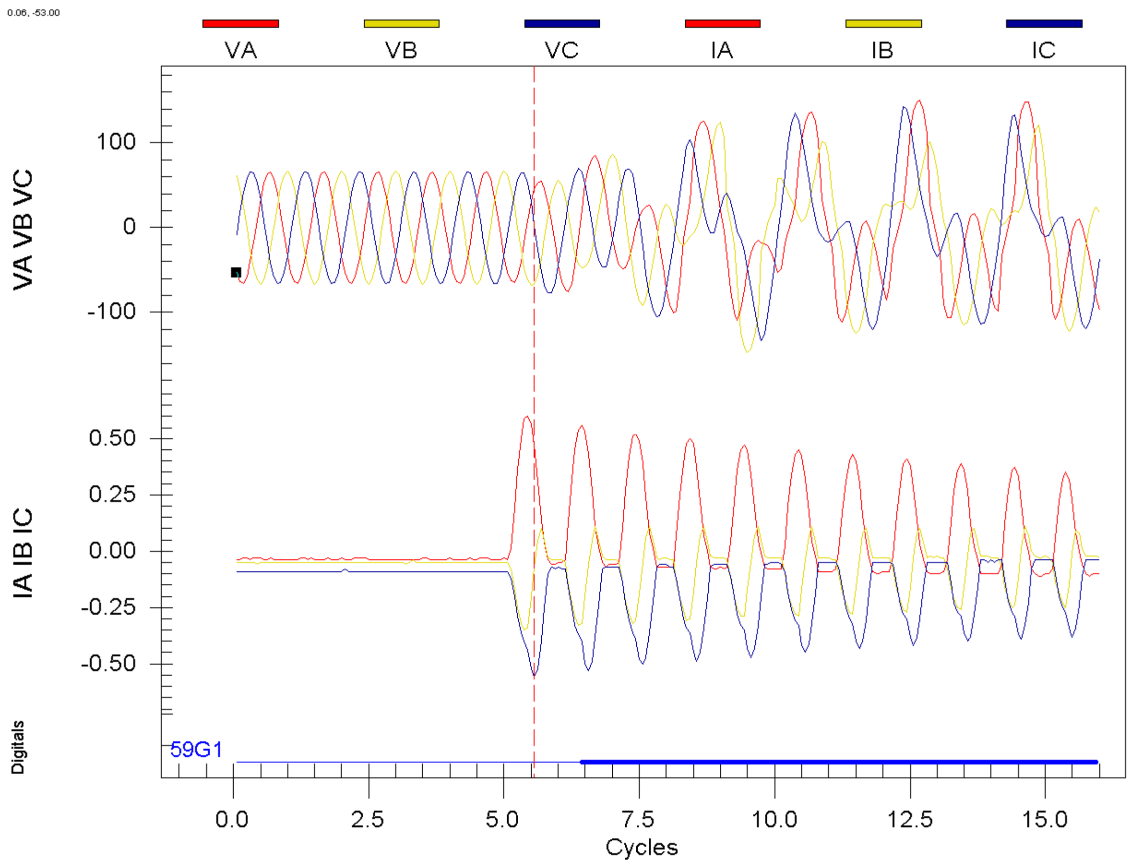

Figure 7 - Sustained zero sequence over-voltage under a ferroresonant condition.

Fundamental frequency unbalances resulting from single phase tripping and reclosing

During single phase tripping, there is significant unbalance in the region of a transmission line carrying load on only two phases. This is fundamental frequency unbalance that results in negative and zero sequence current flow and associated unbalance voltages. Relays that measure negative or zero sequence currents may have to be desensitized, disabled or have appropriate time delays added to override the open phase period [11].

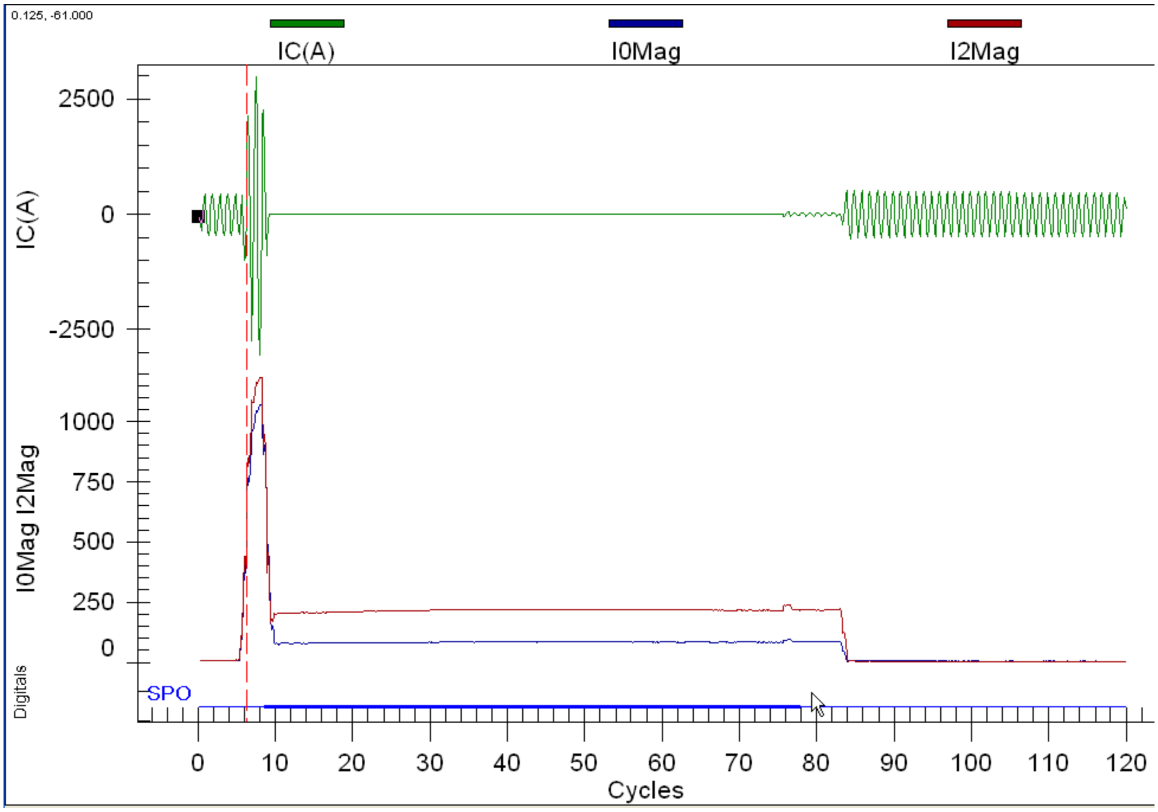

Figure 8 - Unbalance current flow during single phase open.

Figure 8 shows the unbalanced negative and zero sequence currents that flow in a transmission line while a single phase is open (after the large current flows during the fault itself). These unbalance currents cause unbalance voltages and currents in other parts of the system outside the affected transmission line.

Insidious

The following transients are called insidious because they (or their impact on protection) are not as widely recognized as the infamous ones. Insidious transients are described in more detail than the infamous transients because they are either not reported at all, or are reported less widely than the infamous ones.

Transmission line ringdown voltages and currents (impact on shunt reactor protection, and impact on distance relay polarizing voltages)

De-energization of a shunt reactor compensated transmission line will result in the shunt reactor inductance oscillating against the line shunt capacitance. Due to the three phases oscillating at slightly different frequencies and inter-phase energy transfer via phase to phase capacitance and neutral reactors, the currents in each phase are not constant, but follow a low frequency envelope. Figure 9 shows the ringdown voltages and currents from a shunt reactor connected to a 230 kV circuit which was a mix of overhead line and undersea cable. The ratio of highest peak phase current to the prefault peak current is approximately 2.8.

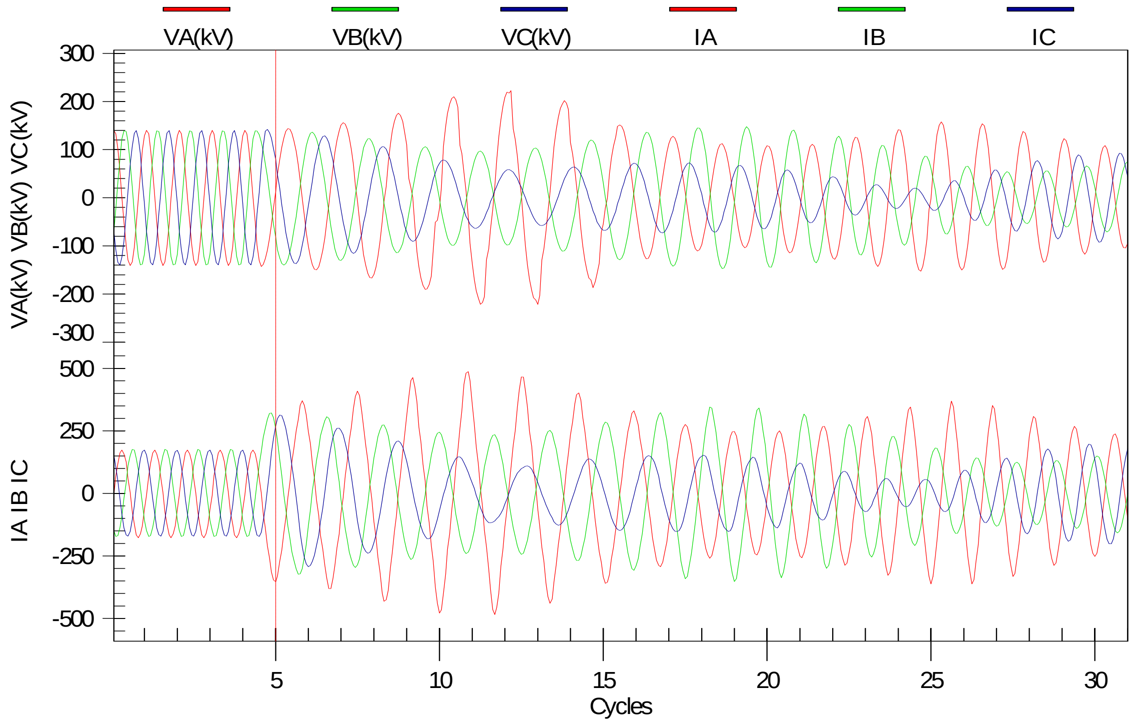

Figure 9 - Ringdown voltage and current in shunt reactor after line deenergization.

The maximum phase current in the shunt reactor can be calculated as $I_{RMS} = V_{L-L} \cdot \sqrt{\frac{C}{L}}$, which exceeds normal rated reactor current for undercompensated lines. This increased reactor current must be taken into account when calculating phase overcurrent settings for the reactor protection. In addition, if the ringdown frequency of the line is outside of the frequency tracking range of the relay, errors caused by improper filtering can result in transient misoperation of overcurrent elements even if the actual current is below the element pickup. In cases where this is a consideration, a minor time delay on overcurrent element pickup can help prevent transient misoperation, as the error in the calculated current magnitude tends to oscillate about zero.

These low frequency voltage oscillations can also cause problems for memory polarized mho elements, as the memory voltage can become corrupted during the interval while the line is ringing, with subsequent “surprises” from the mho elements when the line is reclosed at the first end and line charging current starts to flow again. Each relay manufacturer will deal with this problem internal to the relay in their own way. If the manufacturer has not been successful in avoiding undesirable behaviour, one recourse to the protection engineer is to temporarily block or delay tripping of the mho elements during line re-energization.

It should be noted that if a manufacturer chooses to disable memory polarizing whenever the line terminal is open, it may be necessary to use switch on to fault protection even when using bus side VTs. A current based or offset distance based switch on to fault protection may always be required to protect against switching on to a close-in three phase fault. This is contrary to normal expectations that when bus side VTs are used, memory polarizing will be available for switch on to fault protection of directional distance elements.

<u>Fundamental frequency unbalance currents and voltages caused by controlled closing or opening or staggered closing of circuit breakers.</u>

As noted previously in this paper, the unbalances resulting from open phase conditions due to single phase tripping are well recognized. However an increasing number of applications of circuit breakers include controlled closing, or point on wave closing to minimize switching transients. Some applications of controlled opening are also applied (particularly in switching of shunt reactors). Controlled closing means that breaker pole discrepancies may last significantly longer than the 4 ms or so that is typically expected for a three pole switched breaker. In some cases, the pole discrepancy may last for several power frequency cycles.

Some means of mitigating the impact of fundamental frequency unbalances due to controlled opening or closing include:

1. Extending the time delay of sensitive unbalance overcurrent functions that might undesirably respond to the short time unbalance.
2. Disabling the controlled switching when it is not needed. For instance, when controlled closing is applied on a transmission line terminal, only the lead terminal needs to have controlled closing. When the lead terminal closes with pole discrepancy, only low magnitude line charging currents will flow; so unbalance current will be small. When the follow terminal closes, if controlled closing is used (even though not necessary) unbalance currents will be much larger, due to load flow when the follow terminal is closed.

In some cases, controlled switching may not perform as desired. Protective relay event records can help identify such cases. Figure 10 shows the currents and voltages during de-energization of a shunt reactor. In the case of Figure 10, the controlled opening did not operate as expected on all three phases, and the unsuccesful attempt to interrupt A phase current can be seen with the associated restrike showing as a dip and recovery in A phase voltage. The extended neutral current due to slow interruption of A phase load current can be seen. Figure 11 shows the currents and voltages during properly controlled switching.

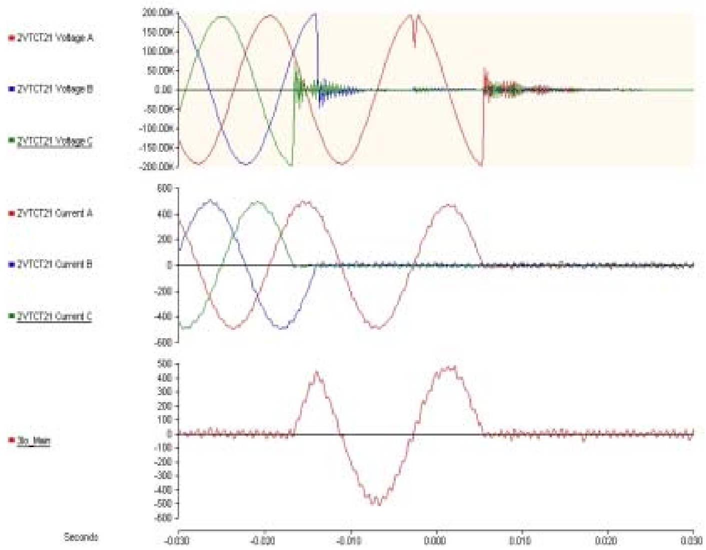

Figure 10 - - Failure of controlled opening of shunt reactor breaker.

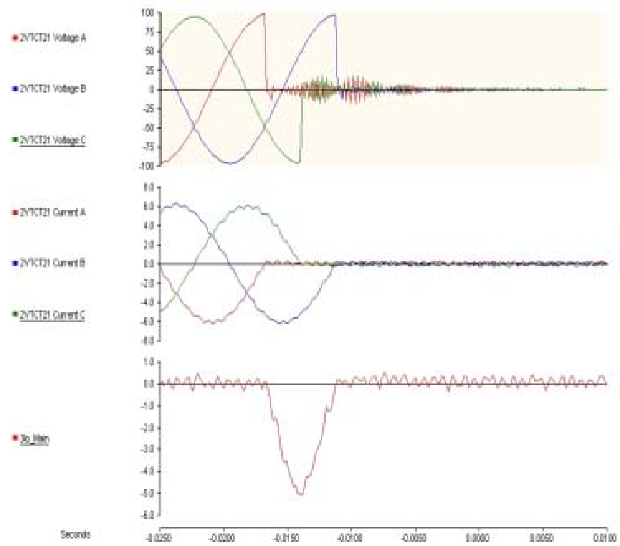

Figure 11 - Controlled opening of shunt reactor breaker

Gapped surge arrestor conduction due to lightning

Early types of surge arresters included gaps that flashed over to prevent transient overvoltages. Current flows through the flashed gap until the first natural current zero is reached. This flow of so called “follow current” could cause very fast protection to detect a fault and trip undesirably. BC Hydro has experienced some undesirable trips of high speed bus differential protection due to gapped surge arresters in the differential zone.

Figure 12 shows a single line diagram of a BC Hydro station with gapped surge arresters on the high voltage bushing of a transformer. These arresters were inside the differential protection zone of two high impedance bus differential relays 87B and 87BS. The relays were of different manufacture. Digital fault recorders (DFR) are connected to measure the currents in each of the transmission line terminals 5L92 and 5L94.

Figure 13 shows a DFR recording of an undesirable trip of the bus protection during a lightning storm. The top three traces are VA, VB and VC of the voltages at the 5L94 line capacitor voltage transformer. The distortion of B Phase voltage at about 4.5 cycles into the recording can be seen. It is apparent that the lightning strike was at the instant VB was near a peak value. The flow of neutral current as soon as the surge arrester started to conduct can be seen in the fourth analogue trace from the top. The conduction stops at the first natural current zero. The operation of the high speed bus differential relay due to the apparent internal fault can be seen.

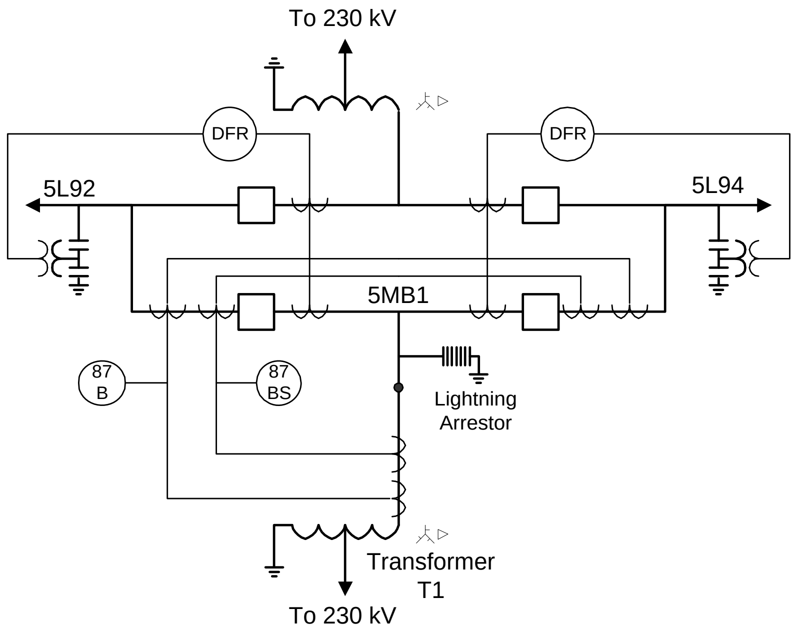

Figure 12 - Single line diagram of station with gapped surge arresters

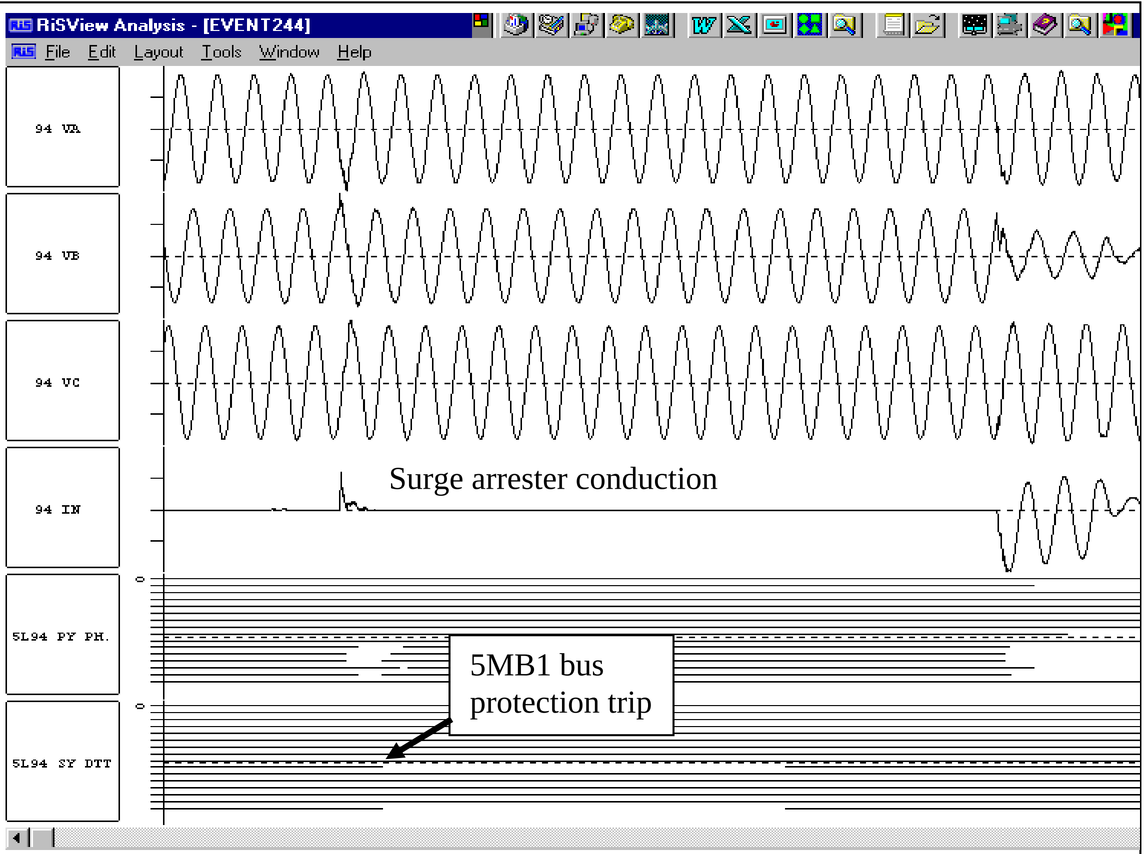

Figure 13 - DFR Record of undesirable bus protection operation

Note that in this instance and in several other instances, the second bus differential relay, made by a different manufacturer, did not operate even though it was set similarly to the one that did operate. The relay that did not operate was not quite as fast as the one that did. The solution applied in this case was to replace the relay that operated undesirably with the same type that was stable during the arrester conduction.

Figure 13 also shows some other digital events on 5L94 primary protection (PY PN.) at the same time as the surge arrester conduction. These events include operation of the sensitive forward looking directional ground overcurrent element in circuit 5L94, and received permissive trip. These events record a near misoperation of the line protection as the forward looking fault detector reset one or two milliseconds before the permissive trip signal was received from the remote terminal. No action was taken with respect to the near miss. The 5L94 line protection was working satisfactorily as can be seen from a correct single phase trip about 4 cycles before the end of the trace, when a second lightning strike caused a real short circuit on B phase and a desirable B Phase trip of circuit 5L94.

Low frequency due to series capacitors may affect negative sequence elements

Figure 14 shows a fault record where a healthy series compensated line undesirably tripped, due to sub-synchronous resonance-induced transients after the successful tripping of the adjacent line on a phase to phase fault. This undesirable trip was caused by incorrect operation of a sensitive ground fault permissive overreaching transfer trip (POTT) scheme using negative sequence directional and overcurrent fault detectors. Initially, the reverse blocking function (Z3RB) was asserted for the fault on the adjacent line. After the fault on the adjacent line cleared, forward-looking negative-sequence fault detectors picked up at both terminals of the unfaulted line. Pickup of the remote forward fault detector is illustrated by the permissive trip received on IN4 and locally by 67Q2 and 67Q2T. The forward fault detectors remained asserted until shortly after the current reversal guard logic, Z3RB timer, dropped out, 5.5 cycles after the fault was cleared on the adjacent line. At that point, the forward pilot tripping element, coupled with permissive from the remote terminal, allowed a POTT trip.

Analysis of the recordings indicates that a significant resonant current flow with a frequency of around 38 Hz was excited between the B and C phase elements of the power system by the initial fault. When the faulted line opened, all of this resonant current flowed through the healthy line. The relay digital filters attenuate but do not fully reject these sub-synchronous harmonic (or low) frequency components. Since these low frequency components were only in two phases, they consisted of positive- and negative-sequence components similar to an internal phase-to-phase fault. In this case there was enough spectral leakage from sub-harmonic frequency to 60 Hz during signal filtering that the erroneous negative sequence components became large enough to assert the fault detectors. Since the source of sub-synchronous transients was the series capacitor internal to the line and the transients were similar to an internal fault, the directional detectors also got confused and declared a forward direction at both line terminals, leading to the false-trip.

On one hand, the negative-sequence fault detector is well-suited for sensitive ground fault protection of parallel lines due to its immunity to zero-sequence mutual coupling. On the other hand, this incident demonstrates its vulnerability to sub-synchronous resonance transients. Both situations were mitigated by using zero sequence overcurrent fault detection and negative sequence directional element.

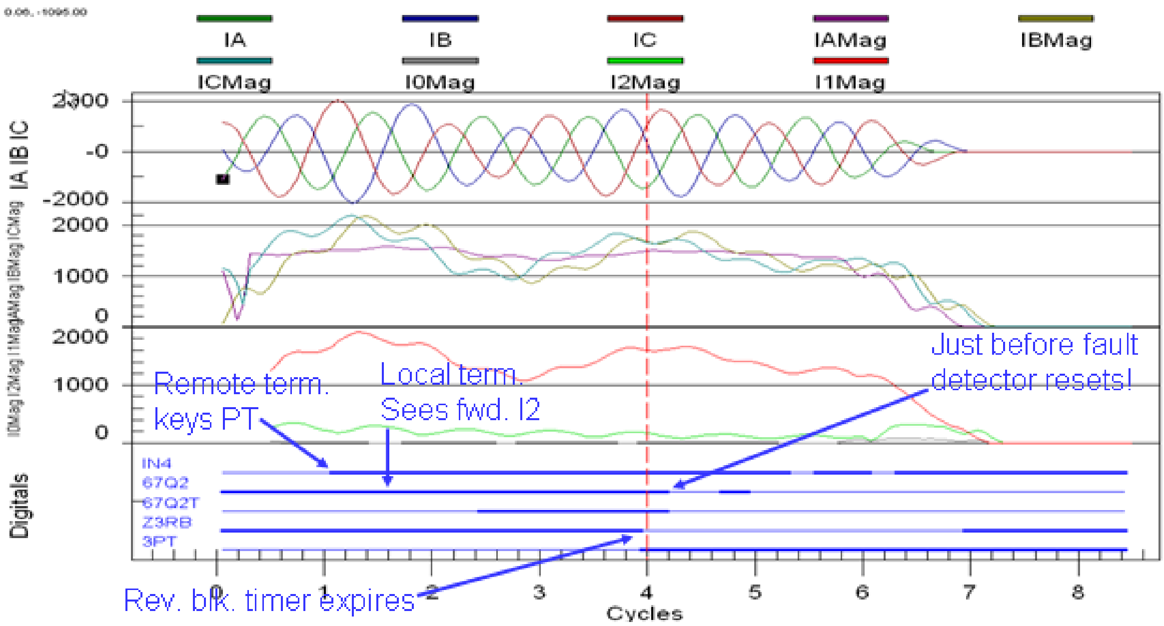

Figure 14 - Line protection mis-operation during sub-synchronous resonance

Extended unbalance from single phase tripping and reclosing

As noted previously in discussion of "infamous" items, unbalances due to single phase tripping are well recognized. However, not so well recognized is the impact of single phase tripping on breaker pole discrepancy timers. In the case of three phase tripping normal discrepancies are less than one cycle in duration, and pole discrepancy timers need only be set marginally longer. However, in the case of single phase tripping, pole discrepancy timers will also be extended to cope with open phase conditions. This means that unbalance overcurrent relays may have to have time delays extended sufficiently to override long pole discrepancy timer settings.

In one case in BC Hydro, a shunt reactor connected to the tertiary winding of a 500 kV auto transformer used negative sequence time overcurrent protection to detect interturn faults. The transformer was adjacent to a line terminal with single phase tripping and reclosing, as shown in Figure 15.

This protection had been secure for many years even though the transformer was connected to a station where the major supply line had single phase tripping and reclosing applied.

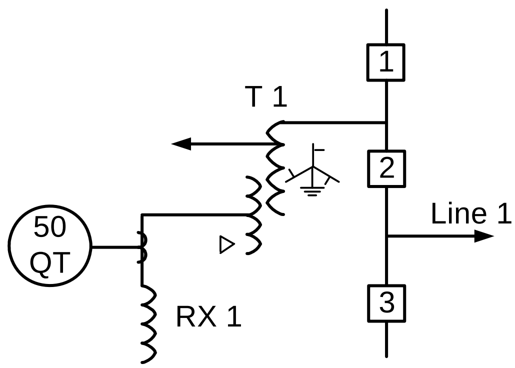

Figure 15 - SPTR Line and adjacent transformer/reactor

On one occasion however, when breaker 1 was out of service for maintenance, a fault occurred on Line 1 and a single phase was tripped. Breaker 3 reclosed successfully, but breaker 2 failed to reclose the open pole when commanded to do so. Breaker 2 was normally the second breaker to close in the sequence, (after about 2 seconds). Eventually Breaker 2 pole discrepancy timer opened all three poles correctly and the transformer reactor was disconnected on all three phases. Breaker 2 pole discrepancy timer was set to override a normal open pole period of 2 seconds and was therefore set at 2.5 seconds. Device 50QT was a negative sequence definite time overcurrent function that was set to override only the normal open phase period of 1 second. It was not set to override the pole discrepancy period of Breaker 2. During the disturbance transformer T1 and reactor RX1 were connected to the 500 kV supply system on only two phases until Breaker 2 pole discrepancy timer expired. The result was that 50QT timed out first, and there was an undesirable lockout trip of the reactor and T1. The mitigation action was to increase the time delay on 50QT.

Secondary transients

Infamous

<u>Incorrect differential currents due to unequal CT saturation</u>

CT saturation is a well recognized problem in power system protection [12]. The problem arises when at least one of the magnetic core current transformers in a differential connection is connected to a burden that is too high or when the transient offset component of fault current is too high or too long. Reference [13] provides a tool for calculating the performance of a current transformer under specified conditions. Figure 16 shows an example of false differential current caused by more saturation in one CT than the other. Note that in Figure 16 the saturation of one CT is caused by the level of transient offset in the fault current. Thus it does not start to saturate until some time after the fault begins. The problem is mitigated by a variety of means, including special designs of relays to tolerate saturation and sizing of CTs for specific applications.

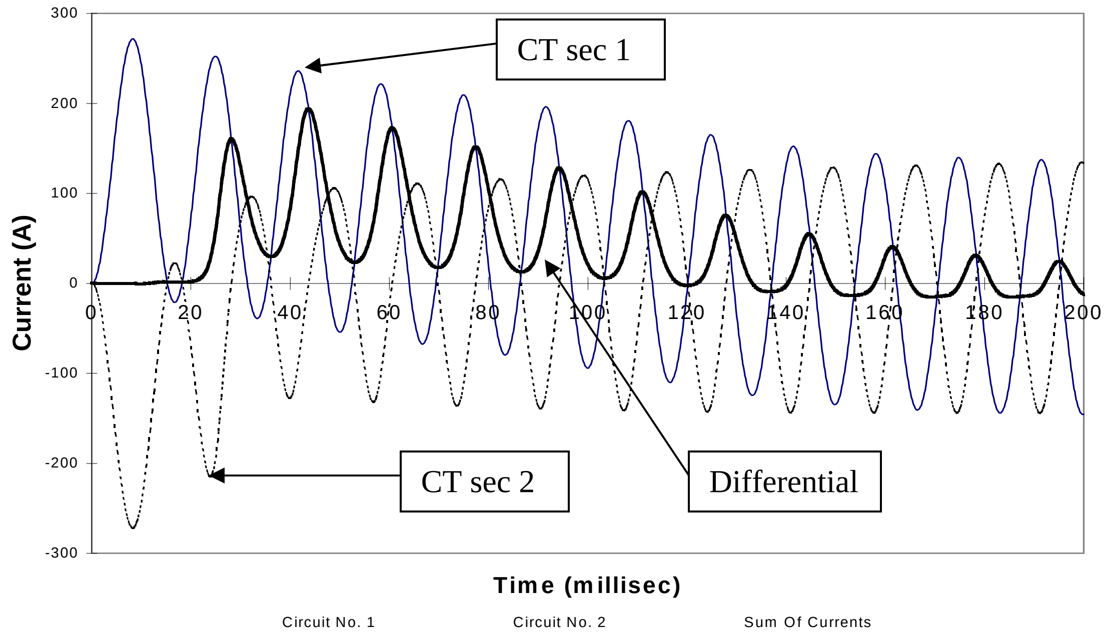

Figure 16 - False differential current due to CT saturation

<u>Improper declaration of breaker failure due to DC tail resulting from CT saturation</u>

When a CT saturates, the secondary current becomes shifted in phase from the primary current. Thus when the primary current is interrupted at a primary current zero, the secondary current is not simultaneously at a natural zero. Thus in order to reach a zero value the secondary current tapers off in a so called "dc tail" as shown in Figure 17 and Figure 18. The "dc tail" is larger when the current transformer is built with anti remanence gaps to control the remanent flux. This "dc tail" can cause undesired slow reset of certain types of breaker failure relay current detectors and consequent undesired breaker failure protection operation.

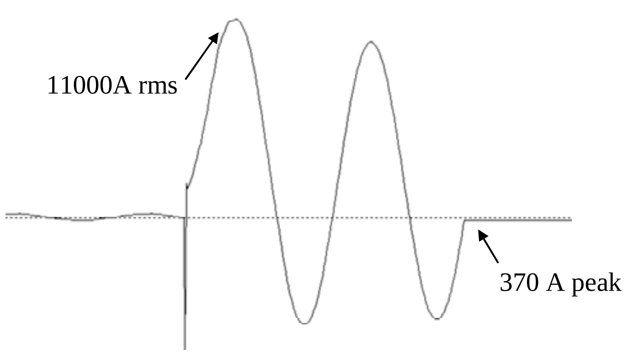

Figure 17 - CT Saturation and dc tail

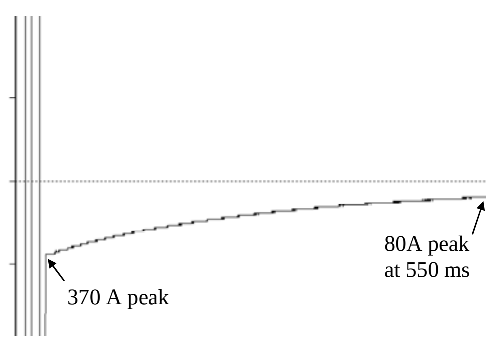

Figure 18 - DC tail zoomed

BC Hydro routinely applies gapped core CTs in EHV applications and has only once had a problem with undesired operation of a breaker failure relay due to the "dc tail". The problem is mitigated by special design of current detectors in breaker failure relays to be immune to the “dc tail”.

<u>Capacitor voltage transformer (CVT) transient inaccuracies.</u>

CVTs usually include tuning circuits to respond accurately to fundamental frequency signals. These tuning circuits may cause a CVT to respond inaccurately to sudden voltage changes if, for instance, a fault at a voltage peak caused the primary voltage to drop suddenly from peak value to zero. It is likely that many CVTs will not properly reproduce the sudden change in voltage. These transient errors in CVTs can cause distance relays to lose some accuracy if the relays are not designed to handle these transient distortions [14]. Indeed, most relay manufacturers take special care to ensure their products will not undesirably operate in the presence of CVT transient inaccuracies.

<u>High frequency secondary voltages</u>

High frequency currents and voltages in the primary system can couple to secondary wiring in control cables in a substation switchyard. Similarly, interruption of direct current through inductive circuits can result in very high frequency and high magnitude voltages on secondary wiring [15, 16].

These transients appear as high magnitude high frequency voltages on the secondary wiring that can damage relays and other connected equipment as well as causing unexpected operation.

Problems due to these transients are mitigated by correct shielding of control cables as well as correct design of connected equipment to meet standard levels of transient voltages. In North America, the applicable standard is Reference 17.

<u>Spurious signals caused by multiple grounds on VT/CT secondaries resulting in improper relay performance.</u>

Multiple grounds on the neutrals of current and voltage transformer secondaries are not normally applied. One reason is that during a short circuit to ground, the ground potential within a substation may vary. If the instrument transformer neutrals are connected to ground at different potentials, these differences in potential will be measured by the connected instruments. This phenomenon is fully described in Reference 18. Several papers in the past at the WPRC have described problems arising from multiple grounds on instrument transformers.

Insidious

<u>CT saturation due to long time constants during reactor energization (spurious unbalance currents)</u>

A high X/R ratio (in the range of 500-1000) is required for shunt reactors to minimize their losses. This high X/R ratio results in offset currents with long time constants, in the order of seconds, after reactor energization. Figure 19 shows a time constant of about 2 seconds for the offset current upon energization of a 230 kV shunt reactor.

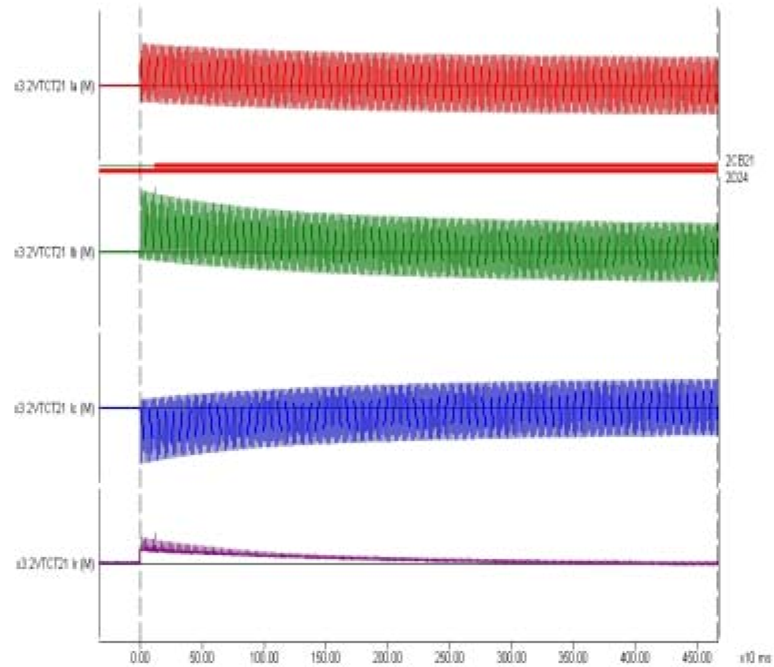

Figure 19 - Shunt reactor energization currents

This very long offset current will saturate current transformers even at low current levels such as normal load. The degree of offset is different between the three phases; so the CT performance will also normally be different between phases and there will be different degrees of saturation (and thus error) in the three CTs. This phenomenon and its mitigation techniques are completely described in Reference 19. However, it is mentioned here for completeness and as a refresher. Figure 20 [From 19] shows how the CT in one phase may saturate more than CTs in the other two phases because of different degrees of offset in the primary currents.

These different degrees of saturation will result in incorrect presence of unbalance currents such as negative sequence or residual during energization. Unbalance overcurrent protection may undesirably operate due to fictitious unbalance current. A mitigation technique that may be used is temporary disabling of sensitive unbalance overcurrent protection during shunt reactor energization (so called inrush tripping suppression). Another technique is to use a neutral CT instead of a residual current of phase CTs to measure zero sequence unbalance current.

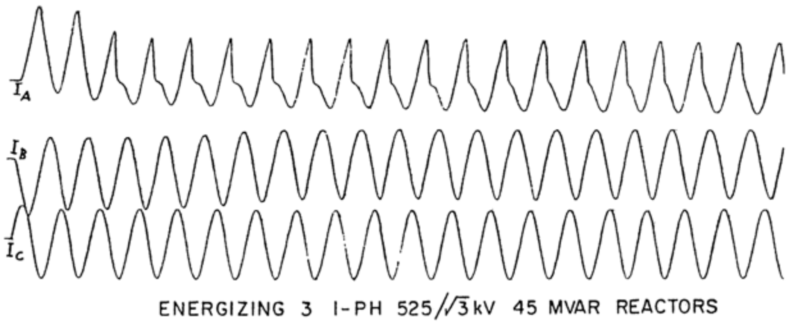

Figure 20 - Unequal CT saturation during reactor energization

If the burden or accuracy class of the CTs at each end of a winding are different, there could also be undesired operation of differential protection due to unequal saturation of CTs at each end of the reactor. Mitigation methods for this problem include setting differentially connected overcurrent relays higher than load current, or using saturation tolerant differential protection such as high impedance bus differential protection.

Figure 21 [Also from 19] shows the different performance between CTs in a power transformer tertiary and CTs at the neutral end (i.e. CB3) of a shunt reactor. It can be seen that the C phase tertiary CT does not saturate significantly in the presence of the transiently offset load current, but the C phase CT on CB3 does, and a high differential current results.

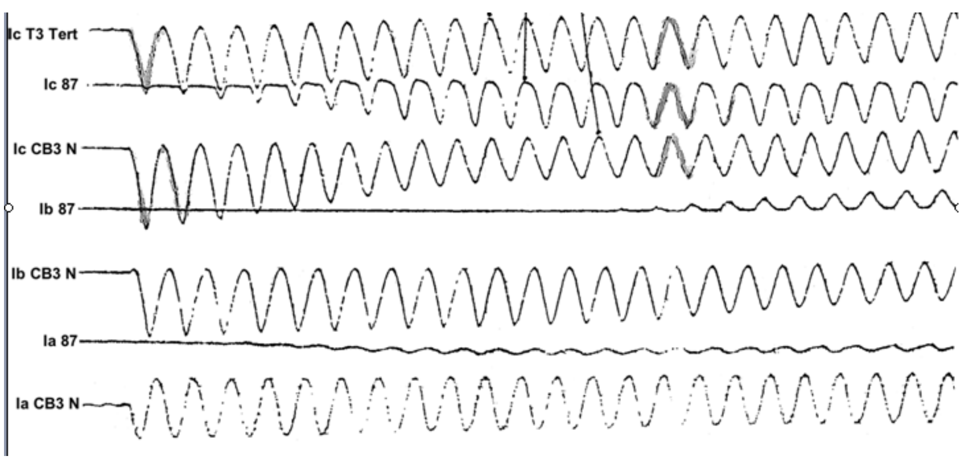

Figure 21 - False differential current from unequal CT saturation in the same phase

<u>DC grounds cross triggering sensitive dc inputs</u>

Although this problem may be classified as “infamous” because it has been well reported (for example in [15]), the increasing application of electronic devices with inputs that can be asserted with low energy levels, has resulted in increased observation of this problem. For this reason the authors have decided to classify this problem as “insidious”. BC

Hydro experienced several protection mis-operations from erroneous pick-up of digital inputs of new microprocessor-based relays. These mis-operations were attributed to capacitive discharge and DC voltage transients imposed on high impedance digital inputs.

BC Hydro investigations showed that only a small amount of energy is required to assert sensitive inputs. There are multiple actions that resulted in an inadvertent operation, one of which is a low-impedance ground on the substation (+) DC voltage bus.

Figure 22 is an example of a substation control circuit. The positive and negative rails of the 130 VDC battery bank are grounded through identical impedances, and are considered perfectly balanced. The input of the protective relay is shown with 75V bi-directional Zener diodes, and an internal resistance. Capacitor C3 represents distributed capacitance from the wire bundle to ground and surge suppression capacitance if any. The device connected to the relay input is shown with a high leakage resistance. Under normal conditions, the (-) DC bus is at -65 VDC with respect to ground. Adding voltages around the loop from the (-) DC bus and through the relay input and C3 to ground, C3 is determined to be charged to +10V (-65 + 75 – 10 = 0) with respect to ground.

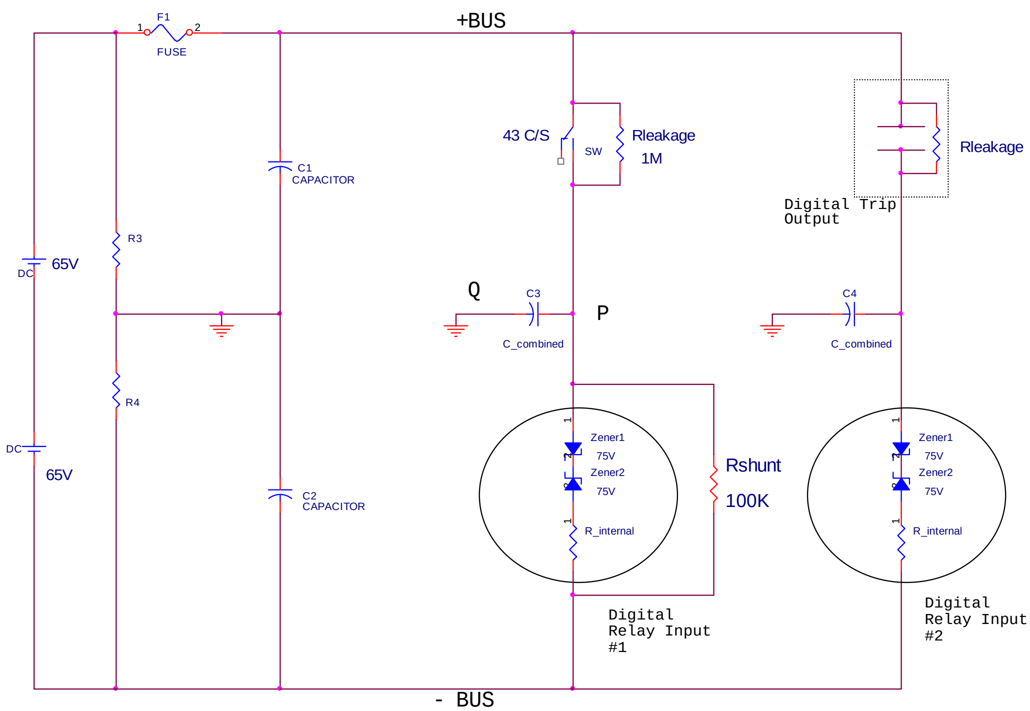

Figure 22 - Typical substation Control Circuit

If the (+) DC bus came into solid contact with ground, the (-) DC bus will drop to -130 VDC. Since C3 is unable to instantly change voltage, 140 VDC will appear across the relay input. C3 will ultimately charge to -55 VDC with respect to ground, with a time constant determined by the value of C3 and the internal resistance of the relay input. The time constant will determine whether the voltage across the relay input will remain above its pickup level long enough for the relay to sense it.

Two mitigation strategies to prevent inadvertent relay operation may be considered. First, if the value of C3 can be kept as low as possible, then the time constant may be such that the voltage will not remain above the relay input pickup level for long enough to be detected. Second, a shunt resistor may be placed across the relay input in order to set up a voltage divider with the leakage resistance of the device connected to the input. With an appropriately sized resistor in the voltage divider, the highest voltage seen across the relay input due to the (+) DC bus ground can be kept below the relay input pickup level. In general, BC Hydro finds that a delay of about 1.5 cycles is sufficient to ensure security in typical applications.

Momentary dc interruptions simulating change of status to inputs

Modern numerical relays are designed to tolerate and even ride through sudden temporary voltage depressions on the dc power supply without undesired effects. However, where the security of a protection system requires assertion of an input signal, the possibility of undesired tripping arises if there is a disturbance on the dc power supply.

Consider for instance the stub line protection function that is sometimes applied as part of a transmission line protection system. This type of protection is sometimes used if the terminal of a transmission line could become separated from the line itself by an open disconnect switch, and if the voltage source for the protection is on the line side of the disconnect switch. The applicable single line diagram and logic diagram are both shown in Figure 23.

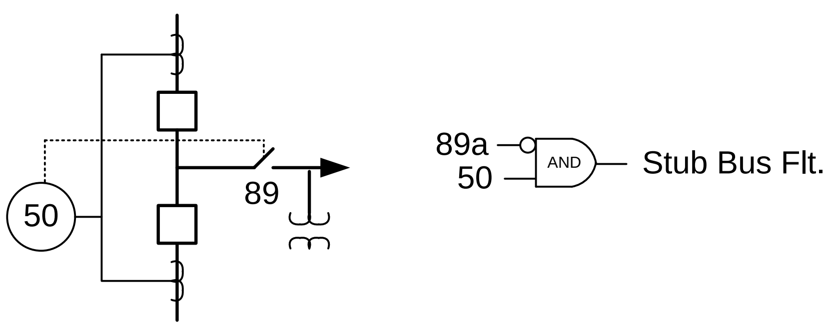

Figure 23 - Stub bus protection system

It can be seen from Figure 23 that if the line disconnect switch is open (i.e., auxiliary contact 89a is not asserted) the overcurrent function becomes a simple differentially connected overcurrent system.

If the dc power supply to Device 50 is considered, as shown in Figure 24, it can be seen that the power supply may be shared by other protection and control circuits. If there is a short circuit on another circuit as shown, the supply voltage to Device 50 will be momentarily reduced until such time as the fuse(s) F3 and/or F4 clear the external short circuit. While the voltage to Device 50 is reduced, input 89a is momentarily de-asserted even as the ride through capability of Device 50 allows it to stay in operation. If the line current is sufficient to pick up device 50, an undesired trip will occur.

Note that it is not possible to supervise the operation of Device 50 with an undervoltage function, since the voltage source is on the line side of the disconnect switch. If the disconnect switch is open, and the line is energized from the remote terminal, then undervoltage supervision of the 50 function would prevent operation of the stub bus function.

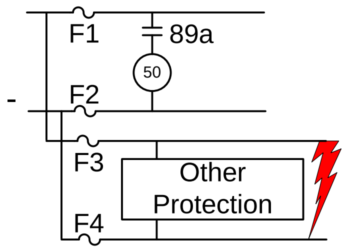

Figure 24 - Short circuit on dc power supply.

Mitigation of this problem is to be aware of the possibility of unexpected de-assertion of inputs due to momentary loss of dc power during short circuits on other parts of the dc system. For this specific example, the current detector could be set higher than load current, or the sense of the line disconnect auxiliary switch input could be reversed so that loss of the input blocks the stub bus protection function.

Conclusion

Power system transients have been classified into primary and secondary groups. Within each group there are well recognized (infamous) transients and not so well recognized (insidious) categories.

In many cases satisfactory mitigation of the impact of all types of transients is feasible. In some cases finding the optimum mitigation action may require simulation or playback of the transient phenomenon so that relay performance in the presence of the transients may be investigated. However if the transient phenomenon and impact on the protection is sufficiently well understood, previous research work will have identified the optimum mitigation method.

Several less well understood insidious transients have been described, and mitigation techniques presented. However, there is no end to the learning that experience can deliver. The authors hope that their experiences will be of interest and value to other protection engineers.

Acknowledgements

The authors thank David Sydor of BC Hydro for providing information on dc grounds cross triggering sensitive inputs, and Brian Burk for careful review and thoughtful comments on the draft paper.

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