Abstract:

This commentary is an addendum to the paper, "Dynamic Performance Testing of Mho Relay Memory Action" by K. H. Engelhardt, as presented to the Ninth Annual Western Protective Relay Conference.

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by
J. A. Jodice
Doble Engineering Company

Presented by
William O. Kennedy
Saskatchewan Power Corporation

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INTRODUCTION

F3-C/D test signals are derived by analog signal-generating techniques. In 1973/4 the design was developed as a means for generating precise, stable sinusoidal test voltages and currents for calibration and evaluation of protective relays at their (preset) trip points. Later, the basic scheme was expanded to include dynamic test capability. The dynamic function involves control of the pre-fault voltage and current phasors, and the post-fault voltage and current phasors, both of which represent steady-state conditions. The transition between the two sets of phasors is purely arbitrary due to the asynchronous nature of the analog signal generation techniques.

Prior to responding to the comments on functional performance noted in the paper by K. H. Engelhardt, a brief review of the analog signal generation techniques is in order. Modifications to the designs will be discussed in response.

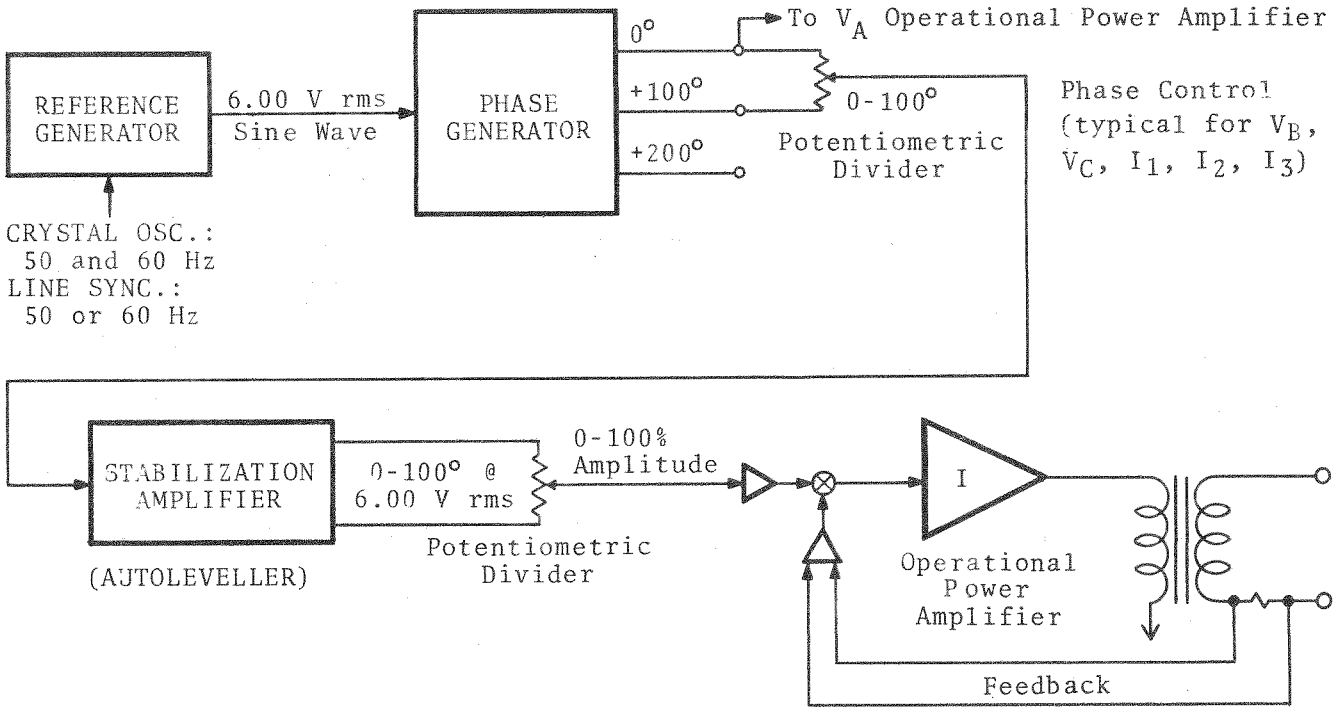


Figure I

Analog Signal Generation:
Current Source Block Diagram

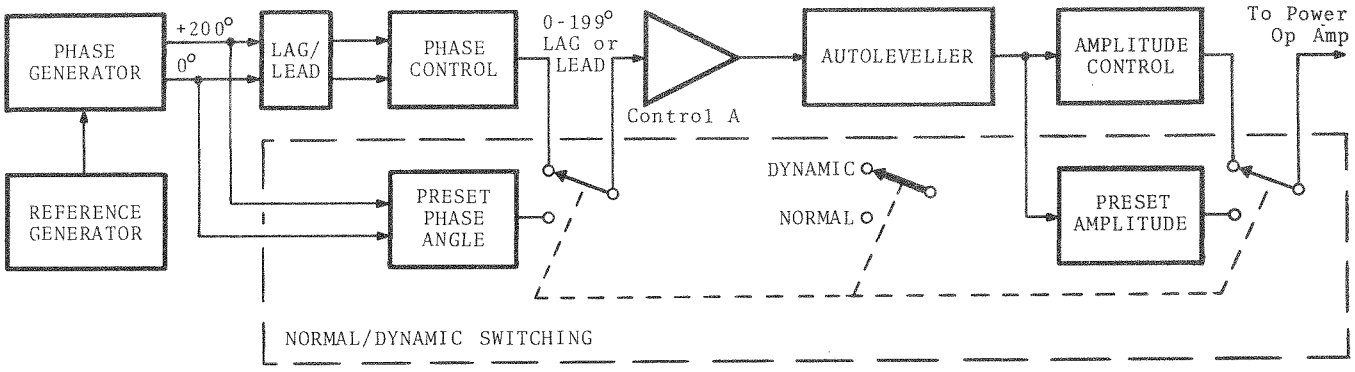


Figure II

Normal/Dynamic Switching

To improve the dynamic test capability of instruments based on these analog techniques certain design changes are possible.

1. Random-Timepoint Transition From Prefault to Fault Current-Page 7

Since the F3 runs asynchronously, the outputs are activated instantly when the "Output On" control is operated. To activate turn-on at zero crossing requires detection of the zero crossing next following operation of the control, and a means to activate the output. Determining zero crossing at this level of precision is not a simple matter. A phase interface pcb, normally used to detect zero crossings for testing automatic synchronizing relays using an F3 and FDF, can provide this measurement function. This circuit can detect zero crossings with a maximum error of ±0.1°. It provides an output pulse at each zero crossing which could be used in a separate circuit to control the "Output On" functions of an F3. Each source would require a phase- interface board and a means to control the "Output On" function. Skew in the control circuitry would result in sources turning on other than at zero crossing. Also, a protocol is required which defines the order (in time) at which the sources would be energized. For example, the sequence might be the next source in the leading, or lagging direction. The complexity of control to achieve this function for multiple sources at precise zero crossing belies the use of any analog signal generation scheme as a reliable means for this application. An alternative technique has been developed and will be discussed later.

2. Reference: Phase Angle Control for A Phase Voltage-Page 8

Phase control of V_A, the reference source is implemented by adding one additional digital phase control, an additional Control A pcb, and an Autoleveller™ pcb. The instrument is physically partitioned such that the pcbs may easily be incorporated.

The phase control is located above the V_A amplitude control, similar to the other sources. The Control A and Autoleveller™ pcbs are located in the card cage. Buss power interconnections and the signal connections to the phase control, the Normal/ Dynamic switching pcb, and the additional boards are made on the pcb backplane.

Documentation describing this modification is available from the Applications Department.

3. Third-Phase PreFault and Fault Currents in Y-Mode-Page 8

An additional current source, the F1 1ø Test System, can be interfaced to the F3D. The F1 output may either be fixed at 0° (V_A reference) or optionally may be phase shifted by the V_C/I_1 phase control. See AN-7, Appendix A. At this time, no provision has been made to provide the N/D switching function. However, a version of the N/D switching assembly capable of controlling 6 sources is available. Should there be sufficient interest, the Applications Department will undertake an investigation of the project.

Analog Signal Generation
Current Source

An oscillator at the power system frequency is followed by a stabilization amplifier to provide a precise signal reference at 50 or 60 Hz - 6.00 V RMS. This reference signal is phase-shifted by operational amplifier circuits using precision passive components to provide signals at fixed phase relationships. Phase control is provided by a potentiometric divider connected between the zero degree output and any other output. In this case, 0° and +100° are shown. As the potentiometer setting is changed from 0% to 50% to 100% of its range, the output phasor will change linearly from 0° to 50° to 100°, respectively. In the F3 instrument phase angle is set by a 3-digit thumbwheel-controlled potentiometric divider that is calibrated directly in degrees of phase angle.

The amplitude of the resulting phasor is not constant; it varies as the law of cosines in proportion to the setting of the potentiometric divider. A stabilization amplifier (Autoleveller™) is connected to the output of the phase shifter to reestablish the 6.00 volt reference level. A second potentiometric divider is connected between the Autoleveller™ output and the input of the constant-gain operational power amplifier. By varying the setting of this divider from 0--100% the magnitude of the test signal is changed to provide whatever voltage or current is required, from 0% to 100% of the source output capability. The amplitude control is calibrated directly in volts or amps.

Normal - Dynamic Switching

The Dynamic function is provided by a second group of preset potentiometric dividers, which control phase angle relationships, current and voltage magnitudes. The normal, or balanced conditions are programmed for 2 voltage sources in open-delta, with 3 wye connected currents - or for three wye connected voltage sources, and 2 currents. Either configuration may be selected by setting the convertible source to V, which provides 3 voltage, 2 current sources, or I, which provides 2 voltage and 3 current sources.

C-MOS switches on the N/D Switching (Printed Circuit Board) select between the balanced quantities and those defining the unbalanced condition as set on the front panel thumbwheel controls.

The N/D status change switch noted on Figure A-1 of Karl Engelhardt's paper is a toggle switch that controls the C-MOS transmission gates in the N/D Switching pcbd.

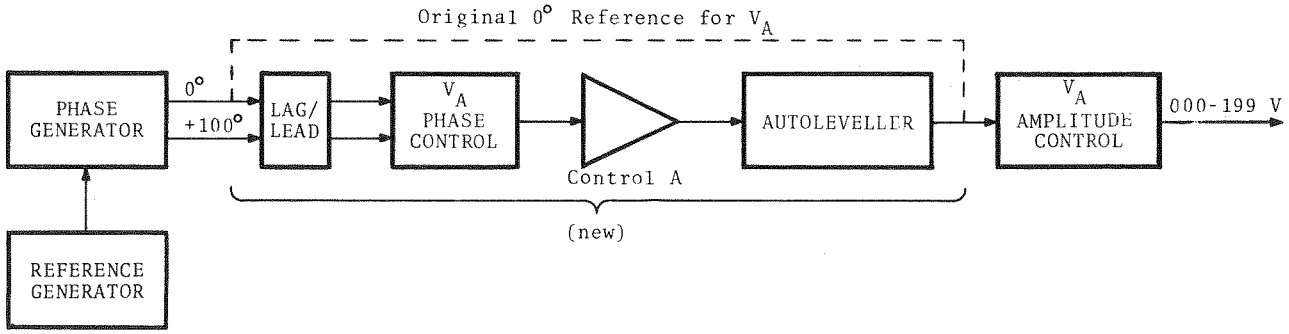


Figure III

V_A Phase Control

New Technology

In 1978/1979 a new digital technique for generating sine waves at power system frequencies was developed. The initial application was in the FDF Dynamic Frequency Source. A frequency source of extreme precision and stability was required for calibration of frequency relays. In addition, a system of timing wherein 3, predefined points on a frequency profile was established. These points remain fixed regardless of the variables of frequency, $\Delta F/\Delta T$, Duration. The digital signal generation scheme is shown schematically in a simplified form in Figure IV. A more detailed presentation may be found in Appendix B.

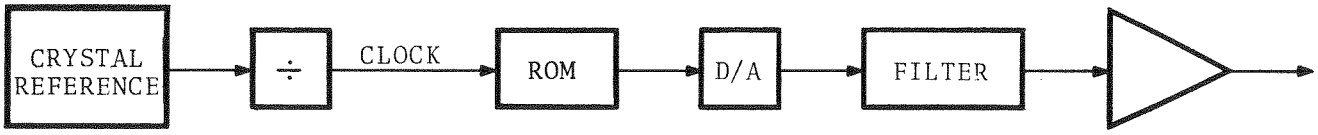


Figure IV

Digital Signal Generator Elements

This technique uses a crystal reference time base, and 2 divider to provide 2 "clock" signal at the required frequency. A ROM (read-only- memory) is programmed with 100 sine coefficients. The ROM is followed by a D/A converter, filter an operational power amplifier.

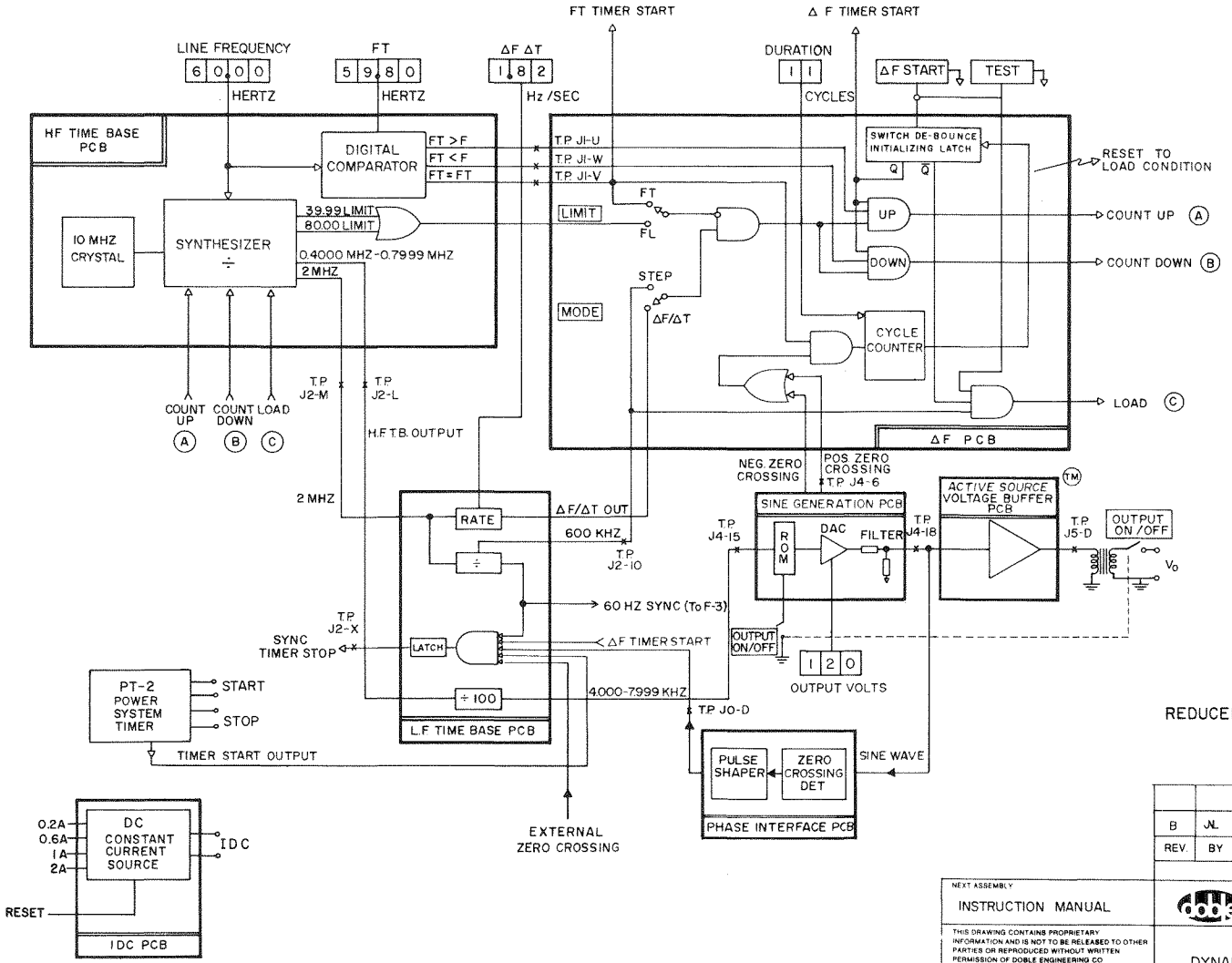
The information contained in the ROM is made available at a controlled, sequential rate, representative of the sine wave frequency. The digital information at each address represents a sine coefficient; this is converted by a digital-to-analog converter (DAC) to an analog quantity. This signal is filtered to eliminate the steps in the sine-approximation and reduce distortion components to well less than 1%. It is then amplified to a suitable level for driving relays.

To insure that the amplifier provides an output starting only at a zero crossing, the control scheme always starts clocking the ROM at the zero address. This digital control technique is superior for this purpose to the phase-interface measuring technique previously discussed because it eliminates any ambiguity due to noise in the analog signal generating/amplification chain; "Output On" skew problems are likewise eliminated since control exists at the signal generation level, rather than at the power amplifier level.

This technique has been expanded to a digital signal generation system which provides for phase and amplitude control of multiple outputs. By using 360 sine coefficients (1° intervals) in a ROM, and clocking the data out in a time sequence representative of a phase angle, polyphase operation is accomplished. A microcomputer provides for control of multiple sine generators. A part of its control function is to enable outputs ("Output On") only at zero crossings. This microcomputer-based digital signal generation instrument also provides for external control of all functions via an IEEE 488 buss interface and external controller using a newly developed, language, ProTesT™. Changes in phase angle, magnitude, off/on functions, as well as $\Delta\emptyset/\Delta T, \Delta V/\Delta T, \Delta I/\Delta T$ functions are included. By loading a series of test parameters into the external controller, dynamic tests of even greater variability may be performed.

Part of the development plan for instruments using digital signal generation and control modules, is an expansion to a 6-output 3 phase system. In this configuration, manual control or external control Via IEEE 488 is possible. An expanded version, which models transmission systems, provides for synthesis of prefault, fault transient and post fault signals. This, in combination with wideband direct-coupled amplifiers, will result in a portable, transient simulator, which can simulate faults as shown in (Reference 15[B]).

MATERIAL LIST				
ITEM	PART NO.	QTY	U/M	DESCRIPTION



REDUCED SIGNAL FLOW DIAGRAM

REV.	BY	CKD	APPR	DATE	ECN
B	JNL	JS HL	RHS	10/21/80	1068

REVISIONS

NEXT ASSEMBLY
INSTRUCTION MANUAL

STANDARD TOLERANCES

DECIMAL DIMENSIONS	0.0	±0.1
DECIMAL DIMENSIONS	0.00	±0.02
DECIMAL DIMENSIONS	0.000	±0.005
ANGLES		±.5°

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
DEBURR ALL SHARP EDGES UNLESS OTHERWISE SPECIFIED

DOBLE ENGINEERING CO.
Watertown, Mass. 02172

FDF
DYNAMIC FREQUENCY SOURCE
FUNCTIONAL BLOCK DIAGRAM

DRAWN	DATE	SCALE
KMF	8/23/79	

DRAWING NO. 75C-0030 REV B
SHT OF

doble
Protection Apparatus Test

APPLICATION NOTE

PHASE CONTROL OF THE F1 BY THE F3'S V_C/I_1 CHANNEL	
AN-7	Original 9/1982

Since the introduction of the Model F1 1 Ø Test System in 1980, users of the Model F3-C and F3-D 3 Ø Test System have benefited from the increased capabilities provided by operating the two instruments together. This is made possible by the F1 To F3 INTERFACE, which provides a signal that locks the F1 in synchronism with the F3. When interfaced together the two instruments can test and calibrate all high burden protective relays, including short-reach impedance, transformer and generator differential, and directional overcurrent relays.

The original F1/F3 interface synchronizes the F1 to V_A, the 0° phase reference of the F3. Since the high fault current supplied by the F1 lags or leads the polarizing voltage or current supplied by the F3 (normally assumed to be 0°), V_B or I_3 must be set to this angle with its lead/lag direction reversed. This may cause some confusion when testing a relay at the angles recommended by the manufacturer.

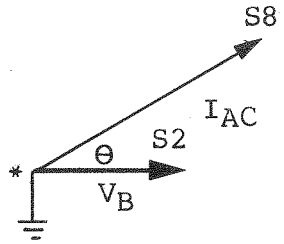
The F1 interface circuit in the F3 can easily be modified to permit controlling the phase angle of the F1 directly by the V_C/I_1 PHASE ANGLE control. With the F1ØC modification installed, the angle of the fault current is dialed directly into V_C/I_1, and the angle of the other voltage(s) and/or current(s) is then dialed into their corresponding controls. This eliminates any confusion that might occur because of the necessity to reverse the phase angles with the original F1/F3 interface.

An inexpensive kit is available for modifying the F3-C or F3-D F1 TO F3 INTERFACE. And for early F3-Cs which did not include an F1 interface, another inexpensive kit is available for installing the interface. Contact the Marketing Department for price, delivery, and installation information.

> **NOTE:** If the F1 output is on when its phase angle is changed by the F3, the F1 error alarm can be tripped, turning the output off automatically. Pressing ENABLE turns the F1 back on at the new phase angle.

Relay Test Plans for high burden relays that require an F1 in conjunction with an F3-C or F3-D show both ways of setting the F3 phase angles. See the example from TP CR/F1&F3CD-1.

D UNIT

TEST	PHASOR DIAGRAM	CONNECTIONS	SETTINGS/REMARKS
Sensitivity @ +30° Maximum Torque Angle	 * C2,C8	S2→R6 C2→R7 S8→R9 C8→R8	V_B = 1 V @ -30° (F1 synced to V_A). -or- V_B = 1 V @ 0° (F1 synced to V_C/I_1 @ +30°). I_{AC} = 1.0 A, 15 A tap. Increase until unit trips... 2.0 A for 0.5-2.5 & 2-6 A, 4.0 A for 4-12 A unit.