Comparison between high impedance and low impedance bus differential protection

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Presented to the

35[st] Annual Western Protective Relay Conference
Washington State University
Spokane , Washington
October 21-23, 2008

1st edition

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Abstract

High impedance bus differential relays are used on most of the busses in North America. The popularity can be explained by the good performance of this scheme in relation to CT saturation and the low cost, if used on a simple bus system. However with the introduction of numerical relays and their low CT burden as well as their ability of measuring several feeder currents, a low impedance bus differential principal could be applied on simple busses also. In addition, the availability of fiber optic communication inside of the substation allows the use of decentralized bus system in which the CT output values becomes transmitted via communication to a centralized unit versus having CT wires running to the control house. Low impedance bus differential protection systems have many positive attributes. Common advantages of all low impedance bus protection schemes are the ability to be able to use CT’s of different ratios on respective branch inputs and the fact that the same CT used for the bus protection can be shared with the feeder protection relay. The question needs to be discussed what selection criteria needs to get evaluated for the selection of the appropriate principal.

The paper will give an overview on both principles and explain the difference in building and evaluating of the differential current. The effect of CT saturation during external and internal faults will be discussed in details for both schemes as well as the CT requirements. Some *advanced numerical techniques* employed in low impedance bus differential relays to recognize CT saturation on heavy through-faults and avoid false tripping are presented. Common guidelines for setting both principles will be reviewed and explained in detail and some examples will be shown.

The influence of the complexity of the bus system on the selection will be discussed. Benefits and disadvantages of both systems will be compared. The comparison will also include the difference during the installation, commissioning, operation and maintenance phase of the different systems. The evaluation will be done technically as well as economically.

Requirements on Bus differential protection

Faults on busses are rare. However, any bus fault will have serious consequences. The main requirements on any bus protection are:

1. **Speed**: The bus protection needs to have a fast operating time. Because of the normally high fault current, the damage of a delayed operation can be critical and in may cases cause evolving events with the damage of critical grid elements like breaker or transformers. Sub cycle protection operations are normally required for the application of bus protection.

2. **Reliability/Selectivity**: Any internal fault needs to be detected and the operation needs to be 100% selective, so that the breakers that are feeding the faulty bus section will be tripped only...

3. **Security**: The bus protection needs to be stable during external faults. This is particularly a challenge for bus protection because the CT measuring the fault current of the faulty feeder becomes often stressed by high fault currents.

The protection engineer has to design the protection of the bus, to comply with all of the above requirements. He has in many cases to find the best compromise between economical requirements, sensitivity, reliability, speed and security. Unfortunately there is no standard answer to achieve this goal. The following considerations should help to understand the options available and give some guidance when and how they can be applied.

Basics

The differential protection principal for high and low impedance differential protection is based on the Kirchhoffs Law, that all currents measured around a protected element (line, transformer, generator, motor, bus) must under normal (non-fault) condition sum up to zero.

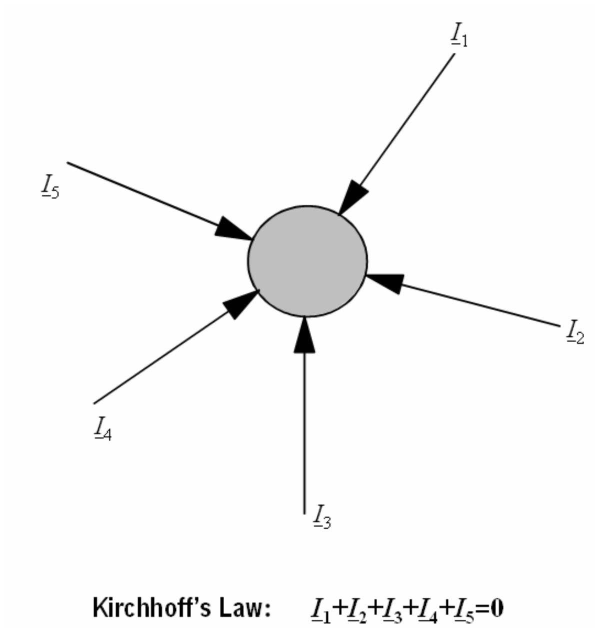

Diagram 1: Basic differential principal

A current sum unequal to zero would indicate a fault in the protected element. The simplest way to obtain this current summation on a bus is by paralleling all current transformer surrounding the bus zone. To be able to do this, all current transformers need to have the same transformation ratio. As shown in Diagram 2, the sum of all current can be measured and an overcurrent element would be sufficient to detect an internal bus fault. On all external faults the measured current would be zero under ideal measurement conditions. Basically all differential protection algorithms are based on this principle. However, the required “ideal measurement conditions” are hard to achieve with inductive current transformer.

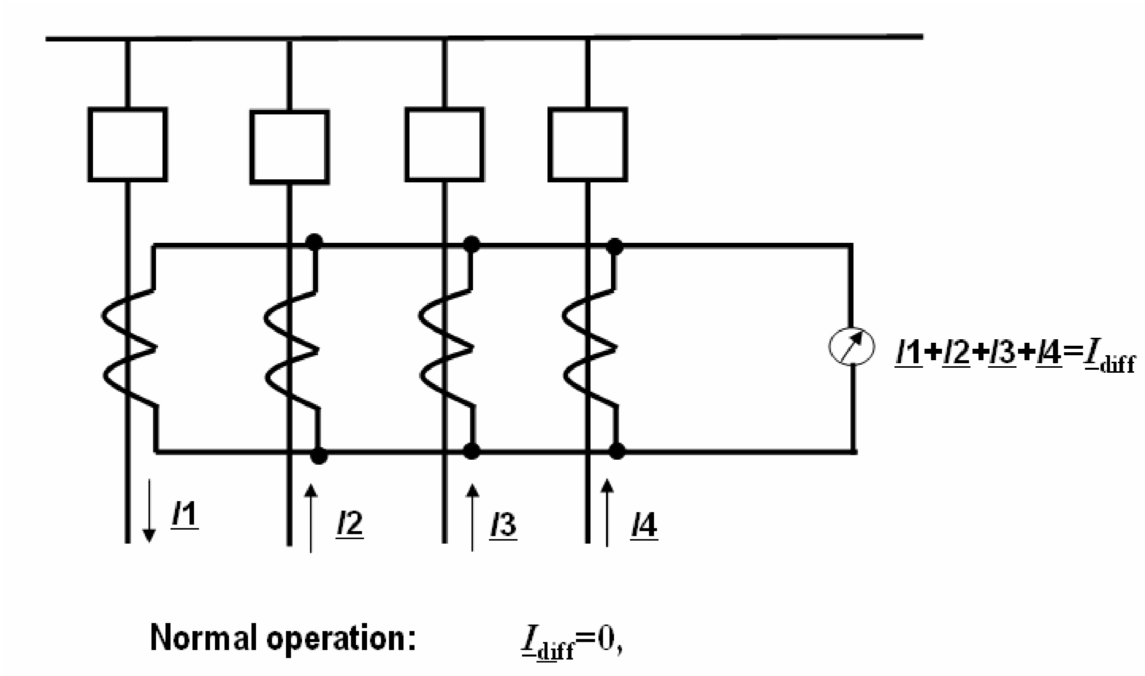

Diagram 2: Simple bus differential application

The two major problems of inductive current transformer are:

1. The accuracy of the current transformer

   The turns ratio of each current transformer has a limited accuracy. In the applicable IEEE or IEC standards, the tolerance can be in a range of 3% to 10% for currents below 20 times nominal current. In the worst case a differential current of 20% of the external fault current would be measured, if one current transformer would measure with -10% and the second transformer with +10% error. The use of a simple overcurrent element for bus protection as shown above can only be applied if the minimum fault current for internal faults is above approx 20% of the external maximum fault current and the CT’s are well sized so that saturation can be avoided.

2. Saturation of the current transformer

Current transformer can only perform a liner transformation of the primary current to the secondary current in a certain range. The range is mainly determined by the amount and the quality of iron used to build the current transformer. Fault current, CT burden and DC time constant of the fault current must be considered during performance evaluation of any given current transformer . On bus protection application also the remanence of a current transformer needs to be considered. When a transformer saturates, it short circuit the secondary current, so that the output current is much lower than actual.

Historically, many solutions were developed to cope with these short comings of current transformers. The following two solutions is presented.

Low impedance Principle

For applications of the low impedance principle, all currents around the protected zone will be measured via CT's and summed up vectorially. This can be done via paralleling all current transformers and measuring the current sum (Diagram 2) or by an algorithm inside a numerical relays which measures each current by a designated input of the numerical relay (Diagram 3). This will have the advantage that different CT's ratios can be used. The numerical relay can compensate for different ratios before it calculates the differential current. In both cases the burden of the current transformers should be as low as possible to avoid saturation of the CT if possible.

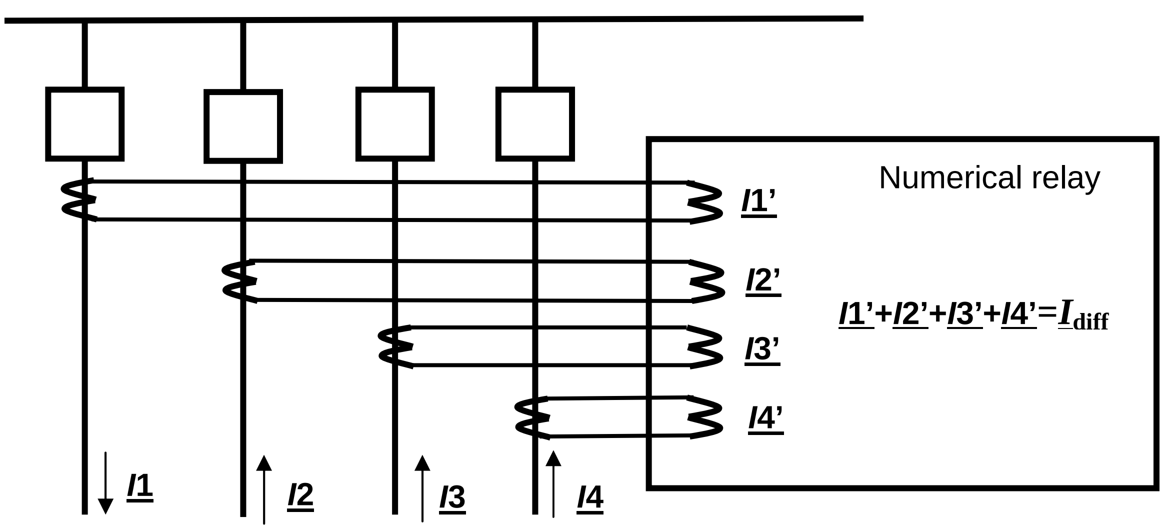

Diagram 3: Low impedance bus differential application with numerical relays

Normally if the trip decision is based only on the current summation, the so called differential current, insufficient security will be offered by the low impedance differential protection scheme. As described above, based on accuracy errors of CT's, an ANSI C-class CT allows errors up to 10%, the differential current for through currents will not end up exactly at zero. The low impedance principal overcomes this problem by introducing a restraint quantity which basically determines how much current is going through the protection zone. The higher the through current, the higher the differential current that is caused by the inaccuracy of the current transformers. Different relay designs will build the restraint value differently and it is important to know how the specific relay derives the restraint value when applying settings to the relay. Most common is the summation of the feeder current amplitude (not vector) or the maximum of the feeder currents. Most differential protective relays are using the so called percentage restraint characteristic. The pick up value for the differential current will be a percentage of the restrain current value The characteristic works in a way that it raises the pick up value of the differential pick up in proportion to the error assumed and expressed as the restraint current.

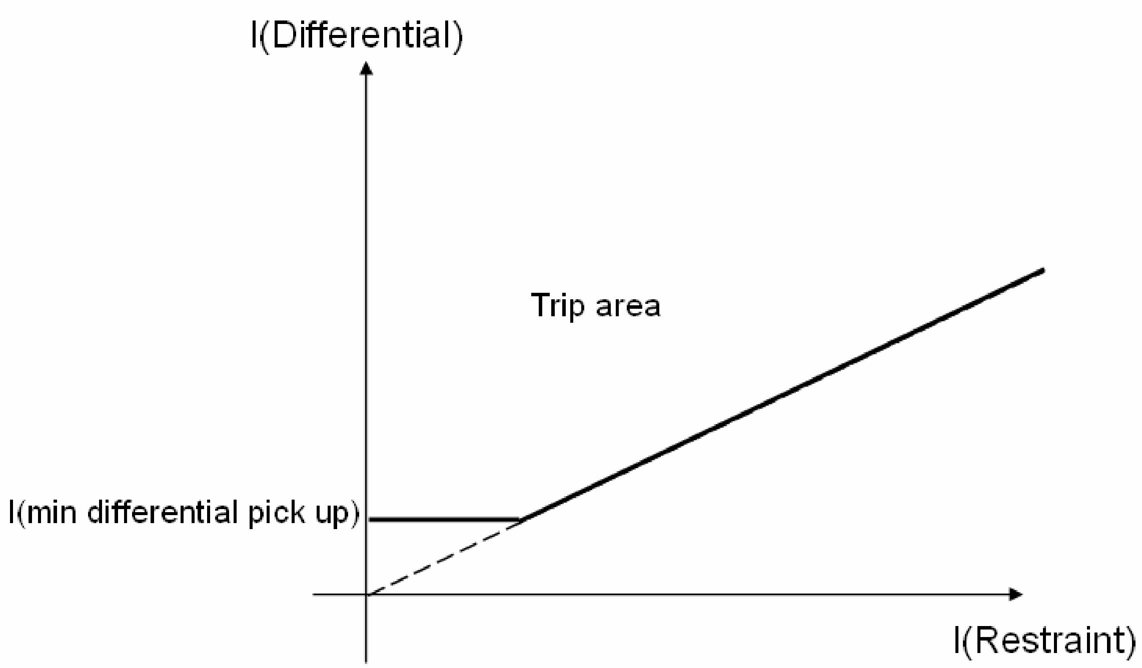

Diagram 4: Percentage restraint characteristic

To set the characteristic, the setting engineer has to calculate a slop setting. If this percentage restrain characteristic should only guarantee stability against the linear error of a current transformer, the current transformer accuracy needs to be considered for the slop value. For example, if the current transformers have a 10% error, the slop setting needs to be 20% plus a certain security margin. This will cover the worst case that one CT has +10% and an other CT has -10% error. Again, it is important to know how the restrain value is calculated to apply the correct slop setting! The percentage restrain characteristic requires normally also a minimum differential pick up setting, because the characteristic may fail for very small differential currents (noise). For bus differential applications a setting which is above the maximum load current should be applied. This will prevent a mis-operation of the protection on any problem with a current transformer during normal load conditions. Most bus protection devices have supervision functions implemented which will detect a differential current caused by a faulty current transformer and alarm this condition before it causes a problem. An internal bus fault will cause enough fault current, so that the minimum pick up setting above maximum load is normally not a restriction.

Saturation with low impedance differential

Besides the linear error, the percentage restrain characteristic can also be used to deal with current transformer saturation. Saturation will occur more likely on high fault currents. It needs to be mentioned here, that saturation can occur with nominal current or even on currents below nominal current if the CT sizing was not done properly.. The DC offset of a fault current, the CT burden, the fault current and the remanence of the CT's needs to be evaluated for the CT sizing for CT's applied for bus differential applications.

If the percentage restrain characteristic is used also to deal with current transformer saturation, an additional restrain characteristic is used, which desensitises the differential pick up value even more as the normal characteristic for very high restraint currents. This is obtained in some relay designs with a second line which is not starting at the zero crossing point and has a higher slop setting.

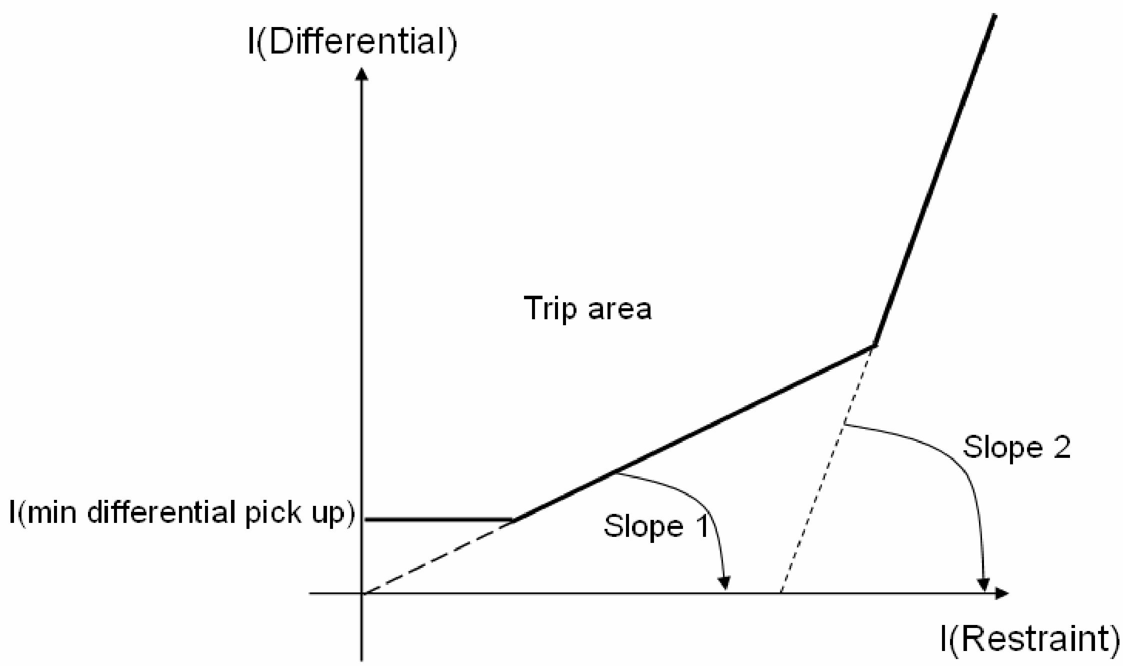

Diagram 5: Percentage restraint characteristic with second slop

However, percentage restraint characteristic has limited ability to stabilize the protection and prevent mis-operating during external fault that causes extreme saturation on only one of the current transformers. The worst case to consider on a bus protection scheme is for an external fault with saturation of one of the CT feeders.. This is a realistic scenario due to the fault current may enter the protection zone distributed to several infeed feeder but will sum up inside the protection zone and leave the zone via the faulty feeder. Translated to the percentage restrain characteristic would the previously described case cause a differential current which is almost as high as the restrain current which is the clear indication for an internal fault. To use the second slop of a percentage restrain characteristic to stabilize the protection will desensitize the protection to a degree that its reliable operation on an internal fault could be jeopardized.

Modern numerical relays have implemented saturation detectors to deal with heavy saturation as described above. One method is to supervise the trajectory of the working point in the Diff/Restraint plane. Saturation on a CT will not happen instantaneously. The CT will at least for the first few milliseconds transform without any saturation. Each manufacturer specifies, to guarantee stability on external faults, the so called saturation free time of the current transformers required by the protection algorithm. An external fault with high fault currents will be seen in the Diff/Restraint plan as a movement from the load point, which is normally on the restraint axis to a point with a much higher restraint value and may be a moderate differential value which will not be high enough to enter the tripping area. Then when the CT starts to saturate the differential value will increase and at the same time the restraint current will decrease a small amount because of the missing current amplitude in the saturated current. This is a situation where a differential relay could operate where no additional measures are taken. One measure could be that the slope of the characteristic is set so high that even under a severe saturation the relay will not operate. The disadvantage is that the relay is then set so insensitive that under real internal faults it would not operate.

Stabilization algorithm

One solution to stabilize the differential protection and improve security also under severe CT saturation is the introduction of an additional saturation stabilization area as seen in Diagram 6.

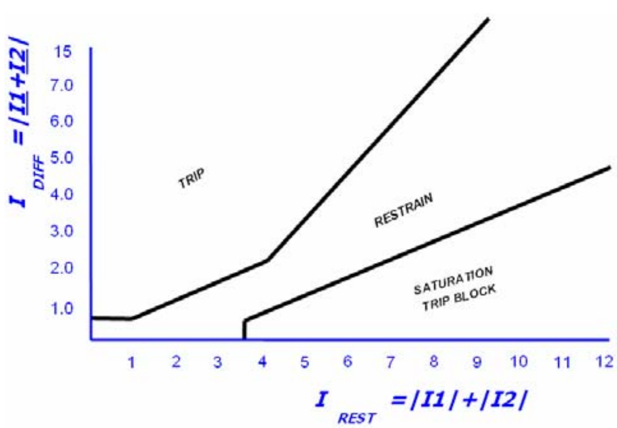

Diagram 6: Characteristic with saturation stabilization area

With this area it is possible to detect the external fault during the first few milliseconds when the CT is not yet saturated. When after entering this area the operating point moves in the tripping area, it becomes assumed, that this is because of saturation and no trip command is generated.

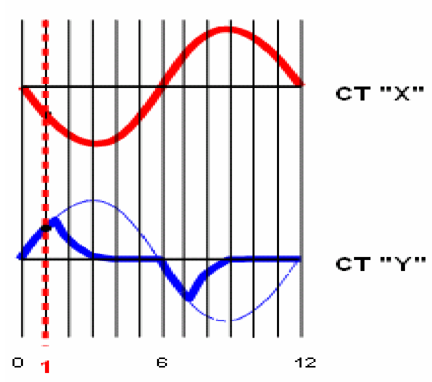

Diagram 7a: Currents with ac-saturation

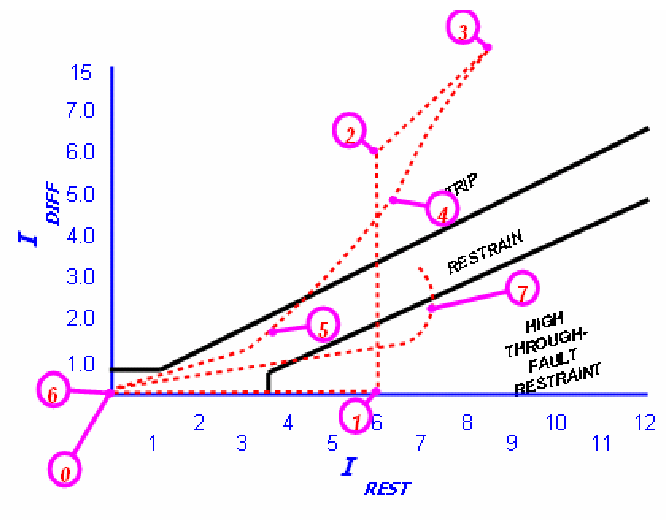

Diagram 7b: Diff/Rest trajectory for with ac-saturation

The blocking of the trip is only necessary for a short time, because on the next half wave the currents will be again unsaturated for a certain time and so pass the saturation stabilization area again so that the blocking timer would be retriggered again. An internal fault will move into the tripping area without passing the saturation stabilization area.

High impedance differential protection

The basic principle of the high impedance protection is the same as the low impedance principal, it sums up all currents measured by the CT's surrounding the bus. The biggest difference is how the high impedance principle handles the problem of CT saturation on external faults. The high impedance principle uses the fact that a saturated current transformer will almost act like a short circuit with a small resistor. In the low impedance application, the relay impedance is normally much smaller as the saturated CT impedance will cause the majority of the differential current flowing through the relay and causing a wrong operation on saturation. The CT impedance during saturation is mainly the resistance of the secondary winding.

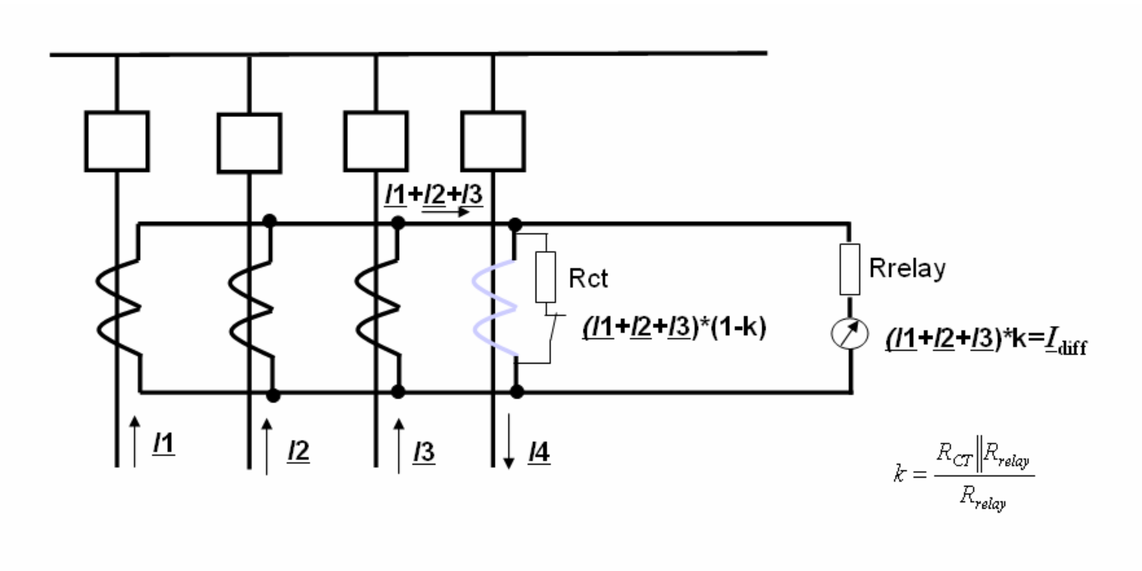

Diagram 8: current split with CT saturation

Example: low impedance

Rct = 0.51 Ohm (ratio 1000A/5A)
Rrelay =0.01 Ohm

$$k = \frac{R_{CT} \| R_{relay}}{R_{relay}} = \frac{\frac{0.51 * 0.01}{0.51 + 0.01}}{0.01} = 0.98$$

On the example above we can see that by using the low impedance principal, that almost all the differential current caused by CT saturation is measured by the protection relay (98%). The high impedance principal uses for this a reason stabilization resistor in series with the relay, to force the differential current to flow via the saturated CT impedance.

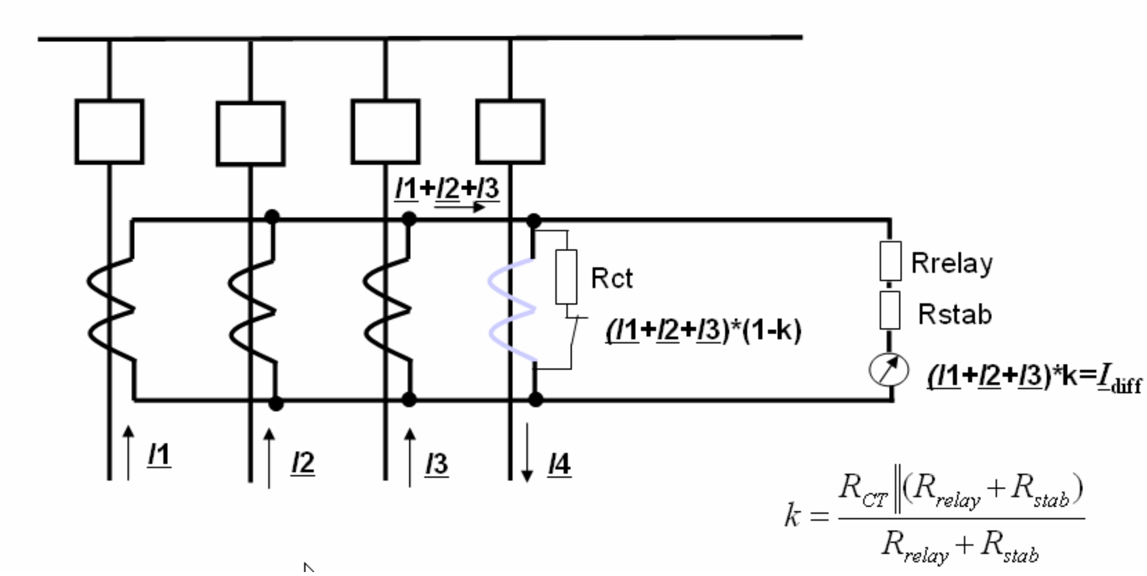

Diagram 9: current split with CT saturation on a high impedance application

Example: high impedance

Rct = 0.51 Ohm (ratio 1000A/5A)
Rrelay =0.01 Ohm
Rstab = 200 Ohm

$$k = \frac{R_{CT} \| R_{relay}}{R_{relay}} = \frac{\frac{0.51 * (0.01 + 200)}{0.51 + (0.01 + 200)}}{0.01 + 200} = 0.0025$$

It becomes obvious that in this situation, the majority of the differential current will flow via the saturated CT impedance bypassing the relay.

Stability
The high impedance principle achieves therefore a good stability for external faults with CT saturation. In detail also the voltage drop across the leads need to be taken into consideration, because they can increase the current through the relay. For stability, the requirement is that the current setting in the relay must be above the current which flows through the relay if on a maximum fault current one CT goes in saturation.

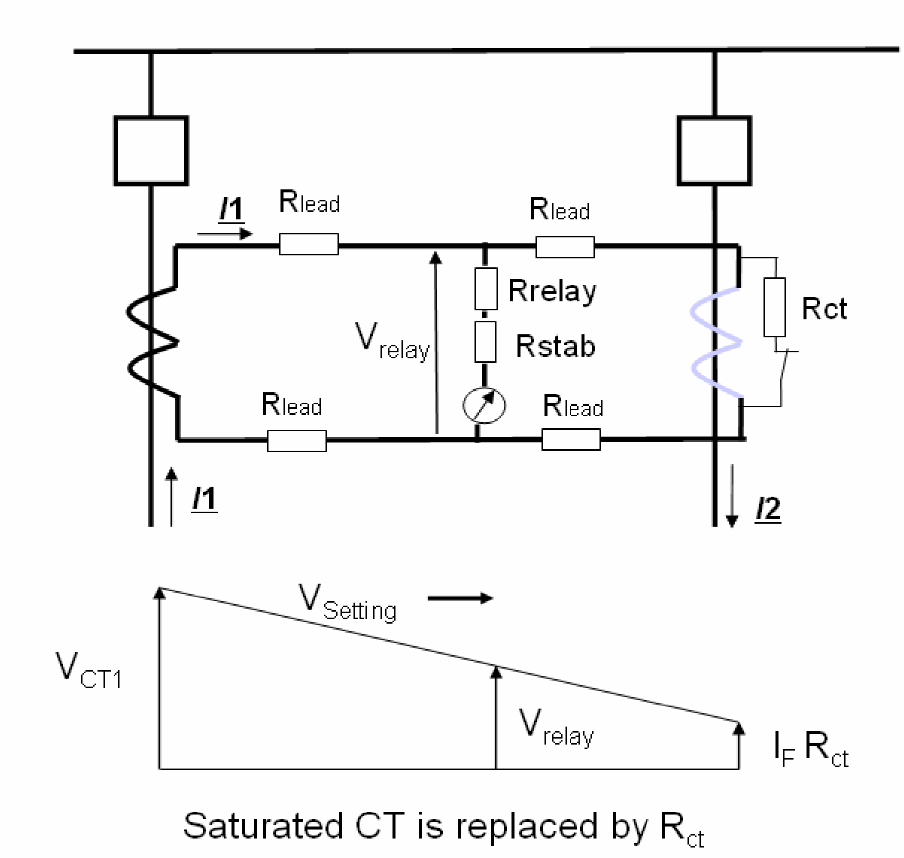

Diagram 10: voltage across the relay for external fault with saturation

To derive calculation formula we want to modify the diagram used earlier in this chapter in a way that it represents the worst case and takes also the lead resistance into consideration. Also is it more convenient to consider the voltage across the relay, assuming that the stabilization resistor is internal to the relay.

Requirement for stability:

$$Vsetting/(2 * Rlead + Rct) > Ifault(max)'$$

Where :

Rlead	:	the resistor of longest wire from the relay to a CT
Rct	:	secondary winding resistor of CT
Ifault(max)'	:	maximum secondary fault current

Sensitivity

For internal faults the current transformers will try to drive a high fault current through the stabilization resistor. This will cause high voltages before the CT saturate, which need to be limited via a varistor. After the relay issued a trip command, the varistor becomes normally short circuit by a relay contact. This is done to protect the varistor against a thermal overload. For the sensitivity consideration the varistor leakage current must also be taken into consideration. The worst case is for an internal fault fed only by one feeder. All other CT's will subtract the secondary fault current by there magnetization current. For this reason it is very important to use low leakage current transformers on a high impedance application.

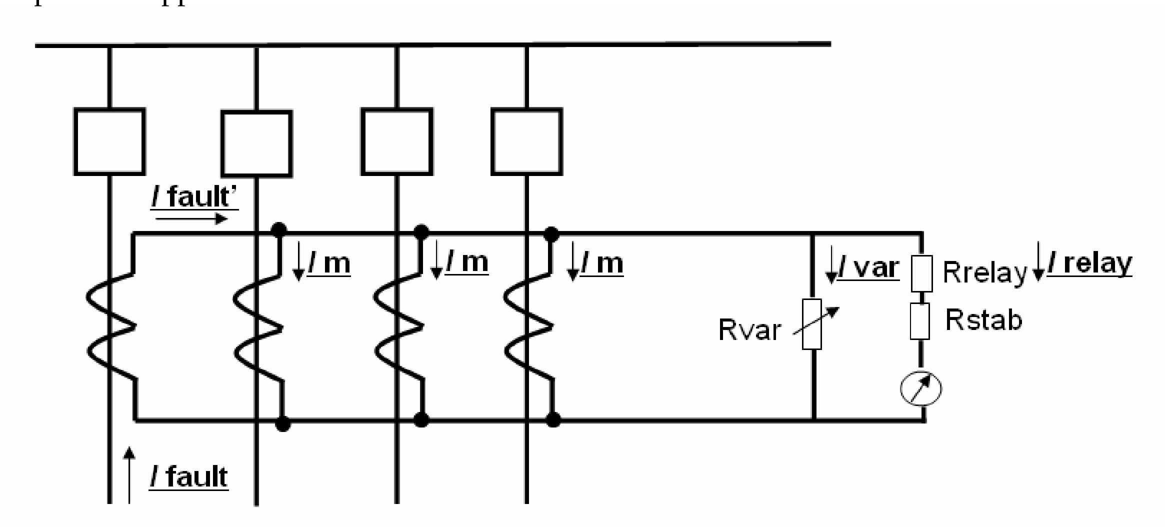

Diagram 11: current distribution on internal fault

Requirement for sensitivity:

Ifault' > n*Im+Ivar+Irelay

Where :

n	:	number of connected CT's
Im	:	magnetization current of CT at relay pick up voltage
Ivar	:	varistor leakage current
I relay	:	pick up setting of the relay

The setting is always a trade-off between sensitivity and stability. A higher voltage setting leads not only to enhanced through-fault stability, but also to higher CT magnetizing and varistor leakage currents resulting consequently in a higher primary pickup current. A higher voltage setting also requires a higher knee-point voltage of the CTs and therefore greater size of the CTs. In general, the kneepoint voltage of the CT's should have twice the voltage of the relay pick up setting. This will guarantee a reliable operation before the CT's go into saturation.

On bus protection a pickup value above the maximum load current is normally applied. An increased pickup current value can be achieved by connecting a shunt resistor in parallel to the relay.

General requirements on high impedance differential applications

1. All current transformers need to have the same ratio.

2. The CT's should have a low magnetization current, because for an internal fault this will reduce the sensitivity.

3. The resistor of the wiring from the CT's to the junction point should be as small as possible and not be too different for the different CT's.

4. High voltages are generated on internal faults. The voltages will normally become limited by a varistor. The insulation of the wiring needs to be rated for the voltage limited by the varistor.

5. The current transformer used for the high impedance application should not be shared with other applications.

6. Each bus zone needs a dedicated relay with dedicated CT's assigned to it.

Conclusion

The paper gave an overview on both principles and explains the difference in building and evaluating of the differential current. The effect of CT saturation during an external and internal fault was discussed in details for both schemes and CT requirements are defined. Common guidelines for setting both principles where reviewed and explained and some examples where shown.

The high impedance principle has an excellent performance in relation to stability on external faults with CT saturation. Many engineers claim also that the high impedance principle is more economically as the low impedance principle. The author of this paper disagrees with this assessment. By adding the actual costs of installation, commissioning and maintenance and compare it with the cost associated with low impedance and considering the use of dedicated CT'for high impedance bus protection may favor the application of the low impedance principal with numerical relays. This is a fact on more complex bus systems with double buses, triple buses or busses with several different sections. The low burdens of modern numerical relays mitigate the problem of CT saturation to a certain degree. In addition numerical relays offer more sophisticated algorithm to deal with saturation. However, the sizing of CT's must guarantee the required saturation free time of the CT under all conditions. If this requirement can be met, the application of the low impedance principle will offer the following advantages:

1. The low impedance principle can share CT's with other applications as the actual feeder protection for example.

2. The fault analysis is more sophisticated because all feeder currents are recorded and available for the analysis of internal and external faults.

3. The low impedance principle will not produce high voltage spikes which will challenge the isolation of the wiring.

4. Commissioning and installation is easier because the requirements are simpler.

5. The assignment of feeder currents to a certain bus zone on complex bus systems (double, triple, …) is managed inside the numerical relay and require no switching of CT's.

The experience of the protection engineer and the requirement of the specific utility application need to be also factored in the selection of the appropriate bus protection principles, in spite of the advantages offered by the low impedance bus protection schemes. On simple, single bus systems the advantages and disadvantages of both systems must be evaluated and based on the actual application one or the other will be best for the application. It is the opinion of the author that on complex bus systems the low impedance principle, realized with modern numerical relays will always offer advantages in security and reliability. Also the installation, maintenance and operation will be much easier with a numerical low impedance relay.

Reference

[1] Blackburn, J. L., Protective Relaying: Principles and Applications. New York: Marcel Dekker, Inc., 1987

[2] Ziegler, G., Numerical Differential Protection: Principles and Applications. Siemens AG, Berlin and Munich, 2005

[3] H.-J. Herrmann and G. Ziegler: Coordination of CTs and Digital Relays, Guidelines and Recent Practice, Relay Symposium, Monterrey 2004

[4] IEEE Std. C37.110 Guide For The Application Of Current Transformers Used For Protection Relaying Purposes, 1996

Biography

Dr. Juergen Holbach is manager of operation at Siemens Energy, Inc in Wendell North Carolina. He was born in Germany and graduated from the University of Berlin with a PhD in Electrical Engineering. He jointed the Siemens AG in 1992 as a development engineer in Berlin Germany. In 1994 he moved to the product management group for protection relays in Nuremberg Germany. Since 2000 he works for Siemens Energy, Inc in Wendell, NC where he started as a product manager for transmission relays. Juergen is member of several IEEE-PSRC working groups as well as CIGRE working groups and holds several patens in the field of protection relaying.

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