A MICROPROCESSOR BASED UNDERFREQUENCY LOAD SHEDDER

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ABSTRACT

For underfrequency protection on the Edmonton Power System and to implement the Alberta Interconnected System Underfrequency Load Shedding Policy, a microprocessor based underfrequency load shedder has been developed. In this system, a microprocessor computes frequency from the power system voltages and performs load shedding in seven discrete preset frequency levels. It is programmed to interface with the SCADA system which will be able to perform load restoration and read messages recorded in the load shedder memory. Using the SCADA system, the load shedder settings can be applied from the supervisory control centre.

History of the project, design and working of the load shedder are briefly discussed in this paper. Laboratory tests and field performance of the system have been satisfactory.

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INTRODUCTION

A power system is operating normally when the power generated is balanced by system load and losses. A sudden loss of a large block of generation can result in a severe mismatch of generation and load. This imbalance causes the power system frequency to decline. Depending upon the severity of the imbalance, the power system can collapse in a short time if immediate steps are not taken to arrest the frequency decay. Low frequency if allowed to persist for longer times can damage the turbine blades. Electric power utilities arrest this frequency decay by dropping predetermined blocks of load at specified levels of frequency using automatic underfrequency relays. Once generation and load balance is achieved, the previously dropped load blocks are gradually added to the system as the generation capacity is brought back online. Normal power system operation is again achieved when all the load blocks are reconnected.

Conventional underfrequency relays respond to frequency decline with the preset time delay. In solid state relays, the inherent delay is generally constant and in electro-mechanical relays this delay varies with the rate of frequency decay. Solid state underfrequency relays using frequency as well as rate of change of frequency are also available for load shedding. A survey conducted by the working group of power system relaying committee of the IEEE shows that the underfrequency relays based on frequency and rate of frequency are not very popular and are not widely used by the power utilities. Most of the underfrequency load shedding and restoration systems installed by the power industry are conventional solid state (electronic) or digital relays. This paper presents a new underfrequency load shedding and restoration system which uses a microprocessor to measure the power system frequency. When the frequency decreases, load shedding is done in seven (7) preset frequency levels. As the frequency recovers above the restoration frequency level and stabilizes, seven (7) discrete signals are sent to the SCADA system for load restoration.

Thirteen underfrequency load shedding units were manufactured, rigorously tested and installed in the Edmonton Power's 15 kV distribution stations. Installation and commissioning of the load shedders were completed in 1985. These load shedders are performing satisfactorily and remain stable during switching and fault conditions.

HISTORY

The purpose of this project was to develop an underfrequency load shedding and restoration system which will perform load shedding as recommended by the task force appointed by the Alberta Interconnected System Operations and Maintenance Committee. The task force did extensive research on the different approaches taken by other power pools to maintain the integrity of an interconnected power system when a sudden loss of generation occurs. Computer simulations on load patterns and frequency excursions under different contingencies were performed. Based on these studies, Alberta Interconnected System underfrequency load shedding policy was developed. Some recommendations of this policy are listed below:

(i) All electro-mechanical relays (u.f.) on the Alberta Interconnected System be replaced by solid state relays. These new relays must meet the following criteria:

a) Tripping Frequency

Variable frequency settings with $\pm$ 0.05 Hz accuracy.

b) Trip Time Delay

Fixed time delay not greater than 10 cycles.

c) Operating Voltage Range

The relay must maintain tripping accuracy in the voltage range of 70%-115% of the normal voltage.

d) Operating Temperature Range

The relay must maintain tripping accuracy in the temperature range 0-40^{o}C.

(ii) Each utility will shed 50% of its connected load.

(iii) Each utility will shed its load in seven (7) approximately equal blocks. First load block will be shed at 59.3 Hz followed by other load blocks at declining intervals of 0.2 Hz.

(iv) The load shedding scheme must attempt to match the amount of load shed to the amount of generation lost to minimize the effect to customers and reduce the recovery over shoot.

A load shedding and restoration system has been designed and developed to incorporate above recommendations of the task force. This system is the first of its kind and is briefly described in the following sections.

UNDERFREQUENCY LOAD SHEDDING AND RESTORATION SYSTEM

The underfrequency load shedding and restoration system designed and developed in this project is housed in a 2286 x 610 x 635 mm dust proof assembly. The system uses a microprocessor to perform underfrequency load shedding and restoration. It processes and monitors the voltage and frequency of five 120 V, 60 Hz signals called channels. The system is programmed to trip 64 auxiliary relays (feeders) at seven (7) different trip frequencies referred to as levels. These seven trip levels and the eighth restoration level can be set in the range 55-61 Hz. Any single feeder or a number of feeders can be associated with any one channel and any one trip level.

The system continuously monitors the voltages and frequencies of all the five channels. When the frequency/frequencies drop below a preset trip level or levels, associated breakers are tripped. As the frequency recovers and stabilizes above the restoration level for the preset restoration delay/delays, commands are sent to the SCADA system to restore the tripped breakers. Messages such as excursion frequency trip time and date, restoration time and date, channel fail, power supply fail, SCADA communication fail, etc., are stored in the RAM which is updated as the events occur. The messages can be read locally on the load shedder LCD display or sent to the SCADA system when requested, where these messages are displayed on the screen and can be stored for system analysis and planning.

The load shedding and restoration system is described by the functional block diagram shown in Figure 1. Input subsystem, CPU, output subsystem, SCADA interface, uninterruptible power supply and operator's console are the major functional blocks of the load shedder. The input subsystem receives power system voltage signals, processes these signals and keeps track of the clock frequency counts between positive going zero-crossings of the processed signals. Using these counts, the central processing unit calculates signal frequency and checks whether the power system is experiencing underfrequency conditions for load shedding and restoration. Decisions of the CPU are conveyed to the output subsystem for load shedding and to the serial I/O to communicate with the SCADA system for load restoration. Uninterruptible power supply unit supplies necessary power to all the components. Relay settings are applied locally using the operator's console or from the central control room through SCADA system. These functional blocks are briefly described in the following text.

INPUT SUBSYSTEM

Figure 2 shows the signal flow diagram for the input and the output subsystems. The 120 volts signal from the power system PT is applied to the isolation transformer equipped with surge protection to arrest high voltage spikes. The isolation transformer steps the signal

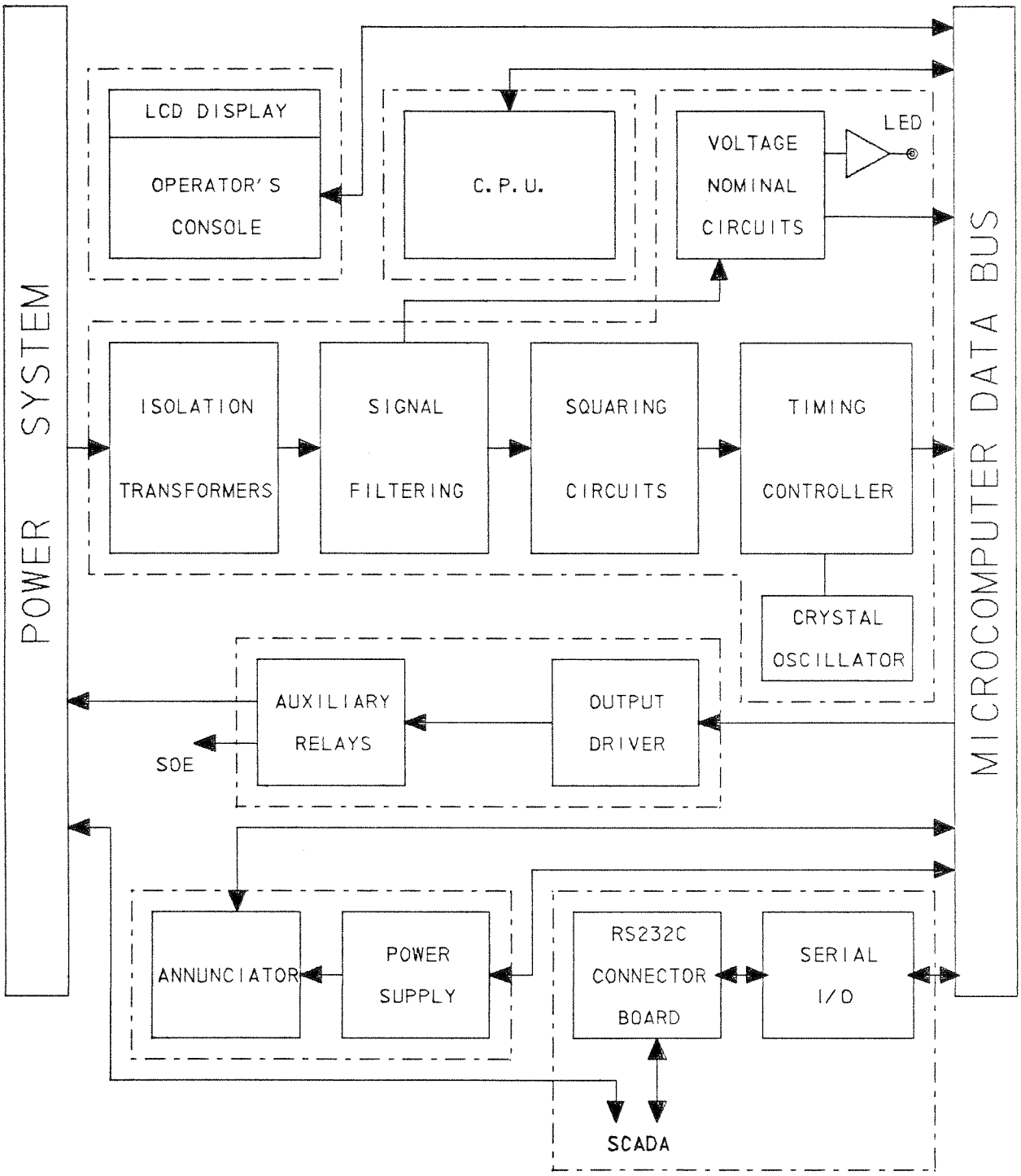

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE LOAD-SHEDDING AND RESTORATION SYSTEM

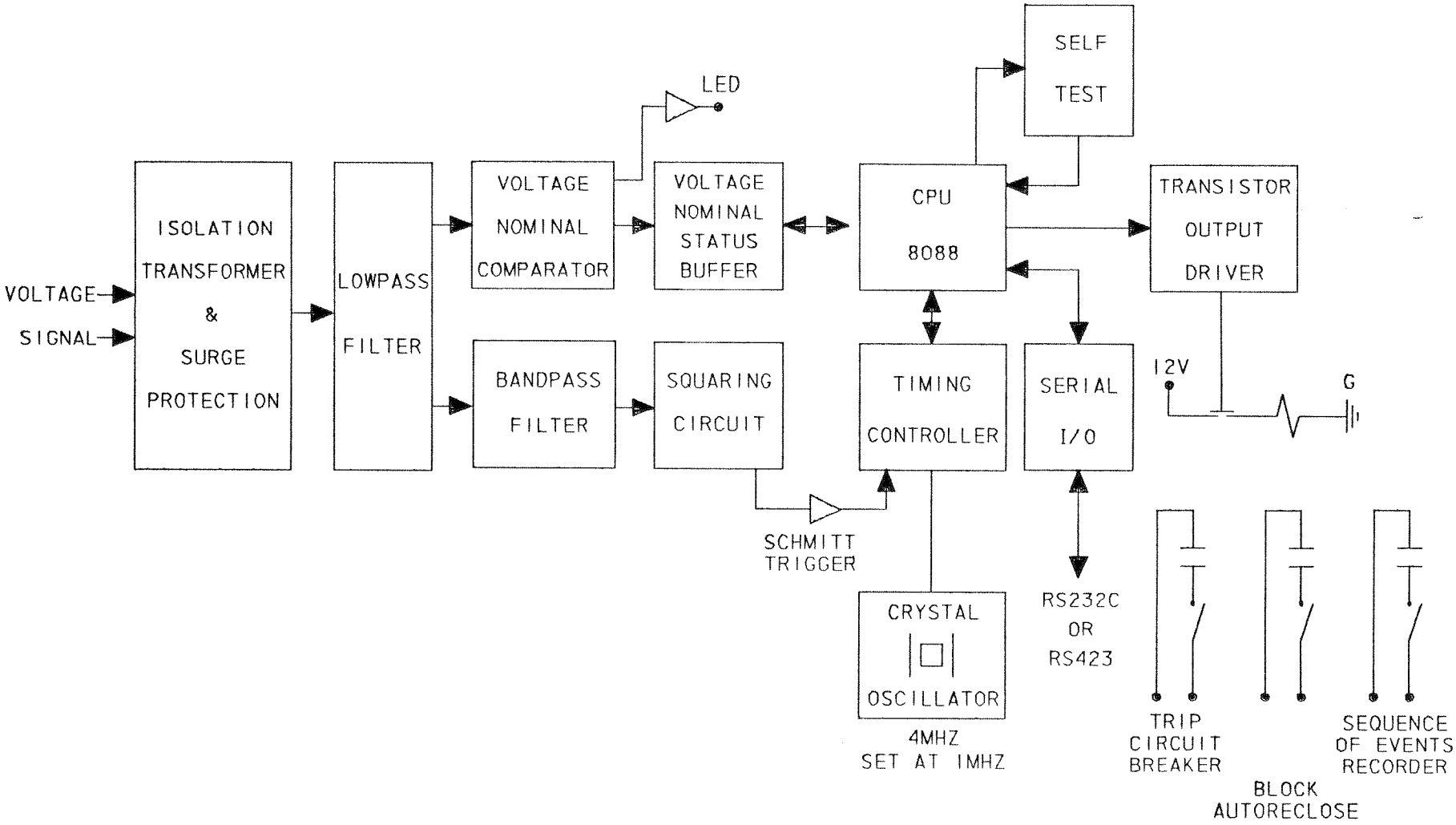

FIGURE 2. SIGNAL FLOW DIAGRAM OF THE INPUT AND OUTPUT SUBSYSTEMS

down to 10 volts which is then passed through a lowpass filter to suppress high frequencies (spikes). Output of the lowpass filter is applied to two parallel circuits which measure clock frequency counts between consecutive positive going zero-crossings and monitor the voltage magnitude. These circuits are referred to as signal conditioning circuit and input voltage supervision circuit and are briefly discussed in this section.

Signal Conditioning Circuit

This circuit comprises of a bandpass filter, a squaring circuit, a Schmitt trigger and a timing controller. The bandpass filter suppresses the harmonic and subharmonic frequencies present in the incoming signal and the clean signal is applied to the squaring circuit. The squaring circuit converts this signal into a square wave as shown in Figure 3b. The square wave is then applied to a Schmitt trigger the output of which is connected to the timing controller. The timing controller, comprising of a count register, a load register and a hold register, derives its time base from a 4 MHz crystal oscillator which is set at 1 MHz frequency reference. The crystal oscillator frequency counts that take place during two consecutive positive going zero-crossings of the aforementioned square wave (shown in Figure 3c) are counted and held in a count register. This count is the period of the measured signal given in microseconds. After each positive going zero-crossing, the contents of the count register are transferred to a hold register via a load register. At the same time the count register is re-initialized. The CPU reads the hold register (signal period) and calculates the power system frequency as described in the next section.

Signal Voltage Supervision Circuit

Equation 1 in the next section shows that the frequency measurement depends upon the clock (crystal) frequency and the clock frequency counts between positive going zero-crossings. This equation is independent of the signal amplitude indicating that the calculated frequency is not affected by voltage variations over a wide range. In certain underfrequency load shedding applications, amplitude of the signal voltage for frequency measurement is very important. It has been observed that the voltage and frequency of the circuits supplying motor loads do not fall to zero immediately when the circuit is de-energized. The voltage and frequency of such circuits decay depending upon the load and circuit characteristics. The situation of voltage and frequency decaying slowly may also be encountered in other cases. Frequency measurement from signals derived from PTs connected to such circuits may lead to undesired load shedding especially when a number of feeders are shed from the load shedder.

In order to avoid above problem, a voltage supervision circuit has been included. This circuit monitors amplitude of the input signal to ensure that the frequency measurement is done only when the signal

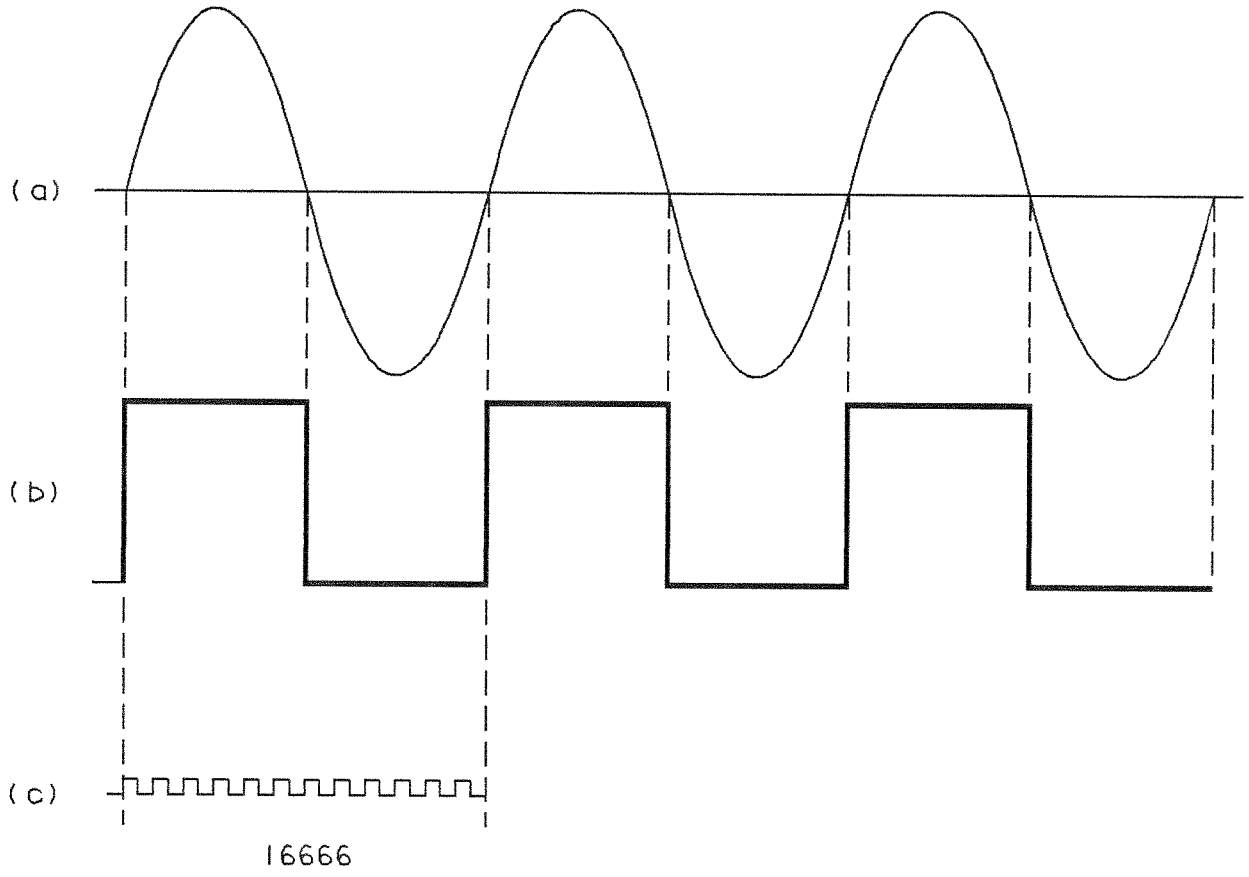

FIGURE 3. (a) INPUT TO THE SQUARING CIRCUIT (b) OUTPUT OF THE SCHMITT TRIGGER (c) NUMBER OF CRYSTAL FREQUENCY COUNTS BETWEEN POSITIVE GOING ZERO CROSSINGS.

voltage is above a preset threshold. The threshold voltage is set at 70% of the nominal value. The incoming signal amplitude is compared with the threshold and if it exceeds the threshold, a monostable multivibrator is triggered. The multivibrator maintains its output as long as the signal amplitude is above the threshold value and the output is indicated by an LED. There is no indication when the signal is below the threshold value and a signal voltage fail alarm message is recorded.

Output of the monostable multivibrator is applied to a buffer. Output of the buffer is one (1) when multivibrator output is maintained and zero (0) when it is not maintained. The CPU reads the buffer and checks if the counts read from the hold register (explained before) are valid or not.

CENTRAL PROCESSOR UNIT (CPU)

The Central Processor Unit (CPU) is based on Intel 8088 microprocessor. The system has 32K erasable programmable read only memory (EPROM) and 6K read only memory (RAM). Main program and the default values of the settings are stored in the EPROM. Load shedding parameters, SCADA information and the system messages are stored in the power fail, battery backed up RAM.

The CPU is programmed to calculate frequencies of the input signals, do load shedding and restoration, perform some self-diagnostics and communicate with the SCADA system. These functions are briefly described in this section except the SCADA link which is discussed in a separate section titled "Communication with SCADA".

Frequency Measurement

As explained in the last section, contents of the hold register in the signal conditioning circuit and the buffer in the voltage supervision circuit are read by the CPU. The CPU checks the voltage nominal status buffer to determine whether to calculate signal frequency or not. Counts coming from the hold register are rejected if the bits read from the buffer are zero (0) signifying low voltage input. When the bits read from the buffer are one (1) i.e. signal voltage is above the threshold value, signal frequency is calculated using the following equation:

$$f = \frac{Fc}{N} \qquad (1)$$

where f is the power system frequency
Fc is the clock frequency which is equal to 1 MHz
N is the number of clock frequency counts between positive going zero-crossings (period of signal in microseconds)

additional preset trip delay (if applied), the CPU issues signals to trip breakers which are set to be tripped at that level. Trip output data from the CPU is buffered, decoded and transferred to respective latches. The latched output is then applied to the integrated circuits which energize the 12 volt DC coils of the associated auxiliary relays. The latched output can be pulsed with a pulse duration settable between 0.1 - 10.0 seconds or it can be maintained as long as the signal frequency stays below the threshold frequency. The trip outputs can be enabled or disabled when applying the software settings. Tripping contacts of the auxiliary relays are wired through Westinghouse FT blocking switches. Each trip output is indicated by a semaphore which can be reset by depressing the corresponding push button.

COMMUNICATION WITH SCADA

The load shedder uses RS 232C/RS-423 or RS-422 interface to communicate with the SCADA system. The information is transmitted serially at baud rates settable between 110-9600 baud.

While discussing the load restoration procedure it was explained that the load shedder is programmed to do the underfrequency load restoration through SCADA system. In addition to load restoration, all the functions that can be performed locally at the load shedder console can also be performed remotely using the SCADA system except the hardware diagnostics which can be performed effectively at the console only. The SCADA system can read and revise the channel, level and feeder setting parameters when desired. Messages such as AC or DC power supply fail, channel fail, breakers tripped, trip time and date, lowest excursion frequency and restore time and date, etc., from the load shedder can be read by the SCADA system from time to time. These messages, signal running frequencies and the load shedder setting parameters for all the load shedders can be displayed on the SCADA screen in the central control room. Failure of the SCADA link does not affect the performance of the load shedder. Five (5) minutes after the SCADA link has failed, the load shedder starts SCADA communications fail alarm and continues to alarm until it is acknowledged. Data stored in the load shedder RAM can be read by the SCADA system as soon as the communication link is restored.

POWER SUPPLY

The load shedder is equipped with uninterruptible power supply comprising of 120V AC referred to as the main supply and 24V DC battery referred to as the standby supply. Both the main and the standby supplies are monitored and their statuses 'AC OK', 'AC FAIL' and 'DC OK', 'DC FAIL' are indicated by LEDs. When the main supply fails, the standby supply takes over with no interruption in the load shedder working and station alarm and remote alarm auxiliary relays are

energized. Power fail message is sent to SCADA system. In addition to the main and standby power supplies, the load shedder is also equipped with NICAD rechargeable batteries which support the RAM, containing system messages and parameters, in case both main and back up supplies fail. The NICAD batteries are capable of supporting the RAM and time of day and date clock for approximately 1000 hours. When both main and standby power supplies fail, all trip outputs from the load shedder are blocked.

OPERATOR'S CONSOLE

The load shedder is equipped with a console having a 40 character alphanumeric LCD display and a 32 key keyboard. The keyboard consists of 0-9, A-F character keys and some function keys such as acknowledge alarm, communication status, display test, enter, clear, memory read, memory write and read message, etc. Using this console, the operator can alter the parameters, read messages, view and reset accumulated information, examine and change any memory location. It is also used to read channel frequencies, display date and time of day and annunciate the occurrence of an alarm. Hardware and software diagnostics can be performed on the console.

TESTING THE LOAD SHEDDER

The load shedder was specified by Edmonton Power with detailed design programming and manufacturing by Datek Industries Limited. Tests for load shedding and load restoration through SCADA were performed. The load shedder successfully passed all these tests. It remained stable during heat test performed at $50^{o}C$ for 24 hours. Hardware input and output circuitry was improved to enable the load shedder to pass the IEEE SWC tests.

The load shedder was vigorously tested in the field. Fault signals containing fundamental, harmonic frequencies and decaying DC were applied. The load shedder remained stable under these transient conditions. No maloperation was observed when a radio frequency source with a frequency range of 30-470 MHz at 5 watts nominal rated power was placed in the load shedder panel. The system also remained stable for walkie talkies operating near or inside the panel. Underfrequency signals decaying at the rate of 1-10 Hz per second were generated using a Doble test set and were applied to the load shedder. It operated exactly as per settings applied for different levels, channels and feeders.

INSTALLATION AND FIELD EXPERIENCE

First unit was installed and commissioned in March, 1984 and the last of the thirteen units was installed and commissioned in November, 1985. Except for some minor problems, the installation and commissioning of the load shedders went smoothly. From March, 1984 to July, 1986 the Alberta power system experienced about nine underfrequency excursions. Lowest value of power system frequency excursion experienced for a period of equal to or more than 166 milliseconds was 58.9 Hz. The load shedder captured all these underfrequency conditions and performed the load shedding as per settings applied. No undesired tripping has been reported so far. The load shedders remain stable during power system faults, transient and switching conditions.

CONCLUSION

The paper has presented a new system developed to provide underfrequency protection on Edmonton Power System as per Alberta Interconnected System Underfrequency Load Shedding Policy. Basic design and functional blocks of the load shedder have been briefly discussed. It has successfully passed extensive acceptance testing and has been in service for more than two years. Field experience of the load shedders shows that their performance during power system underfrequency conditions experienced so far has been satisfactory.

ACKNOWLEDGEMENTS

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