
COMPLETE RELAY PROTECTION OF MULTI-STRING FUSELESS CAPACITOR BANKS

**Leo Fendrick
Lincoln Electric System**

**Tim Day • Karl Fender • Arvind Chaudhary
Cooper Power Systems**

Presented to the
**28th Annual
Western Protective Relay Conference
Spokane, Washington
October 23–25, 2001**

COMPLETE RELAY PROTECTION OF MULTI-STRING FUSELESS CAPACITOR BANKS

Leo Fendrick
Lincoln Electric System
Lincoln, Nebraska

Tim Day
Cooper Power Systems
Franksville, Wisconsin

Karl Fender
Cooper Power Systems
Greenwood, SC

Arvind Chaudhary
Cooper Power Systems
South Milwaukee, Wisconsin

Abstract:

The trend towards large fuseless shunt capacitor banks being employed in power systems is due to the lower cost, compact design, higher reliability with less exposed live parts, and lower losses.

This paper describes a novel application of the impedance method to provide complete bank protection by measuring the impedance of each series string of the capacitor bank.

The scheme can identify the string(s) with an alarm or trip condition, keep the bank in service with pack failures in multiple strings, and only trip when the bank is actually in an unacceptable operating condition.

Traditional Protection of Large Shunt Capacitor Banks

Traditionally, large shunt transmission capacitor banks were made up of parallel groups of capacitors. Then these parallel groups were connected in series to provide the required line-to-ground voltage rating.

For example: Each phase of a traditional 69 kV wye/119.5 kV bank could be made up of five series groups of paralleled 13.8 kV capacitors. Each individual capacitor unit is protected with its own fuse.

Bank protection typically was provided by a voltage unbalance scheme. For our example above, a VT on each phase would be connected from ground to the connection point between the 2nd and 3rd parallel group. The normal voltage output would be 2/5 of the phase-to-ground voltage. This voltage output would then be monitored to verify that it was in the acceptable bandwidth.

Fuseless Large Shunt Capacitor Bank

In contrast, a fuseless bank is made up of multiple series strings in parallel to get the desired bank size. There are no interconnections between the series strings.

For example: Each phase of a fuseless 69 kV wye/119.5 kV bank could be made up of four 17.25 kV capacitors connected in series to get the line-to-ground voltage rating. Series strings are then added in parallel to get the desired Mvar size.

Lincoln Electric System (LES) selected a fuseless bank for the lower exposure of the bank due to the fact that there are no fuse rails, no individual fuses, and live parts are insulated. The bank is also more compact, lending itself to the possibility of expanding it to 75 Mvar. The safe failure mode of the all-film capacitor was another factor. It was also desired that the protection be expandable to provide protection for the future strings that could be added.

LES chose the 33rd & Superior Substation location for the capacitor bank location. The single line of the 33rd & Superior Substation is shown in Figure 1. A photo of CB 3391 and the bank is shown in Figure 2, and a close-up of Phase A is shown in Figure 3. The connection of each string of the bank terminates in a medium voltage current transformer at the neutral bus end of the bank. There is a provision for future strings to be added to the same structure.

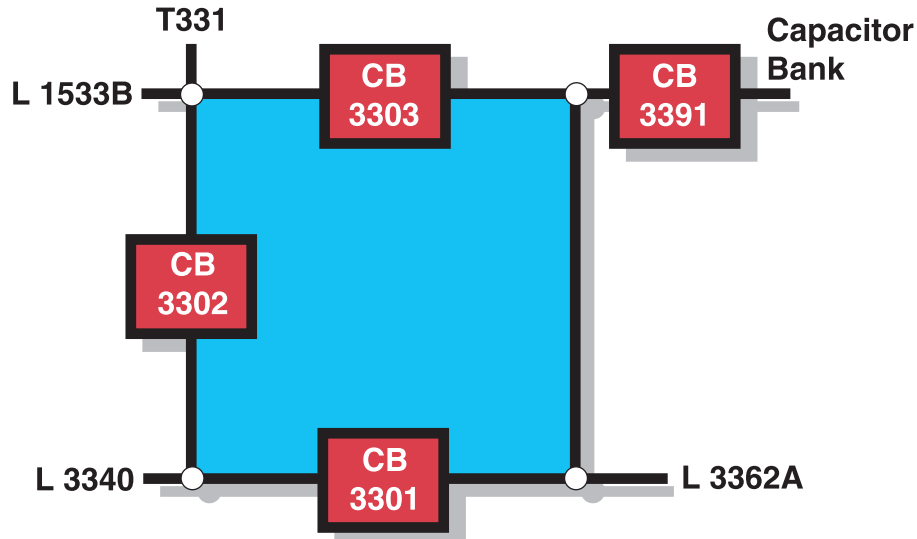


Figure 1.
Circuit breaker 3391 (center) and capacitor bank (right).

The reactor located at the top of the bank reduces the outrush current magnitude and frequency for close in external faults to within the ($I_{peak} \times \text{frequency}$) product of the synchronous closing circuit breaker.

The initial configuration of the bank was chosen to be eight strings per phase (expandable to 12 strings per phase) with four capacitor units per string, with each can rated 17.25 kV, 550 kvar. The initial bank is rated 69 kV wye/119.5 kV, 52.8 Mvar, and it is expandable to 79.2 Mvar. Each capacitor unit is constructed internally of nine series sections of two parallel-connected elements. The total number of series sections in one phase is 288 ($9 \times 4 \times 8$).

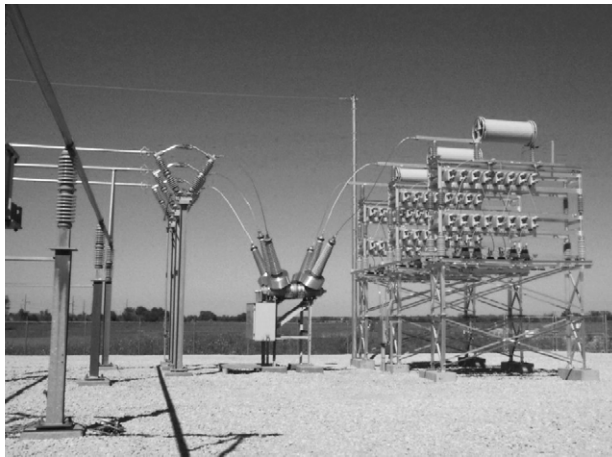


Figure 2.
Circuit breaker 3391(center) and capacitor bank (right).

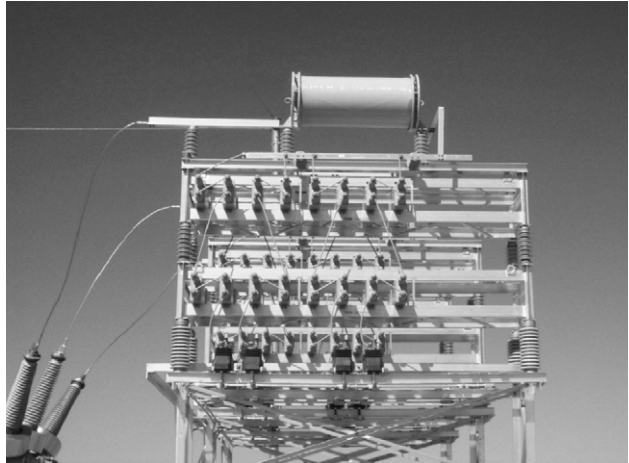


Figure 3.
Phase A.

Protection Concerns of the Initial Scheme

Investigation of the actual unbalance signal levels started the process of selecting the impedance method. Initially, the bank was proposed as a single grounded-wye bank with protection provided by a voltage differential scheme. The voltage differential scheme compares bus voltage to the voltage across low voltage capacitor(s) placed at the neutral end of each capacitor bank phase. This typical protection is illustrated in Figure 4. The voltage differential relaying is able to identify the faulted phase and is not affected by system unbalance.

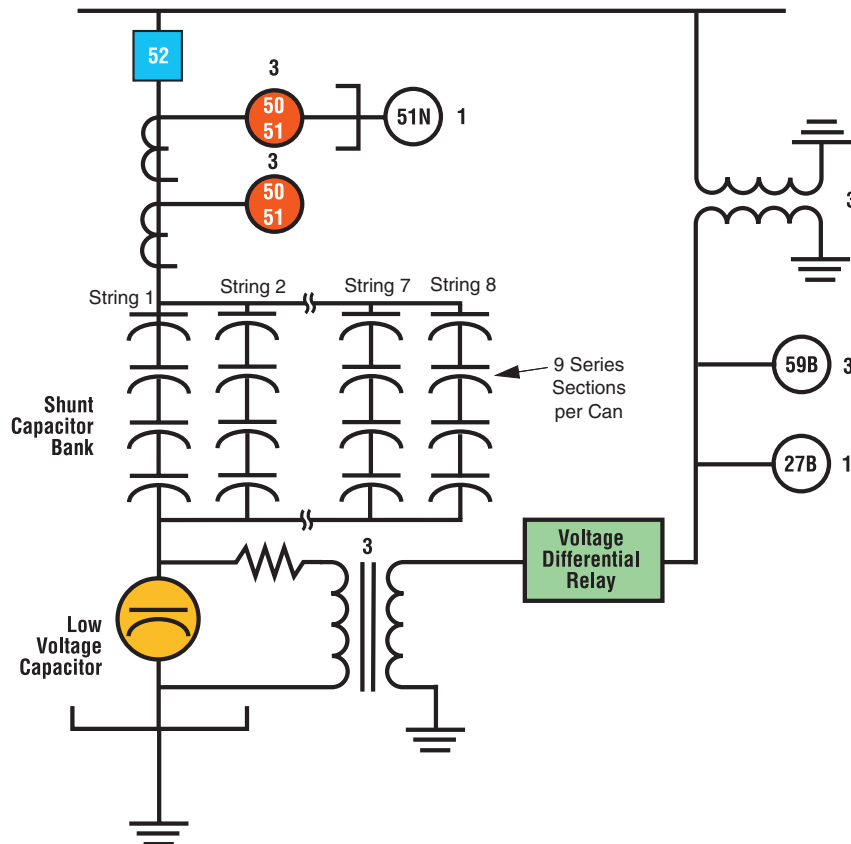


Figure 4.
Typical protection scheme for a fuseless grounded wye capacitor bank.

The normal phase current for the bank is approximately 251 A, and each string current is one-eighth of that: 31.4 A. Each string contains four capacitor units, and each unit has nine internal series connected packs. Thus, the effect of one shorted series section will lead to an increase of the string current to 32.3 A ($36/35 \times 31.4$ A).

But, the increase of 0.9 A in string current represents only a 0.36% increase of the phase current and leads to an increase in the differential voltage of only 0.36%. This small change is in the accuracy range of the instrument transformers and the relays and most likely will not provide satisfactory protection. For example, if there were changes in the applied burden to the bus voltage transformers, that causes changes in accuracy developing a differential voltage that may need to be nulled. This small change in phase current, as well in the differential voltage, masks the real threat to the bank when capacitor sections or units fail: elevated voltage stress upon the remaining sections. In the LES bank, a short-circuit failure of a single section increases the voltage across the remaining sections of that string by $36/35 - 1 = 2.9\%$. (Other string voltages are not affected.) Typically, the bank is tripped if sufficient sections fail to elevate the voltage of the remaining sections to 110% of nominal.

Another cause for concern is the variation of the capacitor divider due to differential temperatures (see Figure 5). The ambient temperature extremes for Nebraska (the location of the capacitor bank) range from -44°C to $+48^{\circ}\text{C}$, or a 92°C spread. Over a capacitor unit dielectric temperature range of 92°C , capacitance will change approximately 3.5%. The low voltage capacitors are typically mounted near the bottom of the capacitor bank with the main capacitors above and thus may be subject to different ambient heating and cooling and different thermal time constants. If the dielectric temperatures of the low voltage capacitors and the main capacitors do not track each other closely, a differential voltage will result which may give the indication of a shorted series section. Essentially, the problem is detecting one shorted series section among the 288 series sections in one phase.

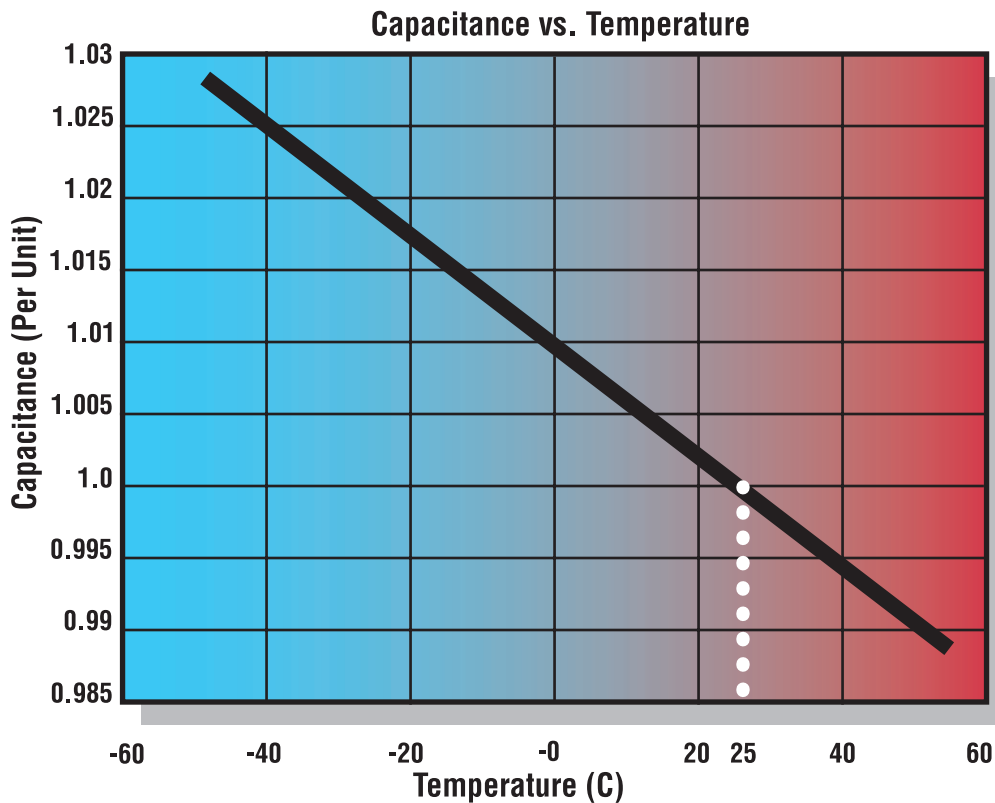


Figure 5.
Capacitance versus temperature.

Other Fuseless Capacitor Bank Protection Schemes Considered

One option considered was the double grounded-wye bank with protection provided by a voltage differential scheme. The voltage differential scheme compares the voltage across low voltage capacitor(s) in the neutral ends of each wye section of each capacitor bank phase.

Another option considered was the double grounded-wye with current differential with current transformers in the neutral end of each wye section of each capacitor bank phase.

Yet another option considered was to configure the bank as a grounded wye with a low voltage capacitor(s) placed at the neutral end of each capacitor bank phase to form an H-bridge. Relaying with a current transformer measuring the bridge current in each phase can determine which phase contains the faulty capacitor unit.

Concerns with Typical Fuseless Capacitor Bank Protection

Assuming that we could reliably alarm and trip from that small difference, our scheme would still be very incomplete. For example, we could have pack failures in different strings cause a trip condition, when this is an acceptable operating condition. Our scheme would not indicate the string(s) with the problem(s). Or, we could even have distributed failures that would have a canceling effect.

Impedance Method – Complete Protection

Given the limitations of conventional schemes, LES decided to use the impedance-based method of capacitor bank protection, incorporating a temperature transducer input as the best option for their needs. Impedance directly qualifies the value of interest for bank protection: the measure of capacitance, and its change in value, which may indicate failure of capacitor sections. This impedance measurement is immune to system unbalance and the self-canceling effects of distributed capacitor unit failures.

The impedance method utilized for fuseless capacitor banks measures the current in each string resulting in a high sensitivity of protection. A single shorted series section causes measured string impedance to decrease $36/35 - 1$ (or 2.9%) from 2164 Ω to 2104 Ω . Now, the problem is simplified to detecting a shorted series section among only the 36 series sections in each string of each phase.

The impedance method provides:

1. The ability of the bank to remain in service with multiple shorted series sections in various strings.
2. Identification of the phase(s) and string(s) with shorted series sections causing an alarm or trip condition.
3. Breaker failure protection.
4. Overvoltage, undervoltage, and overcurrent protection.
5. Expandability for ten-string protection with existing relays.
6. Expandability for twelve-string protection with an additional relay.
7. Flexibility for changes.

The impedance-based capacitor bank relays monitor the bus voltage and capacitor bank phase currents to determine the actual impedance of each string of each phase of the capacitor bank. Because the combined losses of buswork and modern all-film capacitor units are extremely low, it may be assumed that the impedance of the capacitor bank is purely negative reactive ($-jX_c$). This reactance may be determined from capacitor nameplate data and suffices as the initial, or nominal, impedance set point for commissioning. Figure 6 shows this nominal impedance in relation to the operating characteristic of the offset mho used by the relay. Capacitor bank relays, regardless of protection technique, should employ some ability to null out inherent error signals to improve setting accuracy and overall sensitivity. These inherent signals may arise due to manufacturers' tolerances in the capacitor units or slight phase or gain errors in the voltage or current transducers, as well as minor measurement errors of the relay. The impedance-based capacitor bank relay facilitates this necessary nulling by displaying the real-time measured string impedances. These values are used at commissioning to fine-tune the set point values from the approximate ones calculated from nameplate data.

The offset mho elements are inward looking. That is, the elements only operate when the capacitor impedance falls outside of a given mho circle. Temperature compensation of the impedance settings was also desired to provide more robust adaptive protection. Without temperature compensation to accommodate the wide variation in impedance that could occur due to temperature, the alarm and trip thresholds must be set at greater radii on the offset mho characteristic, essentially de-sensitizing protection. However, by being able to monitor the ambient temperature and actively adapt, the radii of the trip and alarm threshold remain at their sensitive values. The mho center and trip/alarm values now automatically shift in the $\pm jX_c$ direction in accordance with the temperature changes. For example, by examining Figure 5, cooler temperatures result in greater capacitance, i.e., less reactance. By measuring the lower temperature via the 4-20 mA output of a transducer, the relay shifts the critical setpoints toward the center of the impedance plane. The amount of shift is determined by the measured temperature and the coefficient entered by the user as a setting. Should the transduced input to the relay fail, internal circuitry and logic detect the abnormal condition, assert a Relay Alarm, and desensitize the trip and alarm radii by a factor of 2.

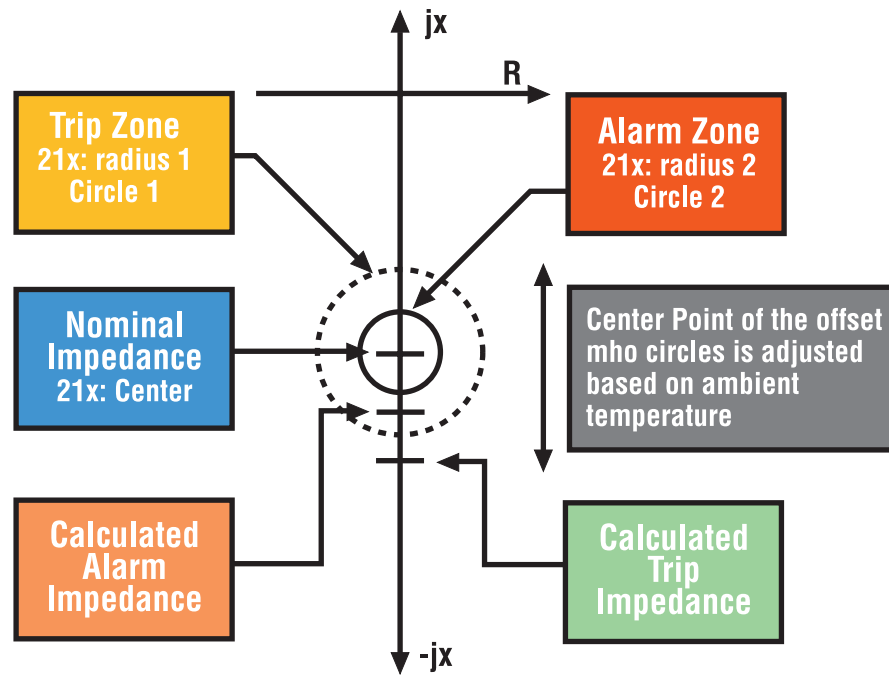


Figure 6.
Impedance-based capacitor bank protection.

Essentially, the sensitivity of the protection is such that a single shorted series section can be detected and an alarm issued. If the number of shorted series sections are large enough to cause an impedance range shift to the trip region, then the string which has a failure is identified. During the subsequent outage, if there are alarms indicated on other strings, preventive maintenance can be performed.

Figure 6 illustrates the concept of offset impedance circles of normal range, the alarm zone, the trip zone, and the temperature compensation which shifts the center of the impedance circle.

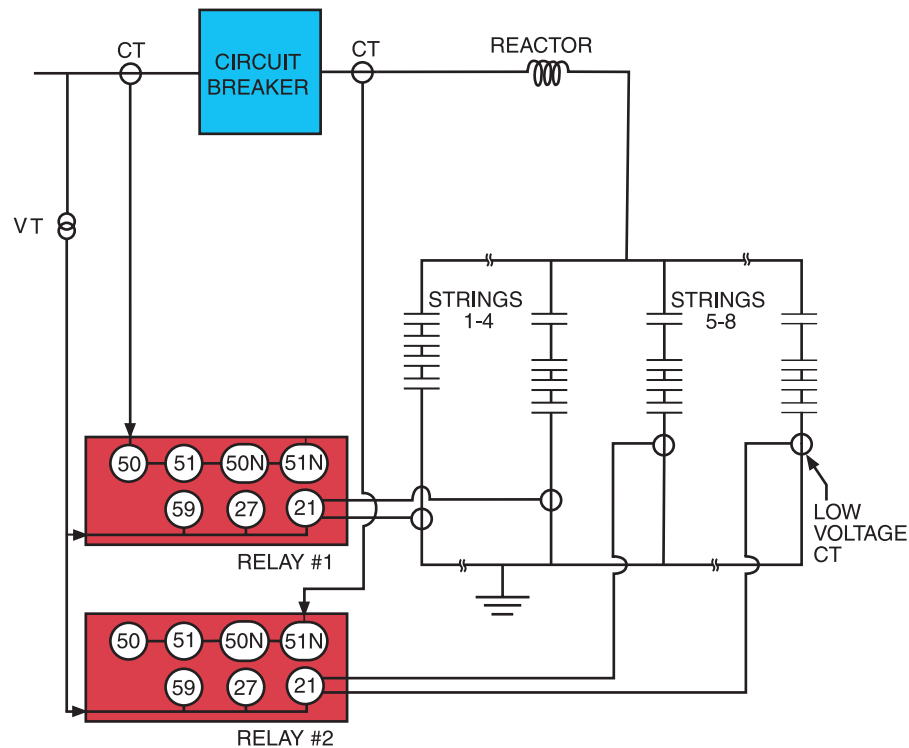


Figure 7.
Diagram of LES capacitor bank controls.

Application Details

Figure 7 illustrates the bank configuration and the protection scheme functionality. In the eight-string impedance scheme, 24 analog input channels are required to accommodate all the required per string current inputs. In addition, the bus voltages provide three analog voltage inputs and the backup phase and ground overcurrent elements require yet another three analog current inputs. This brings the total number of required analog inputs to 30. The large number of analog inputs require two relays running the same protection scheme. Each relay is capable of protecting up to five strings per phase. At present, each relay provides impedance protection to four strings and the overcurrent, overvoltage, undervoltage, and breaker failure protection functions. Note that separate breaker current transformers provide current inputs to each relay, and thus the protection has a healthy measure of redundancy. Future expansion to a ten-string bank can be accommodated within the two relays and an expansion to a twelve-string bank would require another identical relay.

Complete protection of the bank also includes backup overcurrent protection, tripping the bank on loss of voltage to avoid reclosing transients, block closing of the bank to allow for capacitor discharge, and breaker failure protection of the switching breaker. In addition, during large-scale system disturbances and islanding conditions, where islands of over and under frequency can exist, the impedance elements are blocked and only overcurrent protection is enabled. Thus, reactive power support is provided during system disturbances, when it is needed, which may help prevent cascading trips.

Future Enhancements:

1. Overcurrent on each string. The overcurrent protection could even be compensated by the bus voltage since it is already in the relay. This protection would be for catastrophic or growing faults that involve a large portion of the bank, such as a growing fault involving one or more strings in the bank.
2. Inclusion of automatic voltage and var control algorithms. This allows insertion or removal of the capacitor bank from the system.

References

1. *IEEE Guide for the Protection of Shunt Capacitor Banks*, IEEE C37.99-2000.
2. Martin Bishop, Tim Day, and Arvind Chaudhary, "A Primer on Capacitor Bank Protection," *IEEE Trans. on Industry Applications*, vol. 37, pp. 1174-1179, July/August 2001.
3. Malkiat S. Dhillon and Demetrios A. Tziouvaras, "Protection of Fuseless Capacitor Banks Using Digital Relays," presented at the Western Protective Relay Conference, Spokane, WA, October 1999.
4. Tom Ernst, "Fuseless Capacitor Bank Protection," 1999 Minnesota Power Systems Conference Proceedings.
5. Jack McCall, Tim Day, Shawkang Wu, and Tim Newton, "New Techniques for Capacitor Bank Protection and Control," presented at the Western Protective Relay Conference, Spokane, WA, October 1999.

Biographies

Leo Fendrick (S'71) received the B.S.E.E. degree from the University of Nebraska, Lincoln, in 1971. He is the Protection Engineering Supervisor, Lincoln Electric System. A member of IEEE, his previous experience includes various distribution and substation engineering responsibilities.

Tim Day (M88–SM'00) received the M.S.E.E. degree from Washington State University, Pullman, in 1991. He is a Senior Power Systems Engineer in the Systems Engineering Group, Cooper Power Systems, Franksville, WI. His present professional endeavors include modeling and analysis of electrical power systems in order to assess and optimize protection schemes. He enhances existing protective algorithms and develops customized schemes for the EdisonPro line of relays and incorporates Cooper Power Systems' simulator to verify all scheme modifications.

Karl Fender received the B.S.E.E. degree from the University of South Carolina. He is the Manager of Applications Engineering with McGraw-Edison Power Capacitors, Cooper Power Systems, Greenwood, SC. Fender joined Cooper Power Systems, after five years in the U.S. Navy, serving in both design engineering and marketing positions.

Arvind Chaudhary (S'85–M'85–SM'94) received the B.S.E.E. degree from the Indian Institute of Science, Bangalore, India, the M.S.E.E. degree from North Carolina State University, Raleigh, and the Ph.D. degree with a concentration in electric power engineering from Virginia Polytechnic Institute and State University, Blacksburg. He is a Staff Engineer with the Protective Relays and Integrated Systems Group, Cooper Power Systems, South Milwaukee, WI. He is responsible for relay applications for the Cooper line of relays and relay settings for power system equipment, including capacitor banks. He is the recipient of the 2000 IEEE PES Chicago Chapter Outstanding Engineer Award. His previous experience has included Sargent & Lundy consulting engineers (1991–1998) and Bharat Heavy Electricals Limited, India (1979–1983).