Advancements in Relay Current Sensor Technology

by

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Abstract:

With the digital relay's ability to measure quantities such as Voltage, Amperes, Watts, Vars, Power Quality data, etc., this measurement data is being used more and more as input to "distributed SCADA" functions formed around substation integration systems. As such, requirements for higher accuracy data in the metering range is beginning to show up in relay specifications. New technology in the current sensing and conversion arena is now available that can provide higher accuracy than traditional magnetic current transformers over a wide dynamic range (including both signal level and frequency). This paper present the theory and performance characteristics of one of these new current measurement systems.

Introduction

From the beginning of relay design, transformers were used on the inputs to provide surge protection, isolation, and scaling to the currents and voltages connected to the relay's measuring circuits. As designs moved from Electromechanical to static analog to digital, there have been only minor changes in the basic transformer design. In the case of the transformers used on the current circuit input, the application required performance from .1pu to 40pu without the necessity of high accuracy near the end points. Voltage signals, on the other hand, typically operate in a narrow range of ±20% of nominal and as such have never posed much of a problem in the normal operating range. Recently with the integration of digital relays into distributed SCADA systems there has been an expanded need to measure current over a larger dynamic range with greater accuracy. Data such as Volts, Amps, Watts, Vars, power factor, and harmonic distortion is being required as digital relays begin to supplant transducers as the source for this data.

Problem Statement

Current measurements in the range of .05 to 2 pu are now of concern. To be able to measure current accurately in this range as well as provide the dynamic range required for relaying is a challenge with present technology. The primary challenge lies in compensating for the magnitude and phase angle errors introduced by the magnetizing current of the isolation transformer. Figure 1 shows the equivalent circuit of a transformer. Given a 1:1 transformer with an input current, I_P, the output current, I_O, can be expressed as:

$$I_o = I_P - I_M \qquad (1)$$

where I_M is the magnetizing current. The error in the output current can be expressed as:

$$\%\ error = \frac{I_M}{I_o} * 100 \qquad (2)$$

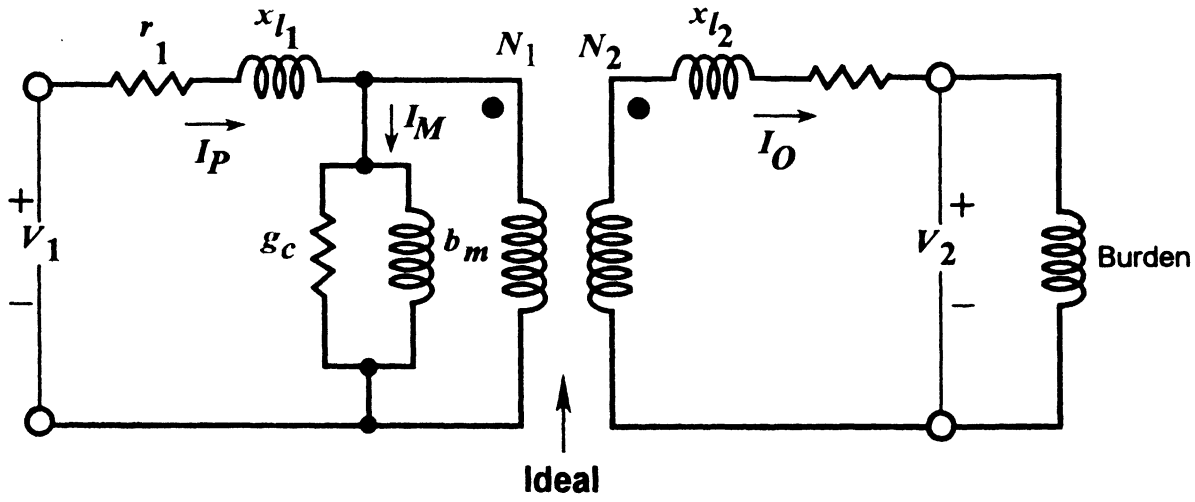

Figure 1
Transformer Equivalent Circuit

The primary variables in the magnitude of the measurement error are the size of the burden resistor and the leakage voltage drop resulting from the load through the transformer.

One clear path of improving the accuracy and dynamic range of current measurement is to minimize or "zero out" the flux required by the core of the transformer. As the magnetizing current is a function of the voltage across the magnetizing branch, minimizing this voltage would be a means of minimizing this current error.

Problem Solution - the "Zero Flux" CT

A very simple and elegant technique for creating a "zero flux" CT has been found and is realized as follows:

First, the input current is divided via a resistive current splitter as shown in figure 2. The divider is composed of copper and alloy resistors and placed in the configuration shown to minimize cross talk and mutual coupling. The alloy selected has an extremely low temperature coefficient of resistance and as such exhibits no measurable change in resistance over the temperature range of -40 to 70°C. By choosing values of R1 and R2 that are much greater than the resistance of copper, it can be shown that the ratio of the current through the middle resistor, R3, to the input current is very nearly:

$$\frac{I_3}{I_{IN}} = \frac{R_1 R_2}{R_1 R_2 + R_3(R_1 + R_2)} \qquad (3)$$

The resistive divider has been designed to operate continuously at 200A. At this level of input current, the divided current through the middle resistor is calibrated to 3A ±0.1% by shaving material off of either R1 or R2.

It is now desired to measure the scaled current flowing through R3. This is accomplished by placing a two winding torroidal magnetic core CT around this resistor. Each winding on the core is wrapped with 1500 turns of wire, enclosed in a Faraday shield, are then wrapped in insulation to provide isolation from external transients and surges.

The heart and elegance of the sensor design is the current comparator circuit shown in figure 3. The basic concept is to electronically provide the magnetizing flux for the current measuring torroid in the circuit. As mentioned earlier, one way to minimize the magnetizing flux is to drive the voltage on the magnetizing branch to zero. One winding, called the sense winding, is connected to an op-amp in a negative feedback configuration. The output of the op-amp is connected to the second winding of the torroid

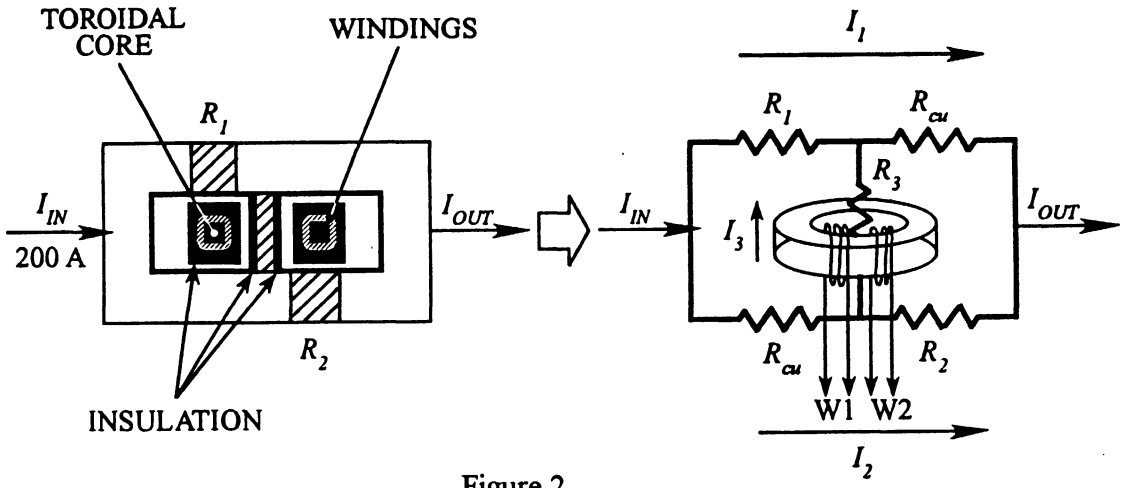

Figure 2
Zero Flux CT Construction

known as the forcing winding. In this configuration, the op-amp, in trying to zero out its inputs, will drive a current through its output terminal that will be equal (scaled by 1500 turns) and opposite to the primary input current. This current which is now proportional to the input primary current is passed through a dropping resistor resulting is an output voltage proportional to the input current.

One item of note with this circuit is that there is no DC feedback path in this circuit. As such, any offset voltage that may exist in the op-amp might force the outputs into saturation. To avoid this problem, a chopper stabilized op-amp is used in the feedback path. A chopper stabilized op-amp periodically switches the polarity of its input and output simultaneously. As a result, any DC offset in the op-amp is converted into an AC signal which is coupled back through the sensor into the sense input of the interface circuit and synchronously subtracted out.

Data Conversion

In most of today's digital relays, there is a conditioning process that an analog signal must go through on the way to being digitized. The first step is to scale the signal to a level that can be interfaced with low level analog circuits (described above). The second step in the traditional conversion process is to filter out all frequencies greater than 1/2 the sampling frequency (per Nyquist's theorem). This filter is known as an Anti Aliasing Filter (AAF) and can be designed either with passive or active components. In all cases, phase and magnitude performance of each filter is dependent on the accuracy of the components used and is diffucult to match channel to channel. Another factor in the accuracy equation is component drift over time - all capacitors lose value and resistors just wander.

Most relays today use only one A/D converter to perform all digitization. In order to sequence all the signals into the converter, a device known as a multiplexer is employed. The multiplexer, in response to an address input, selects one of the

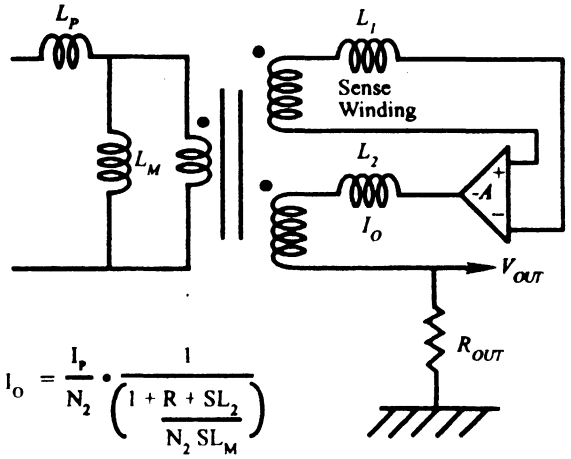

Figure 3
Current Comparator Circuit

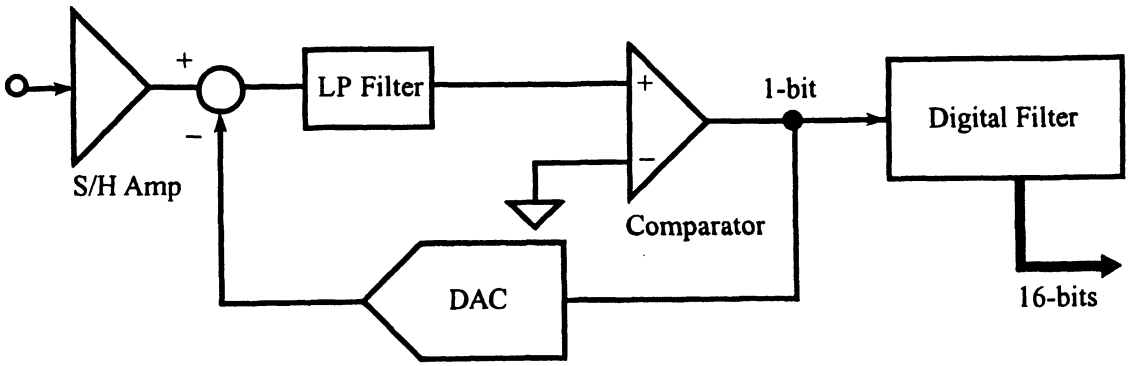

Figure 4
Delta-Sigma A/D Converter Block Diagram

signals to be input to the A/D converter. Depending on the speed of the A/D, each signal will have some time delay as to its relation with each other signal. This time delay is called skew. For example, if an A/D took 10usec to digitize an analog signal and it was converting a total of 9 signals, there would be a time skew of 80usec (1.73 electrical degrees at 60Hz) between the first and last signals. This can result in noticeable errors or realtime software overhead to adjust the sample times when calculating power, etc.

If more accuracy in the measurement is desired, a device know as a sample and hold (S/H) can be added in the signal path. Each S/H receives a "hold" command from a common source. Upon receipt of this command, the instantaneous voltage value present on the input of the S/H is held while each signal is converted by the A/D. Maintenance of the number of bits available is oftwn limited by the accuracy of the parts used at this stage. Once converted, the digitized values either need to be collected by the CPU or stored in local memory and transferred in mass to the CPU.

Delta-Sigma A/D Conversion

Advances in Application Specific Integrated Circuit (ASIC) design has brought commercial reality to a 20 year old A/D technology known as Delta-Sigma (Δ-σ) or "over sampling" A/D conversion. Use of this technology enables a radically different solution to the entire data conversion process described above. The following is a brief description of the Δ-σ conversation process.

Figure 4 shows a block diagram of a Δ-σ A/D converter. The diagram has two primary parts - a modulator circuit (the Delta part) and a digital decimation filter (the summing or Sigma part). The modulator is composed of a few simple components, namely, a summing junction, a low pass filter or integrator, a 1 bit A/D converter, and a 1 bit D/A converter in the negative feedback loop. The modulator operates at a very high sampling rate - typically in the multi-megahertz range from which the Δ-σ gets its other name as an "over-sampling A/D".

The basic operation of the Δ-σ modulator can be understood more intuitively by demonstration. Figure 5 shows a first order modulator (the order of the modulator denotes the order of analog filtering or integration in the loop). Full scale inputs in this example are $\pm$1V and the three test nodes are labeled V1, V2, and V3. The output of the comparator, V3, is the output of the loop and is also the input to the 1 bit D/A converter which converts the digit into a $\pm$ full scale ($\pm$1V) signal.

At the differential or summing amplifier, the +1V or -1V signal is subtracted from the analog input voltage. The output of the summer, V1, is input to the integrator. The integrator acts like an analog accumulator, that is, the voltage at V1 is added to the value stored the accumulator and becomes the new value at V2. The voltage at V2

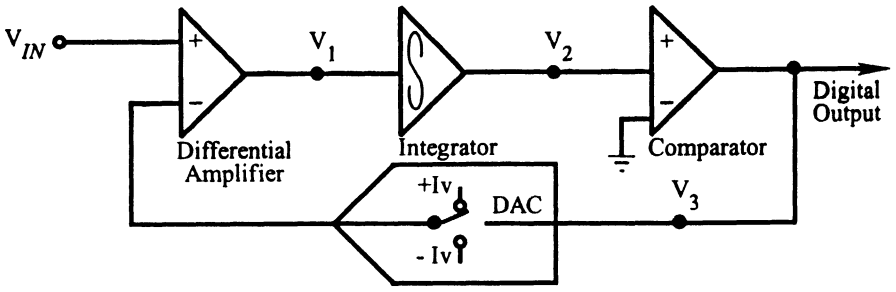

Figure 5
First Order Delta-Sigma Modulator

is then compared with ground. If V2 is greater than zero, the comparator outputs +1Volt (equal to a logical 1). If the value is less than zero, the comparator outputs -1Volt (equal to a logic 0). New values are computed each clock cycle.

In the "walk through" shown in Table 1, all nodes are initially set to zero and the analog input voltage is set at 0.6V. At each clock step, all values in the loop are updated. It is left to the reader as an exercise to step through a complete modulation. Note that for the constant input in this example, the pattern of node values will repeat as can be seen by comparing modulation steps two and seven. The value of the modulator outputs at node V3 over this period can be averaged and, as shown in the example, is equal to the input voltage of 0.6V.

This averaging can also be understood by looking at the output of the D/A converter as it sums with the input voltage. This sum is fed into an integrator. For the integrator to maintain stability, the average value of the voltage into it must equal zero, therefore, the average value of the output of the summing junction must be zero and subsequently, the average value of the voltage out of the D/A converter must be equal to the average value of the input signal.

Clock Period	V1	V2	V3	Period Average
0	0	0	0	
1	0.6	0.6	1	
2	-0.4	0.2	1	
3	-0.4	-0.2	-1	
4	1.6	1.4	1	0.6
5	-0.4	1.0	1	
6	-0.4	0.6	1	
7	-0.4	0.2	1	
8	-0.4	-0.2	-1	

Table 1
Delta-Sigma Modulator "Walk Though"

Another point of comparison to make is the fact that a first order Δ-σ operates like a voltage to frequency converter. In the conventional Voltage to Frequency based A/D converter, the output pulses from a Voltage Controlled Oscillator (VCO) are counted over a period of time. Similarly with the Δ-σ, the output train of pulses is effectively counted in an averaging procedure thus producing many partial sums.

The second half of the Δ-σ is a decimation filter. Since the converter samples at such a high rate, the bandwidth of the sampled data is very high. Typically, data is extracted from the Δ-σ at a much lower rate than the sampling rate, therefore, in order to focus the bandwidth in the area of interest, a digital low pass filter is used to further process the data. This process is know as decimation. One of the benefits of the Δ-σ technology is the ability to create any type of output filter in the digital domain. The most popular filter used to decimate the resultant sums is known as a Finite Impulse Response (FIR) filter.

Figure 6 shows the implementation of a 4th order FIR filter. The two basic operations are multiplication (X) and addition/accumulation (Σ). Filter coefficients a_0 to a_3 represent the impulse response of the function being implemented. The unit delays indicate that the output is calculated not only with the present sample but also with previous samples of data. The filter's input,

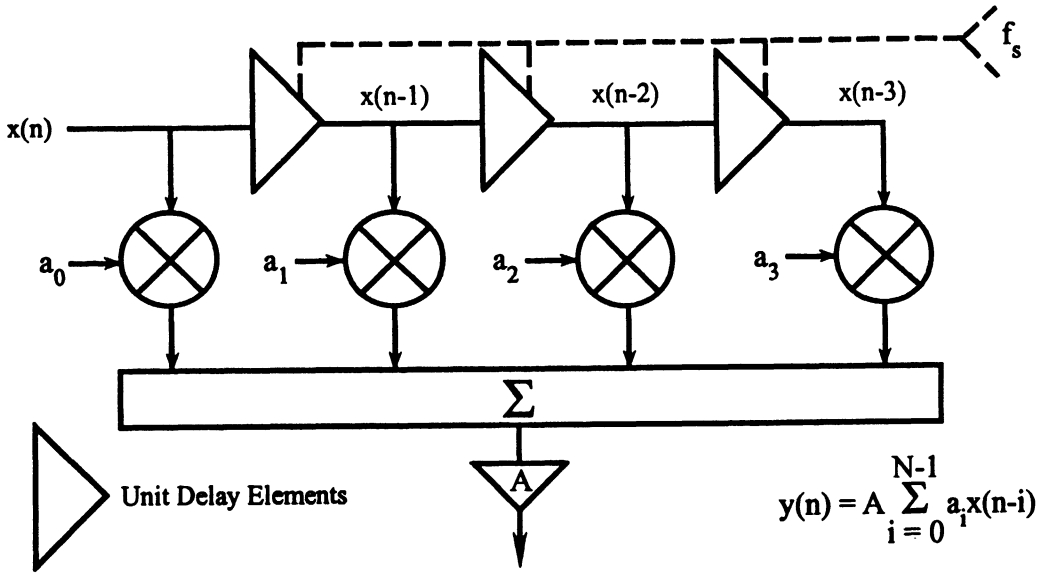

Figure 6
Finite Impulse Response (FIR) Filter Implementation

x(n), and output ,y(n), are digital words of any desired length. In the case of the 4th order filter shown here, each result requires 4 multiplications and resultant accumulation.

As mentioned earlier, different filter characteristics can be implemented by changing the coefficients of the FIR filter. The *ideal* low pass filter can be approximated by a function known as a $sinc^2$ function and has the frequency response shown in the lower half of figure 7. The impulse response of the $sinc^2$ function is triangular in shape as shown in the top half of figure 7. As such, the coefficients used in the FIR count from 1 to the decimation filter over-sampling rate and back down to 1. A decimation filter can be designed to compute two concurrent sets of triangular decimations (as depicted by the two sets of triangles shown in the upper half of figure 7) and subsequently generate data at a rate equal to the over-sampling ratio/f_m - the modulator output rate. Many designs allow data to be extracted at different rates with different accuracies.

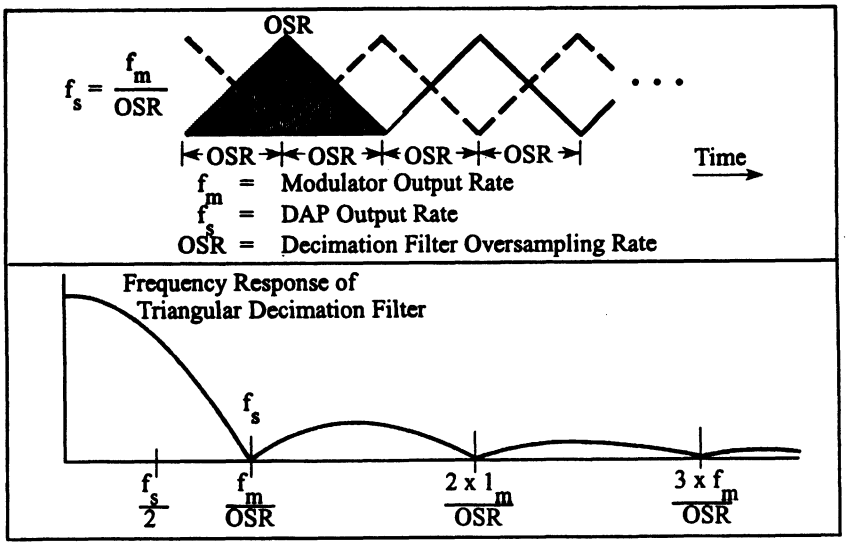

Figure 7
Top: Decimation Coefficients for a $Sinc^2$ Filter *Bottom*: Frequency Response of the $Sinc^2$ Filter

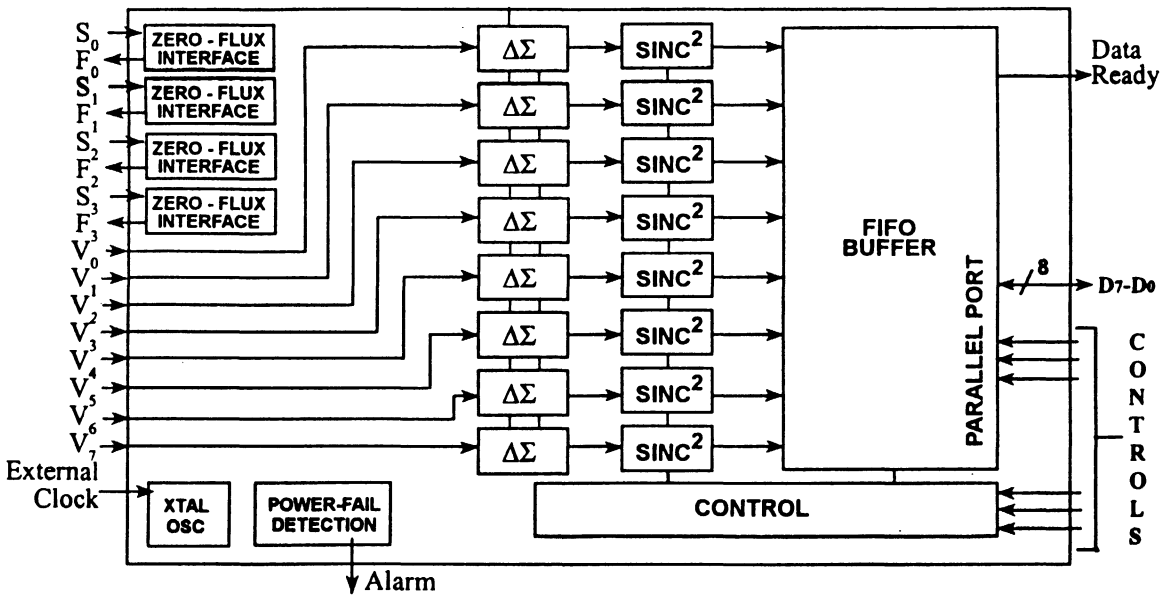

Figure 8
ASIC Based - 8 Channel Delta-Sigma A/D Conveter

Due to the simplicity of the Δ-σ design, it is possible to incorporate many converters on one silicon base. By taking advantage of ASIC integration capabilities, all converters can be operated synchronously and all results can be stored in an on board buffer. Figure 8 shows an architecture where 8 A/Ds are combined onto one chip. Up-front design of the interface control lines will permit tight coupling of the converter with Digital Signal Processors (DSPs) to further refine the data.

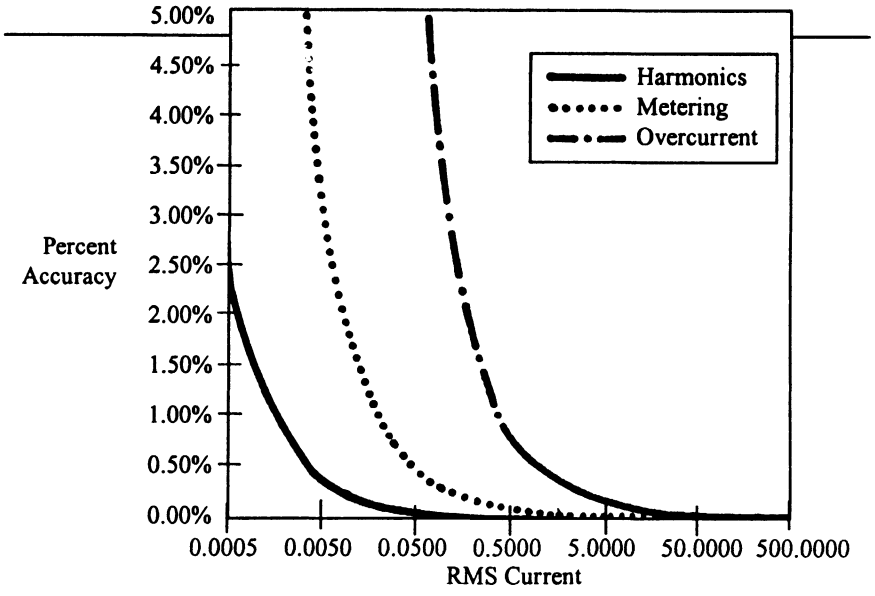

Figure 9
System Accuracy as a percent of eading

There are a number of key benefits from the use of Δ-σ converter technology, namely:

- The high rate of sampling on the input minimizes or eliminates the need for external anti-aliasing filtering
- Digital filtering provides shaping options not available with analog filters
- Multiple channels of conversion can be imbedded on one chip and sampled synchronously thereby eliminating the need for sample and hold circuitry

System Performance Results

The combination of a zero-flux current sensor and a Δ-σ was assembled and tested for accuracy over 3 ranges of interest. In particular, tests were run in a harmonic measurement range (peak current .5A), a metering range (peak current of 15A), and a relay range (peak current of 315A). Measurements were made in all test ranges and accuracy was computed as a percent of *reading*. The results of these test is shown in figure 9. Note that by overlapping the measurement ranges, better that 0.5% accuracy can be achieved over a dynamic range of 50ma to 300A.

Conclusions

The evolving use Intelligent Electronic Devices for data acquisition in the substation has created tighter requirements for analog measurement accuracy. New current sensing technology based on zero-flux current sensors combined with enhanced A/D converter technology can provide superior measurement performance over a wide dynamic range.

For Further Reading

"Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation", by J.ames C. Candy and Gabor C. Temes, IEEE Press, ISBN 0-87942-285-8.

Biographies

Mark Adamiak received his Bachelor of Science and Master of Engineering degrees from Cornell University in Electrical Engineering in 1975 and 1976 respectively and his Master of Science degree in 1983 from the Polytechnic Institute of New York. From 1976 through 1990, Mark worked for the American Electric Power Service Corporation (AEP) in the System Protection and Control section where his assignments included R&D in Digital Protection and Control, relay and fault analysis, and system responsibility for Power Line Carrier and Fault Recorders. In 1990, Mark joined General Electric's Power Management business in Malvern, Pennsylvania as Manager of Advanced Technology Programs. He is presently responsible for Substation Integration systems and for developing and evaluating new technology applicable to the protection, control, and monitoring community. In 1986, Mark was the winner of the Eta Kappa Nu (HKN) society's "Outstanding Young Electrical Engineer" award. Mark is a member of HKN, a Senior Member of IEEE, Vice Chairman of the IEEE Relay Communication Sub Committee, and the US representative to IEC TC57 - Working Group 11 on Substation Communication.

Rikk Wolfs graduated from the Georgia Institute of Technology with a Bachelors degree in Electrical Engineering in 1977, and subsequently received his Masters degree in Electrical Engineering from Villanova in 1990. Rikk successfully completed the Navy Nuclear Power training program in 1978, and spent the next seven years as an officer in the Submarine Force, attaining the rank of Lieutenant Commander. In 1985 Rikk joined GE's Aerospace Business Group, where he worked in various roles in the development of several satellite programs, the last of which was as the Program Manager for attitude control subsystems for commercial satellites. In 1995, Rikk joined the Power Management Department of GE, where he assumed the role of Project Leader for the Digital Feeder Protection 200 (DFP200) program concurrently with responsibility for all new product introduction. Rikk is a member of ETA Kappa Nu (HKN).