COORDINATION OF MICROPROCESSOR-BASED LINE RELAYS WITH ELECTROMECHANICAL RELAYS

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ABSTRACT

When bussing an existing line equipped with electromechanical line relays, the application of microprocessor-based line relays at the new terminals can create an interface problem. Due to the inherently different operating speeds of these two types of relays, a coordination problem can exist between their pilot protection elements. One suggested method to solve this problem was to modify the electromechanical relay scheme so that proper coordination could be achieved. Another method is to relocate an electromechanical system from one end to match the existing electromechanical system at the other. Florida Power and Light Company (FPL) was searching for a microprocessor-based line relay that would coordinate directly with the existing electromechanical line relays without making any relay panel modifications or relocations. A microprocessor-based line relay, with a special blocking scheme developed to coordinate with electromechanical line relays, was tested back-to-back in its special blocking mode with two types of existing electromechanical line relay panels and found to satisfy FPL's requirements.

INTRODUCTION

This paper covers the evaluation and selection of a microprocessor-based line relay for non-critical lines in the Florida Power and Light (FPL) system. Per FPL's protection philosophy, the non-critical lines are provided with primary pilot protection and step-distance backup protection. For non-critical 230 kV lines this protection is packaged on two 28-inch wide panels. The packaging for non-critical 138 kV and 115 kV lines is done on one 28-inch wide panel. FPL was looking for a single 19-inch wide panel package for application on voltage levels of 230 kV and below, as a cost reduction measure. This could be accomplished by using microprocessor-based line relays. However, special problems existed when applying microprocessor-based line relays in the existing system with electromechanical relays.

While bussing an existing line and applying electromechanical relays, interfacing with the existing electromechanical relays generally does not present any coordination problem. However, the application of a microprocessor-based line relay interfacing

with an electromechanical relay (see figure 1) presents a problem associated with communication coordination between their pilot protection elements.

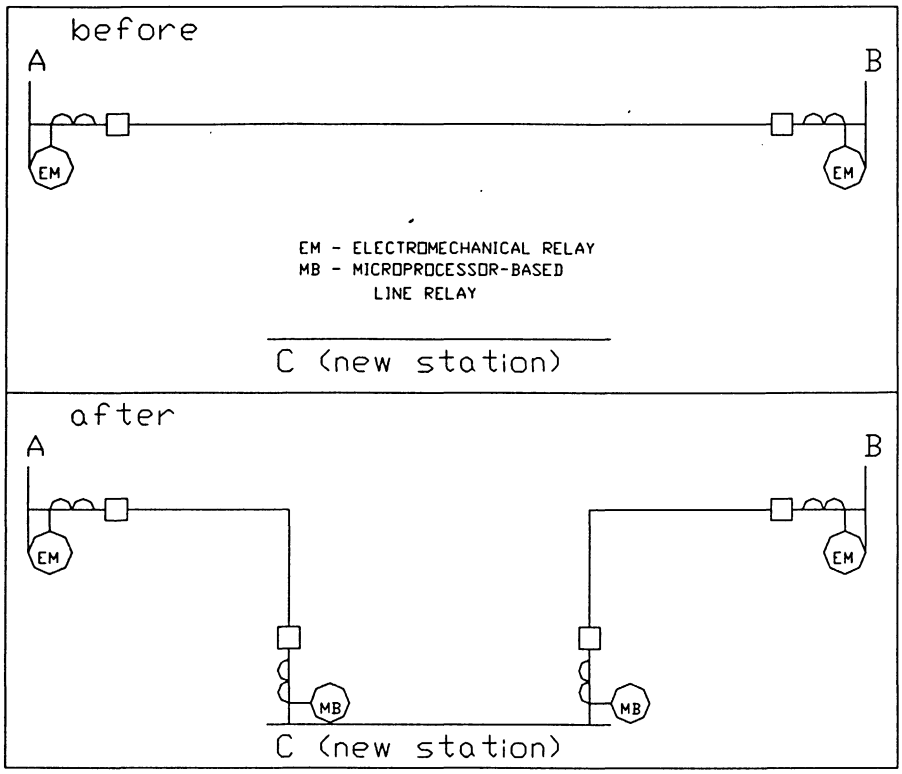

FIGURE 1. BUSSING AN EXISTING LINE

This problem arises due to the difference in the operating speeds of the electromechanical and microprocessor-based line relays. One suggested way to solve this problem was to modify the existing electromechanical relay scheme to coordinate with the microprocessor-based line relays. FPL's desire not to modify the existing line protection panels led to a search for a microprocessor-based line relay that would coordinate directly with the existing electromechanical relay without requiring relay panel modifications. As a result, a microprocessor-based line relay with a special blocking scheme was tested against two types of existing electromechanical line relays. Back-to-back tests were conducted separately between electromechanical line panels containing mho and reactance distance elements against this microprocessor-based line relay.

DESCRIPTION OF PROBLEM

For directional comparison blocking schemes, internal faults will be cleared by the tripping elements at both terminals and no coordination is required. The main concern when applying a directional comparison blocking scheme is security against external

faults. This requires coordination between the tripping elements at one end versus the blocking elements at the other end.

When coordinating electromechanical relays against microprocessor-based line relays in a blocking scheme, coordination problems are expected because of their differences in operating speed. The microprocessor-based line relay's operating time is fairly independent of fault current magnitude (more specifically, fault location and source impedance). An electromechanical relay is an energy device that will operate fast for high fault currents, but will operate slow for low fault currents. The two most common problems are summarized below:

STRONG SOURCE BEHIND ELECTROMECHANICAL RELAY

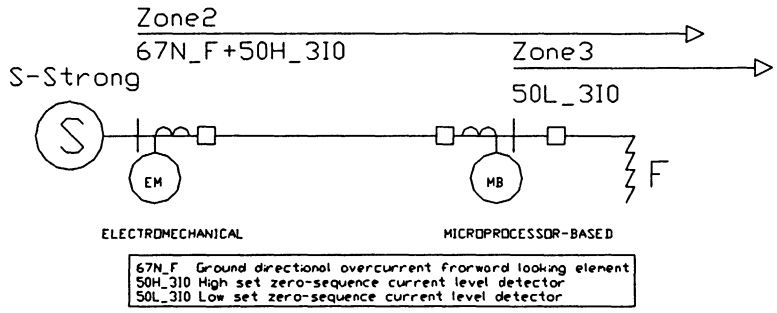

FIGURE 2. STRONG SOURCE

For an external fault at location F, heavy fault current will flow through the line due to the strong source behind the electromechanical relay, such as the case for a short line. As a result, the electromechanical relay may operate faster than the microprocessor-based line relay. During these high levels of fault current the electromechanical relay's forward looking tripping elements may operate faster than the microprocessor-based line relay's reverse looking blocking elements. For the fault at location F the operation of the electromechanical relay's tripping elements plus its coordination time delay may be less than the operate time of the blocking elements at the remote end plus the communication channel time. If this condition occurs then the electromechanical relay may trip its end of the line prior to receipt of the microprocessor-based line relay's blocking signal. Some measure is needed to block this type of overtrip.

WEAK SOURCE BEHIND MICROPROCESSOR-BASED LINE RELAY

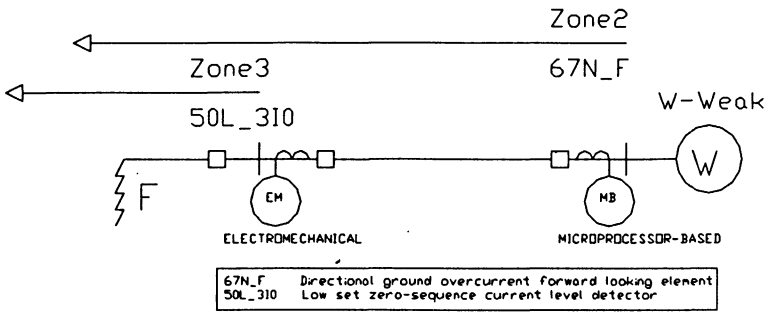

FIGURE 3. WEAK SOURCE

For an external fault at location F, low fault current will flow through the transmission line due to the weak source behind the microprocessor-based line relay, such as the case for a long line. As a result, the electromechanical relay will be slow to operate. The operate time of the microprocessor-based line relay's tripping elements may be faster than the electromechanical relay's blocking elements plus the communication channel time. To prevent the microprocessor-based line relay from overtripping, its coordination time delay must be properly set to account for this condition.

PROPOSED SOLUTION WITH SPECIAL BLOCKING SCHEME

This microprocessor-based scheme was developed to allow faster operating times when coordinating with electromechanical relays at the remote end while still maintaining security. Fast fault clearing in this directional comparison blocking scheme is achieved when the microprocessor-based line relay's phase and ground distance protection is supplemented with directional ground overcurrent protection. Both phase and ground protection schemes share a common communication channel.

SIMPLIFIED SCHEME LOGIC

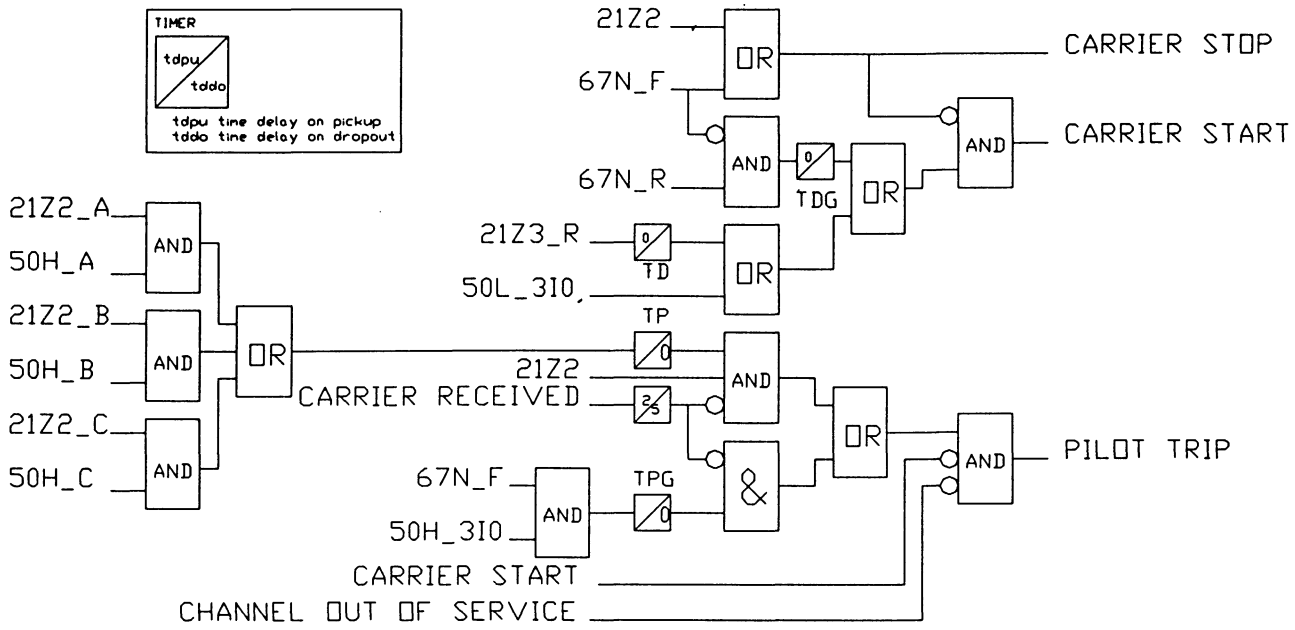

FIGURE 4. SPECIAL BLOCKING LOGIC

Element	Description
67N_F	Directional ground overcurrent forward looking element
67N_R	Directional ground overcurrent reverse looking element
21Z2	Zone2 element operated
21Z2_A	Zone2 element involving phase "A" operated: A-G, A-B, C-A
21Z2_B	Zone2 element involving phase "B" operated: B-G, A-B, B-C
21Z2_C	Zone2 element involving phase "C" operated: C-G, B-C, C-A
21Z3_R	Reverse-looking Zone3 element operated
50H_A	High set phase "A" current level detector
50H_B	High set phase "B" current level detector
50H_C	High set phase "C" current level detector
50H_3I0	High set zero-sequence current level detector
50L_3I0	Low set zero-sequence current level detector

Timer	Description
TP/TPG	Time delay on pickup, phase and ground respectively
TD/TDG	Time delay on dropout, phase and ground respectively

MICROPROCESSOR-BASED SCHEME LOGIC DESCRIPTION

Refer to Figure 4. To address the problem encountered during external faults driven by a strong source the following has been implemented. The reverse-looking zone3 elements (21Z3_R) or the non-directional low set zero-sequence current level detector (50L_3I0) starts carrier to send a fast blocking signal to the remote end for external faults. The non-directional low set zero-sequence current level detector (50L_3I0) can be set very sensitive for ground faults. When an external ground fault occurs this non-directional element is able to send the blocking signal very quickly. If

either a zone2 element (21Z2) or the ground directional overcurrent forward looking element (67N_F) operates then this will stop the blocking signal.

For phase faults the microprocessor-based line relay's zone3 elements (21Z3_R) should be set as the reverse-looking characteristic. The method of synchronous polarization for this type of operating characteristic consistently produces faster operating times than the self-polarized offset mho characteristic. The reverse-looking zone3 elements are able to quickly send a blocking signal for external phase faults.

To address the problem encountered during an external fault driven by a weak source the following has been implemented. The zone2 elements (21Z2) and the directional ground overcurrent forward looking element (67N_F) supervised by a non-directional high set zero-sequence current level detector (50H_3I0) are responsible for tripping the circuit breaker(s) during an internal fault. Tripping is delayed for times TP and TPG, for phase and ground faults respectively, to ensure that the blocking signal from the remote end is received during external faults.

The segregated zone2 elements (21Z2_A, 21Z2_B, 21Z2_C) are supervised by their corresponding high set phase current level detectors (50H_A, 50H_B, 50H_C). These are needed for low level external faults to ensure that the forward looking zone2 elements of the microprocessor-based line relay will not operate for fault current beneath the electromechanical relay's reverse looking zone3 elements operating requirements. This prevents overtripping of the microprocessor-based line relay when the fault current is too small to operate the electromechanical relay.

To prevent false operation during 'holes' in the blocking signal, created by the contact bounce of an electromechanical relay, a 2 millisecond time delay on pickup/5 millisecond time delay on dropout timer has been included in the signal receive logic.

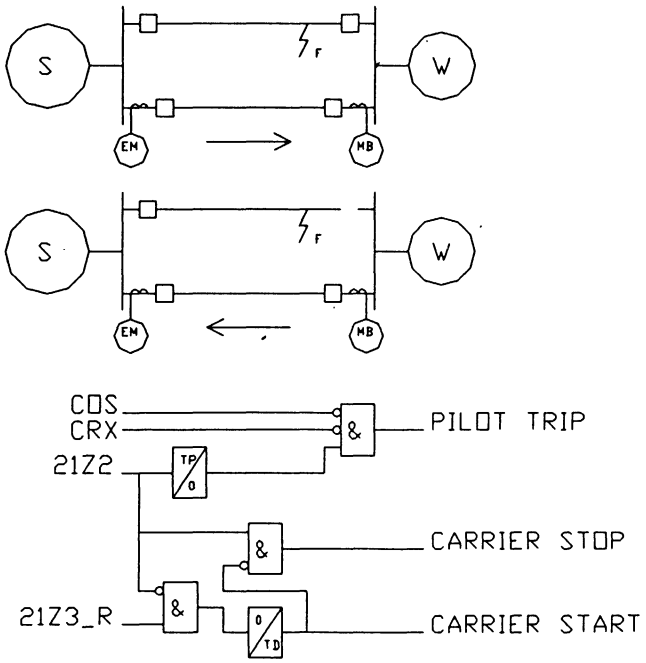

FIGURE 5. SIMPLIFIED CURRENT REVERSAL LOGIC

Refer to figure 5. Current reversals occur on parallel lines when the source at one end is significantly stronger than the other. When a close-in fault occurs on one of the lines, current flows through the other line from the strong source towards the weak source. If the fault is cleared first at the closer terminal then the current in the healthy line will reverse in direction since there is no longer a path to fault in the previous direction. This can cause coordination problems on the parallel line.

Time delays on drop-out, TD and TDG, for phase and ground faults respectively, ensure that the blocking signal is maintained long enough to prevent inadvertent tripping of a healthy line during the sequential clearing of a fault on a parallel line during a current reversal.

The TD time delay on dropout timer prevents overtripping of the electromechanical relay during current reversals on parallel lines. This time delay prevents a race between the dropout of the electromechanical relay's zone2 element and the microprocessor-based line relay's reverse-looking zone3 element. The time delay on dropout timer extends the blocking signal from the microprocessor-based line relay after the fault current reverses to prevent overtripping at the electromechanical end. The current reversal logic for the ground protection is similar.

TEST CONDITIONS

FPL supplied the following two electromechanical line relay panels along with their PLC transmitters/receivers.

Panel 1 — For 138 kV short line - reactance distance elements for phase fault protection and directional overcurrent elements for ground fault protection

Panel 2 — For 230 kV long line - mho distance elements for phase fault protection and directional overcurrent elements for ground fault protection

These panels were tested separately for pilot protection coordination with the microprocessor-based line relay. The relay settings used for these panels were selected for two existing lines in the FPL system. The lines selected have parallel lines. This was done to facilitate testing of the desired current reversal scenarios.

Referring to figure 6, combinations of the following fault types and conditions generated the entire range of simulations for the test cases:

Fault types
- single line-to-ground
- line-to-line
- double line-to-ground
- three phase

Internal and external faults

Current reversals for faults on parallel lines

Strong and weak sources

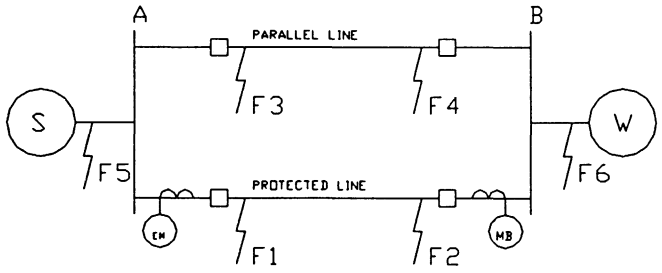

FIGURE 6. TYPICAL SHORT CIRCUIT MODEL WITH FAULT LOCATIONS SHOWN

TEST SET UP

Test equipment was used to implement a double-ended simulation with 12 sources, i.e. 6 voltages and 6 currents as shown in figure 7. Two current amplifiers were available to simulate close-in high current line-to-line and double line-to-ground faults.

An attenuator was inserted in the communication path between the two carrier sets to simulate the actual losses in a power line carrier system.

Two separate DOS based PC software programs were used as described below:

The first package was used to model both sets of parallel lines so that prefault and fault signals at both terminals could be generated and recorded for each simulation test case. The second package was used to playback synchronized prefault and fault signals through the test equipment to the two terminals for both line protection schemes.

A digital fault recorder was used to capture the analog waveforms presented to the relays and also to record the status of their output contacts for each and every simulation test case.

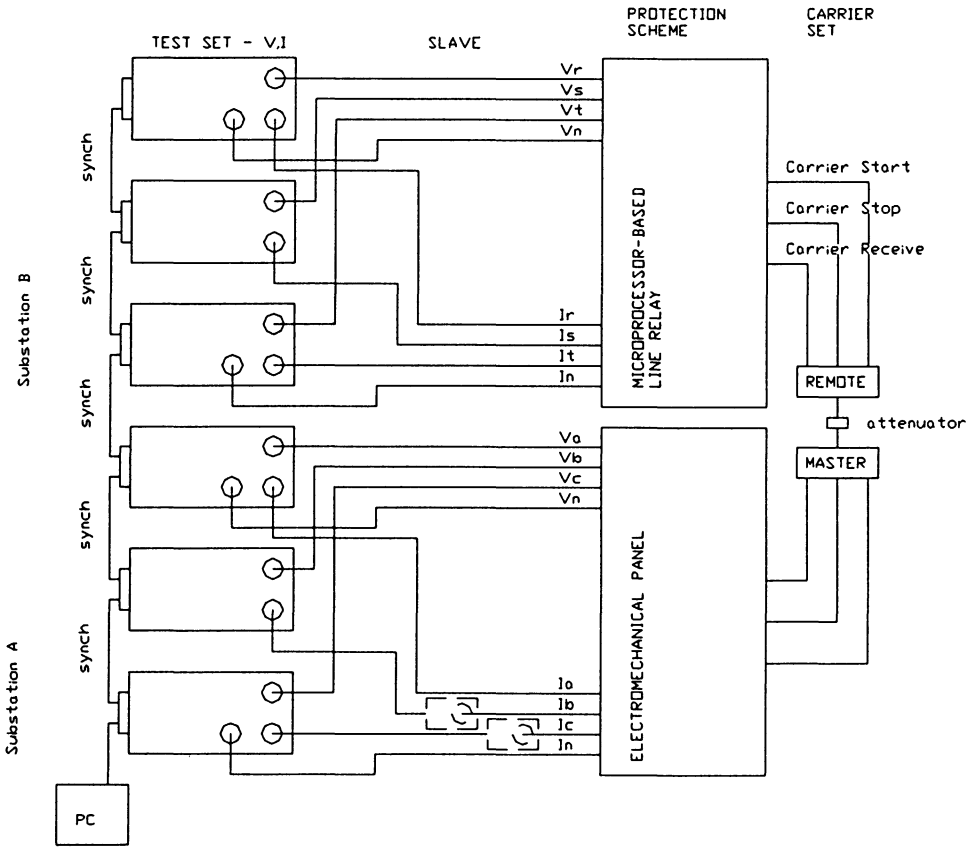

FIGURE 7. TEST SET UP

RESULTS

The microprocessor-based line relay's distance elements were faster than the electromechanical relay for the majority of the test cases. For the rest of the cases, no misoperations occurred due to the special blocking scheme.

The microprocessor-based line relay's reverse-looking zone3 elements were able to send the blocking signal quickly for all external phase faults so that overtripping did not occur for the electromechanical relay.

The typical time required for both ends to close their trip contacts was approximately 2.5 cycles.

The optimal timer settings confirmed from the tests are as follows:

TP = 10ms + maximum channel operating time

TPG = 0ms, simplex communication channel (transmit and receive on same frequency)

TD = 14ms + maximum channel operating time - minimum channel reset time

TDG = 14ms + maximum channel operating time - minimum channel reset time

where

maximum channel operate time = maximum time for the receiving relay to pickup once the other relay has sent the blocking signal

minimum channel reset time = minimum time required for the blocking signal to dropout at the receiving relay once the transmitting relay has stopped sending

CONCLUSIONS

The special blocking scheme provided high speed clearing of all internal faults and was secure for all external faults and current reversals. No modifications were necessary for either of the electromechanical panels provided by FPL. As a result of this testing, FPL has a single design standard for non-critical lines that substitutes for several existing design standards based on long or short lines, and, ground directional overcurrent or ground distance schemes.

ACKNOWLEDGMENTS

The authors would like to extend their thanks to M. L. Davidson, R. T. Ross, B. R. Webster and M. E. Lacedonia of Florida Power & Light and David Keeling, Sam Sambasivan, Biren Gosalia, and Otis Brooks of GEC Alsthom Inc. for their contributions in the development of this task.

BIOGRAPHIES

Madan Gaudi, P.E., received his B.S.E.E. from Thapar College Of Engineering, India and his M.S.E.E., from University Of Miami. He is also a graduate of the Westinghouse Advanced Power Systems School. He is the Lead T & D protection engineer in Florida Power & Light's Protection & Control Engineering section. He has worked thirteen (13) years at FPL; ten (10) years in Power Supply Technical Services and the last three (3) in Protection & Control.

Steve Turner attended Virginia Polytechnic Institute and State University from September 1980 to 1986 to complete his B.S.E.E. As an undergraduate he participated in the cooperative education program with Virginia Power. After graduation he started employment with the Naval Facilities Engineering Command, Atlantic Division as a power systems analysis engineer. In the beginning of 1989 he moved to Kansas City, Kansas to work with Black and Veatch Engineering Transmission and Distribution Division as a protection engineer. Then in August 1989 he returned to Blacksburg, Virginia to begin his M.S.E.E. at Virginia Tech. He spent the summer of 1990 as an intern with American Electric Power Service Corporation's System Protection Department during completion of his master's degree. After graduation he was hired by GEC ALSTHOM T&D INC.'s Protection and Control Division as an applications engineer.