A REAL TIME DIGITAL TNA FOR RELAY TESTING.

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ABSTRACT.

This paper describes the design and performance of a real time digital transient network analyser (DTNA) for testing relays. The DTNA uses a parallel processing architecture to run power system simulations in real time with a time step of 50-100μs. Relays are supplied with the appropriate signals from the DTNA and the output from the relay trip circuit is fed back into the simulation. Examples are given of tests on a commercial distance relay.

INTRODUCTION.

Analogue TNA's of considerable complexity have allowed high speed relays to be tested in an interactive mode with the relay trip signal being fed into the simulation. [1], [2]. Such analogue TNA's are expensive and occupy considerable space and as a result tend to be confined to manufacturers and some of the larger utilities. The technique of playing off-line EMTP simulations at relays via conditioning amplifiers has made it possible for smaller Utilities and academic researchers to test existing and prototype relays in a non-interactive mode (relay operation not fed back into the simulation). Such techniques allow the primary system to be represented in considerable detail but the duration of output waveform they can produce is limited by storage capability to typically 0.5s. The length of test waveform can be increased by piecing together several consecutive runs [3], [4]. The sequence controller which joins the runs together can also allow a certain degree of interaction between the relay and the simulation if it can choose from a library of runs representing different relay trip times and current interruptions. To build such a library requires a multitude of runs even for a single system and only makes sense if certain benchmark systems can be defined. Unfortunately many of today's relaying problems are unique to the Utility concerned and the benchmark solution although helpful is not sufficiently precise to remove all reasonable doubt about the relay performance in the specific application under study. In addition the combination of computers and sequence controllers required is relatively expensive.

If the digital solution can be made to run in real time then the storage limitation problem is overcome. The waveforms can be passed directly to the relay under test via conditioning amplifiers and the relay operation can be fed back into the process to influence the post fault solution. The process then becomes very similar to the analogue TNA technique. Until recently it has not been possible to run real time electromagnetic transient solutions on a digital processor with a time step small enough for relay fault studies. One might have expected that as supercomputers become ever faster it would become possible to run an electromagnetic transient solution in real time on such a computer. However even if this were to be possible the structure of a mainframe will not allow access to the necessary variables during the solution process. This led researchers at the Manitoba HVDC Research Centre to seek an alternative solution based on parallel processing techniques and state of the art digital signal processors (DSP) [5]. As will be appreciated from the following section the solution

they found is a digital simulator with supercomputer performance.

Their original goal was to replace the large scale analogue simulators used to model HVDC converters and systems but in the process of achieving that goal the hardware evolved is also suitable for simulating ac systems of sufficient complexity for testing relays. The versatility of the hardware allows it to be used to test controllers for HVDC systems [5], relays for ac systems and in the future will be of great assistance in testing interactions between dc system controllers and relays in the contiguous ac systems. Such ac systems very often contain series compensation and relaying series compensated lines is one of todays major concerns.

One of the major problems with large analogue simulators is the difficulty of correctly interconnecting the various elements. Anybody who has had to hand "patch" an analogue simulator for even a small sytem will know how simple it is to make connection errors. This problem has been overcome in the DTNA by using an input graphics package on the control workstation. This same graphics package (DRAFT) has been developed for use in off-line simulations [5], [7] and the user is given an option to select either a compiler to run an off line simulation or the DTNA. The DTNA compiler allocates tasks to various processors and makes sure that the interconnections are consistent with the circuit diagram assembled in the DRAFT routine.

This paper briefly describes the simulator hardware, how a case is entered using the DRAFT graphics package running under X Windows and a selection of relay test results.

SIMULATOR HARDWARE.

Whereas an analogue TNA uses scaled down models of system elements, a DTNA models these same elements by solving the mathematical equations which describe the element behaviour. Because the DTNA processors run algorithms which solve equations the component they repesent can be changed simply by altering the algorithm.

A typical electromagnetic transient study requires a time step of around 50μs. A system such as that shown in Figure 4 would require hundreds of millions of floating point operations per second (MFLOPS) to solve all the necessary equations at least once in a single time step. The most powerful computer workstations available today can run at only a few MFLOPS on an intermittent basis. It is clear that a special purpose device is required which uses parallel processing techniques running on processing elements capable of very high speed floating point arithmetic.

The DTNA is made up of several standard 19" racks. Each rack contains 18 processing element cards (PE's), one inter-rack communication card (IRC) and one workstation interface card (WIC) [8]. The first system used for the relay tests, Figure 4, required two such racks. Any one rack can communicate with only four other racks but this is not a significant restriction due to the natural sparsity of power systems. Since there are only three types of card, and programmable VLSI devices are used to construct the cards, the cost of the DTNA is much less than for an analogue simulator of similar capability. In addition the same card may be used to run code representing a synchronous machine in one study [6] or a transmission line in another study. This is a versatility which an analogue simulator cannot match.

Each PE card is equipped with a processor capable of up to 13 MFLOPS. It also has hardware to allow interfacing to external signals. Two analogue channels can be selected to monitor variables being computed on that card and these channels can be scaled on-line to suit the external device. (The signals to drive the conditioning amplifiers feeding the relay were obtained from these channels.) There is also a circular buffer with 6144 data locations which can be used to capture a designated part of the variables for subsequent display or processing on the host workstation. An input channel can also accept a logic signal such as the closing of the test relay contacts.

The IRC transfers data generated on its rack to other connected racks which need this information for the next time step. Transfer of information takes place at 500 Mhz.

The WIC deals with the communication between the DTNA and the host computer network over an ethernet communication link. The data transfer rate is 10 Mhz. The WIC also performs on-line diagnostics to ensure each PE is operating correctly.

Figure 1 shows the layout of the arrangement for testing a relay. The workstation which controls the case entry, download to the simulator, case run and data collection from the simulator during the run is on the far left. The first cubicle on the left contains relays under test, the second contains an HVDC controller not being used in these tests and the third cubicle contains the 4 racks of the present DTNA. Just beyond the third cubicle can be seen part of the cubicles containing the conditioning amplifiers. The latter are by far the largest elements of the test set up.

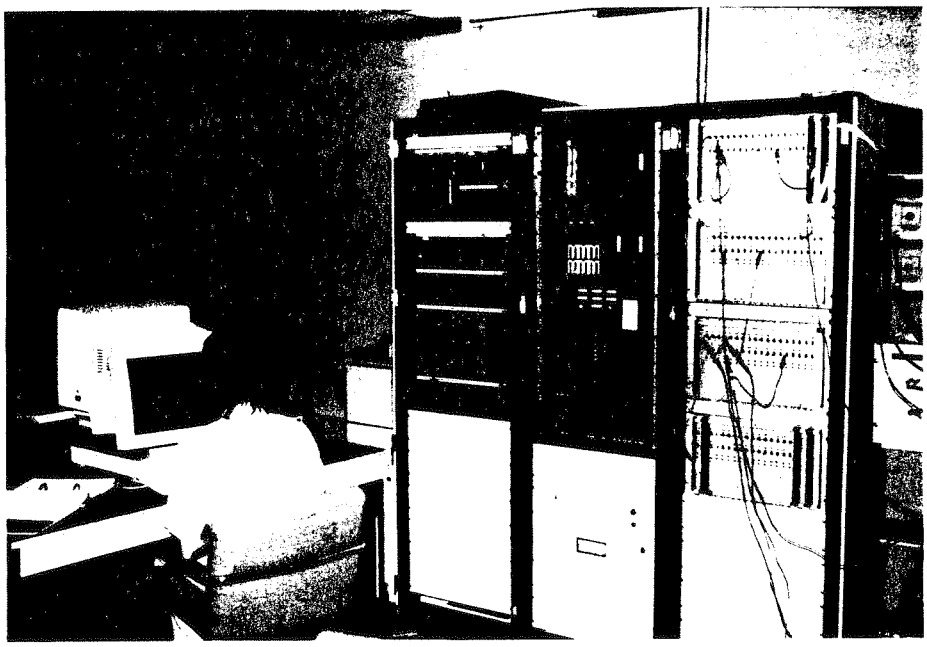

Figure 1. General view of relay test set up.

SIMULATOR SOFTWARE

If the relay engineer is to be able to use the DTNA it must be simple to set up and interface to the relay. Considerable effort had already gone into the development of a graphical front end for the Manitoba Hydro electromagnetic transients simulation package (EMTDC) and the DTNA makes use of this same package known as DRAFT [7]. The DRAFT menu offers the user a choice between running the case on EMTDC (off-line) or the DTNA. Otherwise the process of entering system data is identical.

The user interface to the DTNA is via the host workstation shown on the left of Figure 1. Various high level software routines are available to set up, run and analyse a case. In the setting up of a typical case the DRAFT screen is divided into a right 'menu' or component selection area containing Icons representing all of the system elements which have been coded for the real time simulator, and an area on the left where the system is being assembled. Figure 2 is a "screen dump" taken during this process. With the aid of a mouse any desired component can be selected and dragged into the left area to be connected at the desired

location. There are many more Icons available than are shown on the screen and again the

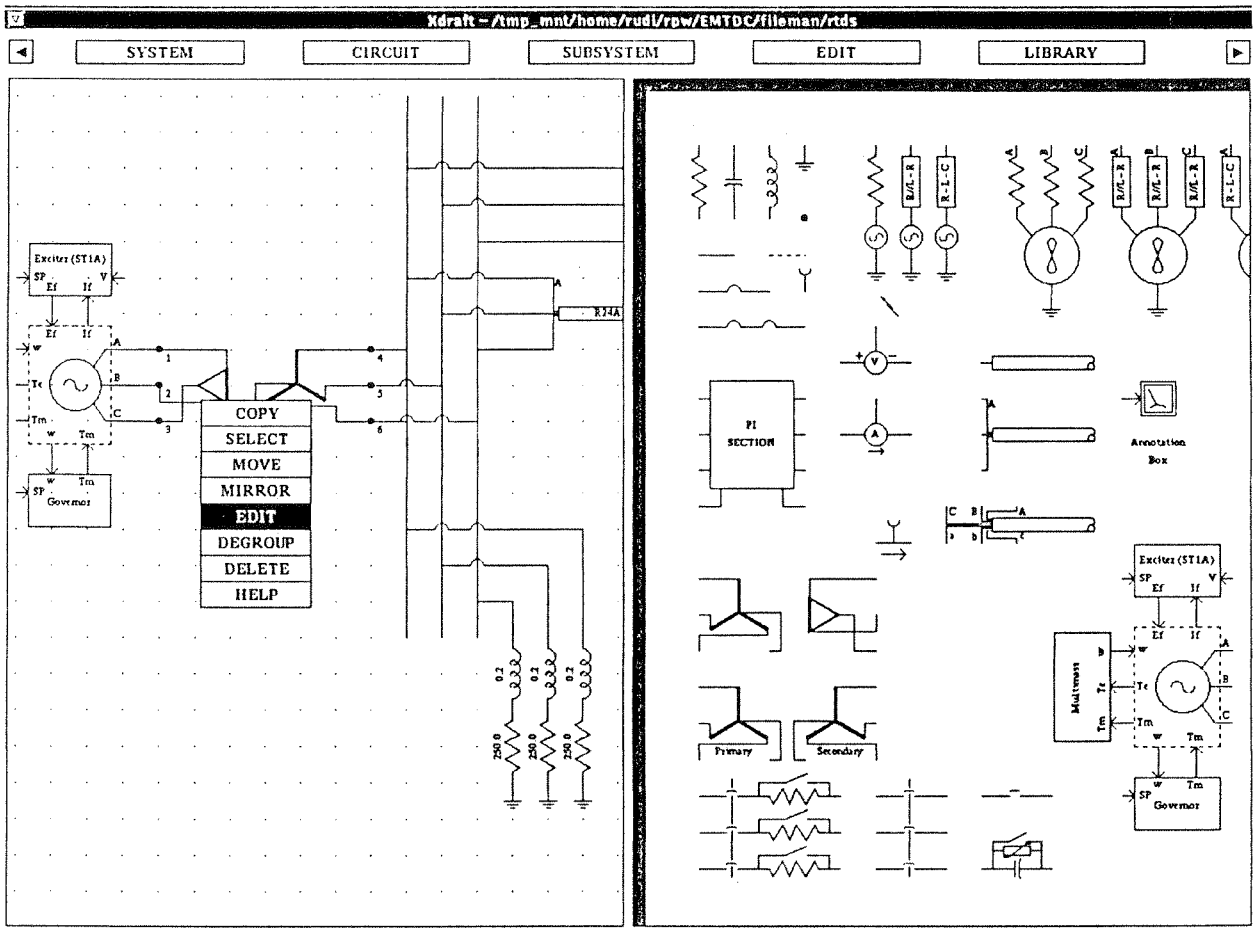

Figure 2. The DRAFT screen during data entry.

complete menu can be examined by using the mouse in the right hand window to scroll up and down, left and right. When a particular Icon is incorporated in the circuit diagram the user is prompted on the screen to supply the necessary data for the item in question. Figure 3 shows the response of the DRAFT screen to the edit box selected in Figure 2 and details of the transformer are now entered in the appropriate boxes. Although only a portion of the entire circuit is visible on the screen in Figure 2 one can move around the whole circuit by scrolling with the mouse.

Once the circuit diagram is complete the information is translated into a data file for use by the compiler. The compiler combines this information with information derived from another input program describing the system dynamics eg timing and type of fault, prefault load flow etc, and produces the code which must be executed by the PE and IRC cards on each rack. The code run by the processors on these cards has been hand assembled to represent the various elements in a power system. The sets of instructions are stored on the host workstation and are accessed by the compiler as required. The user of the DTNA need never be exposed to this low level software.

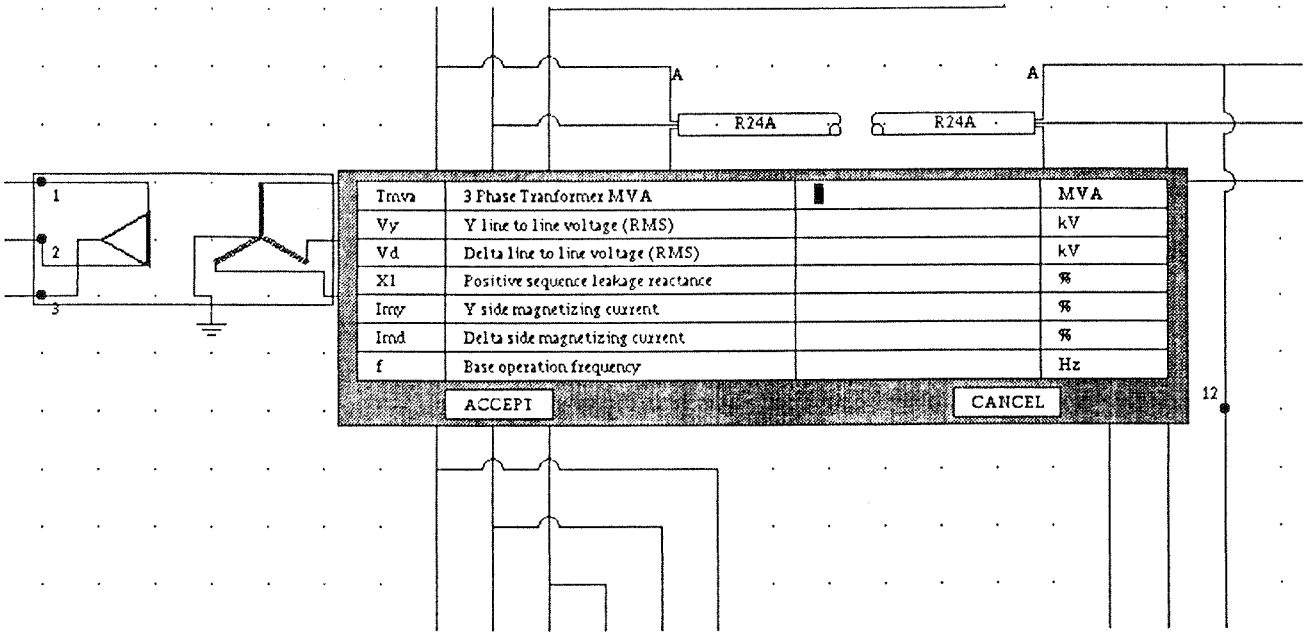

Figure 3. The "edit" screen in response to the request in Figure 2.

The compiler uses diakoptic techniques to separate the power system model into decoupled blocks which can be executed on the available DTNA racks. It performs the software equivalent of "patching" in an analogue computer and indicates to the user which card has been allocated which model. This allows the user to identify where he should connect say a particular conditioning amplifier or an oscilloscope to observe a particular variable behaviour. The only connections which the user must make are from the simulator to the conditioning amplifiers, the relay trip contacts to the card running the breaker model and any recording apparatus on to appropriate monitoring points on the simulator or relay.

Data capture from the simulator backplane is also part of the data entry procedure. Addresses for the desired waveforms must be specified before the run so that the data points are stored for use by the post fault processing software.

RESULTS.

Once the steady state is established and the user is satisfied that the conditioning amplifiers have been switched on, recording apparatus trigger primed etc. the fault is initiated from the keyboard and will be applied at the next occurrence of the preset point on wave. In the series of tests to be described the breaker operation is triggered by the closing of the test relay contacts. The breaker model has a pre-insertion resistor which comes in at the first current zero after the relay trip and current interruption takes place at the following current zero. The first test system has no power system stabilizer and the power swings continue for some time after any reclose operation. This allows the relay to be tested under power swing conditions.

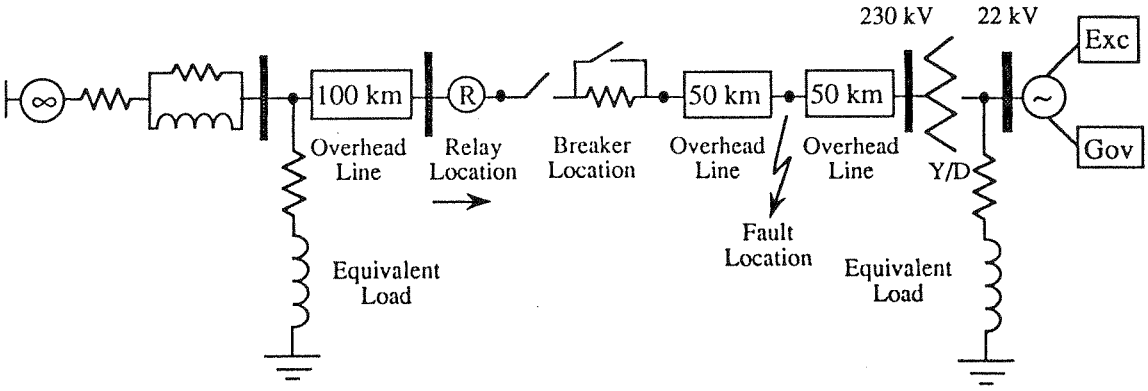

Figure 4. First test system.

The test relay is a 3 zone distance relay employing an analogue phase comparator. Figure 4 shows the first system simulated which required 2 racks to run the simulation. The machine is a turbine alternator set with governor and AVR. The protected line is 100km long and the zone 1 setting was chosen to be $27/\underline{85}^0$ primary ohms corresponding to 80km. Zone 2 was set at 150% of zone 1 and zone 3 at 150% of zone 2 in the forward direction and 25% of zone 1 in the reverse direction. All three zones have circular mho characteristics.

The scaling of output variables had to ensure that the conditioning amplifiers could handle the levels. The present current amplifiers have a bandwidth of 0 to 10kHz but can only reach 40A rms and the fault currents were therefore kept below this level. Each voltage amplifier is capable of producing up to 235V rms, 0.625A from dc to 100kHz.

The following figures show waveforms recorded on a digital storage oscilloscope and subsequently downloaded to an X-Y plotter. Only a few of the test waveforms are shown to illustrate the capability of the DTNA. Figure 5 shows the alternator $\Delta\omega$ signal and the phase "a" current for a 100ms reclose interval on a L-G fault. Figure 6 shows the voltage and current variables at the relay location for a three phase short circuit at 50 kms along the protected line. The two cursors indicate the fault initiation and the relay trip signal which in this case are 22.4ms apart.

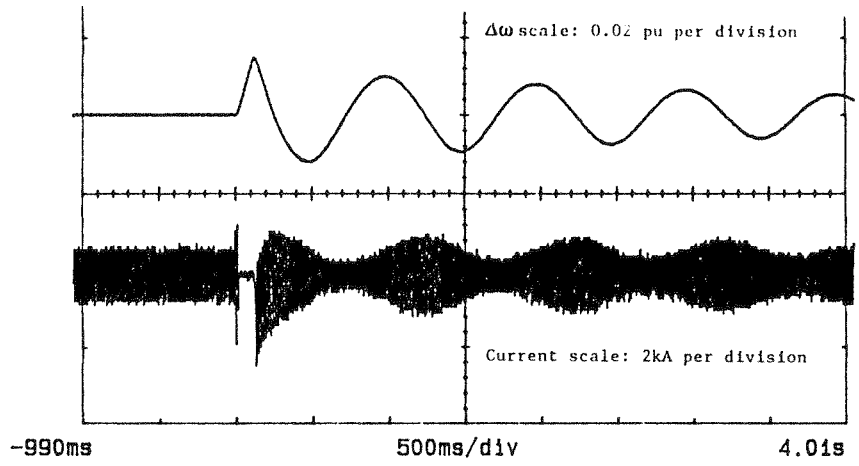

Figure 5. Faulted phase current and $\Delta\omega$ for 100ms reclose interval.

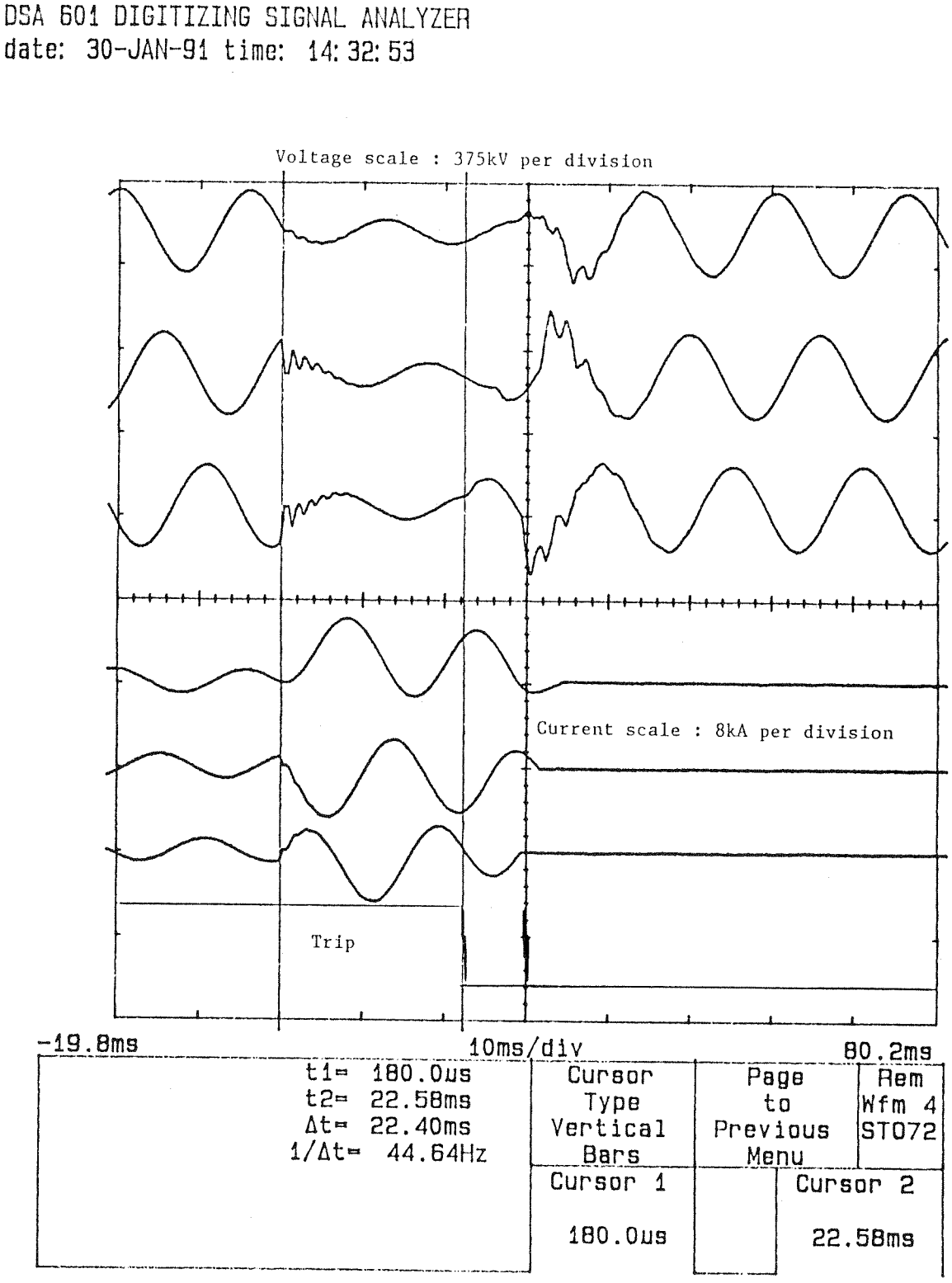

Figure 6. Relay voltages, current and trip output for a three phase fault

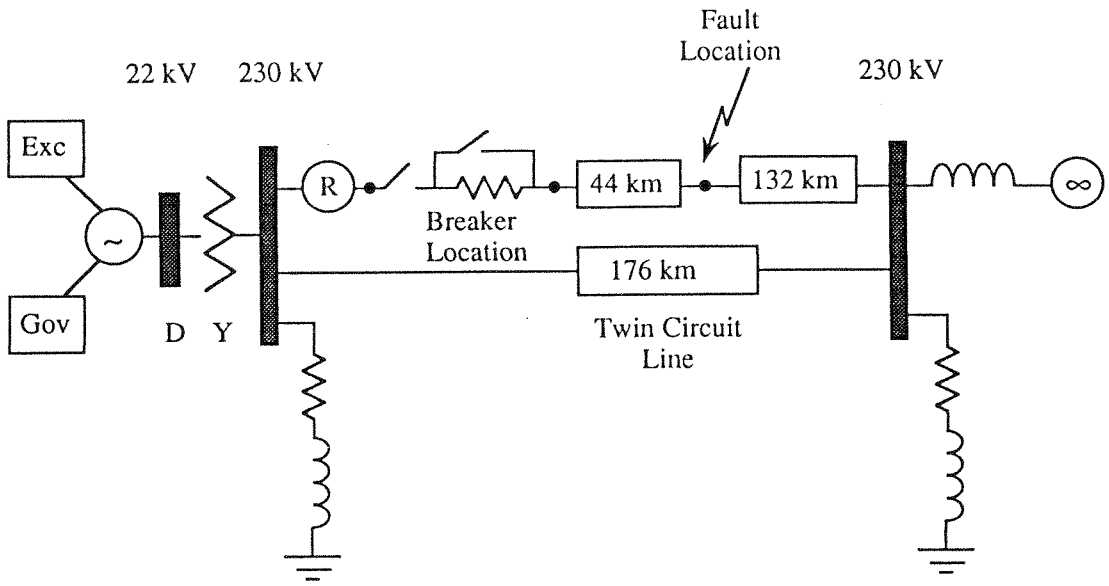

Figure 7. Second test system.

Figure 7 shows the second system simulated. It is a double circuit line and the fault location is as shown. This system also required 2 racks to run the simulation. The relay settings were altered to give a zone 1 setting of 85.32/86.4° primary ohms, (100% of line length), and a zone 2 setting of 150% of line length. Figure 8 shows the result for a L-L inter-circuit fault (phase a of one circuit to phase b of the other circuit). The inter circuit fault was not picked up by the ab element in any zone and the "a" phase element operated in zone 2 after 44.6ms (the zone 2 delay was set at zero). Figure 9 shows the result for a L-G fault with the generator $\Delta\omega$ signal shown to a different time scale. The power swing in this case is much less than in the previous test system because of the parallel path maintaining power transfer capability.

The third system used for testing a relay is shown in Figure 10. It is the 500kV system linking the converter station at Dorsey just north of Winnipeg to the Forbes and Chisago stations in Minnesota. The series compensation shown will be brought into service in 1993. The purpose of this set of tests was to determine if the existing relays can be set to protect the line when the series compensation is introduced. This system required all four of the existing racks to run the simulation.

In order to test the existing relays the simulator and conditioning amplifiers were taken to the Dorsey converter station. One of the two relays at Dorsey protecting the northern section of the line was withdrawn from service and subjected to test waveforms from the simulator. Figure 11 shows the relay waveforms for a three phase fault at the Forbes busbar. The relay zone 1 reach must be set so that it does not reach beyond the Forbes busbar and with a setting of 90 primary ohms the relay did not operate despite the significant subharmonic visible on the waveforms. (Total uncompensated line impedance of 188Ω.) Figure 12 shows waveforms for a three phase fault to ground at the south end of the northern capacitor bank (T2B). The fault level causes significant MOV conduction and causes the protective gap to be triggerred in just over a cycle as can be seen in Figure 13. Zone 1 operated in 24.7ms.

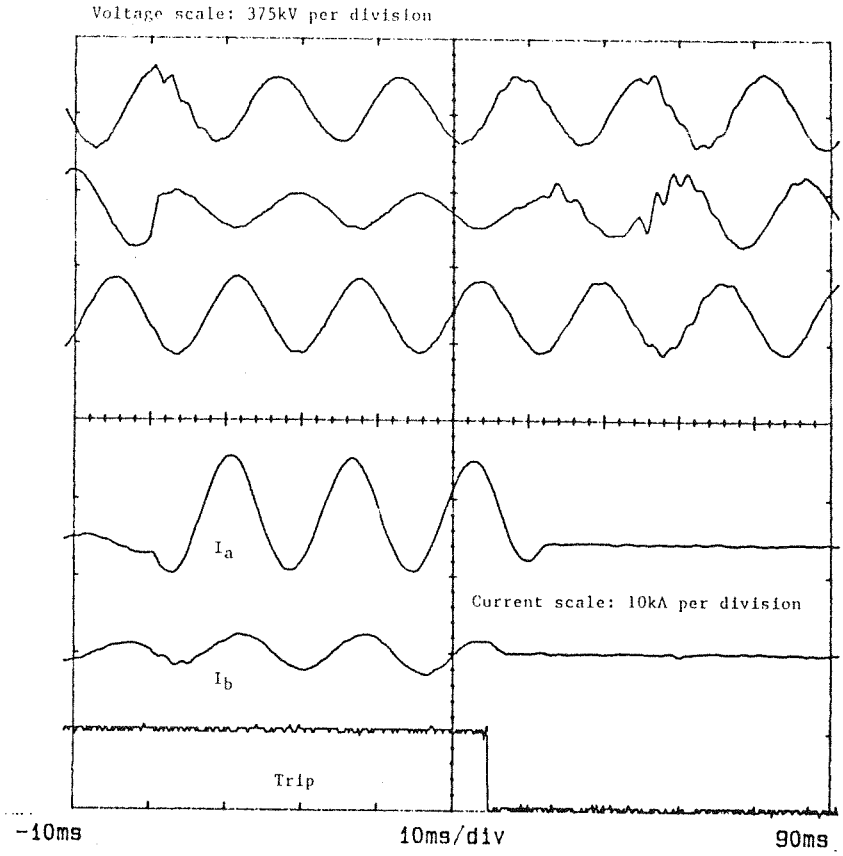

Figure 8. Relay voltages and current for an inter-circuit fault.

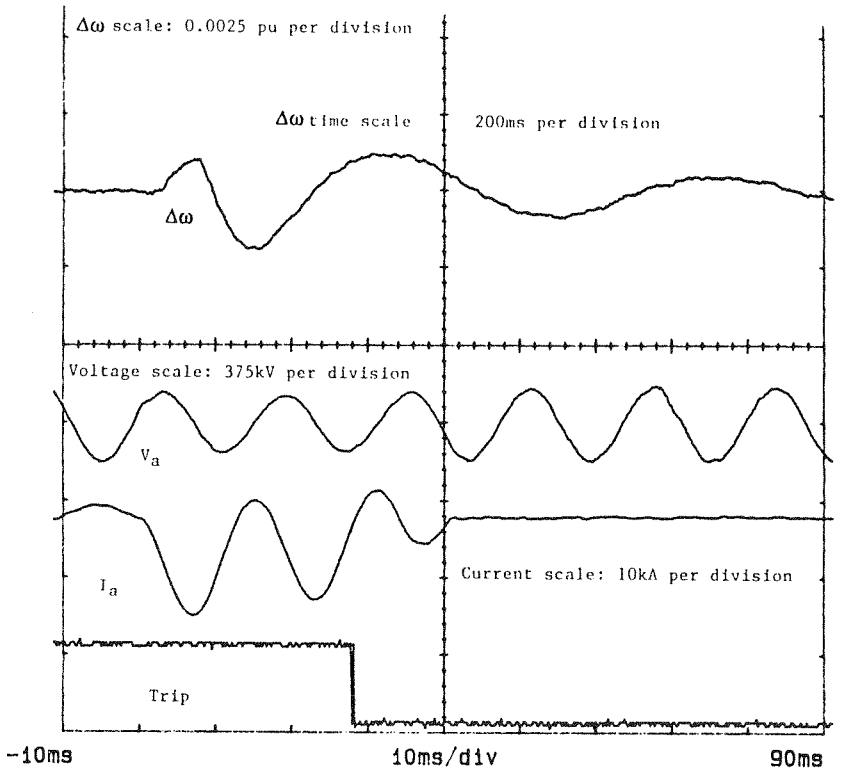

Figure 9. Faulted phase current and voltage and $\Delta\omega$ for a L-G fault.

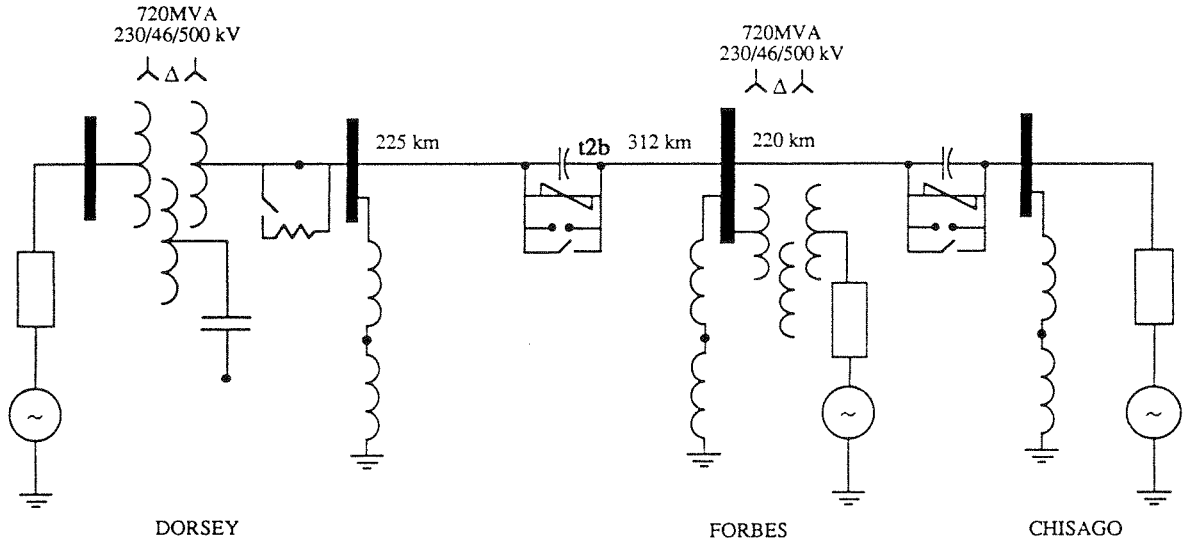

Figure 10. Third test system.

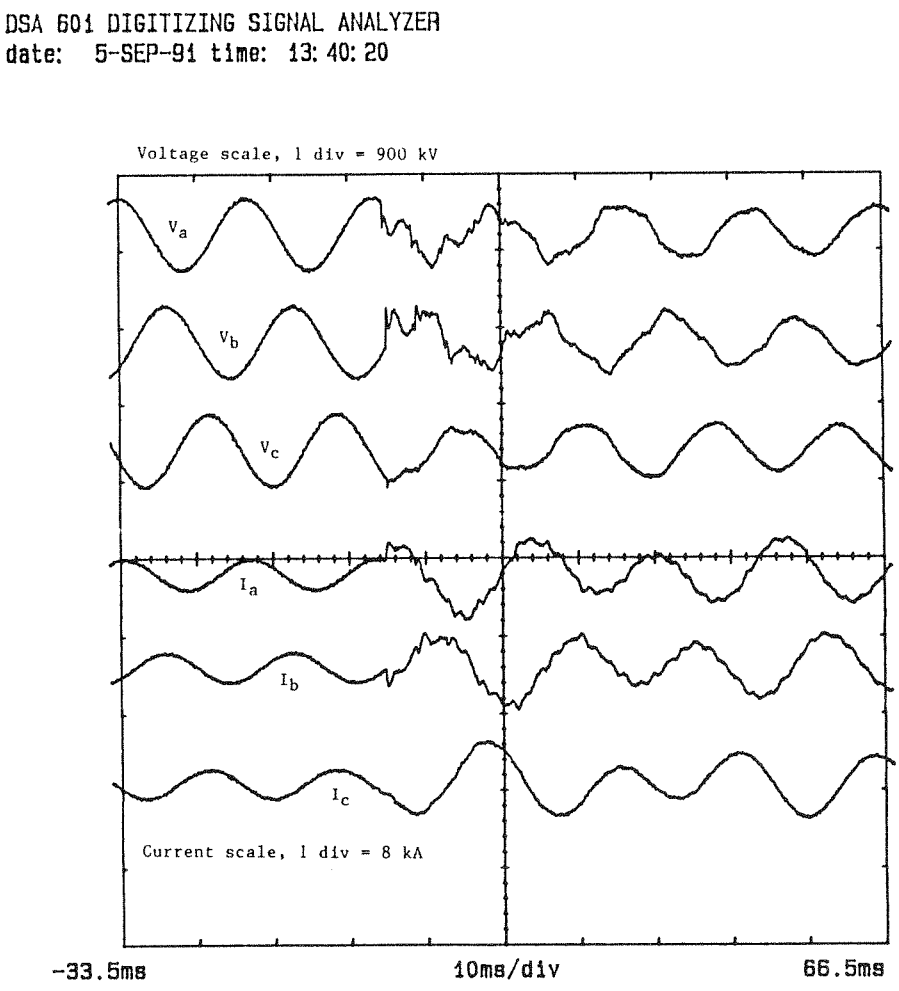

Figure 11. Dorsey relay voltages and currents for a 3-phase fault at Forbes. (No trip)

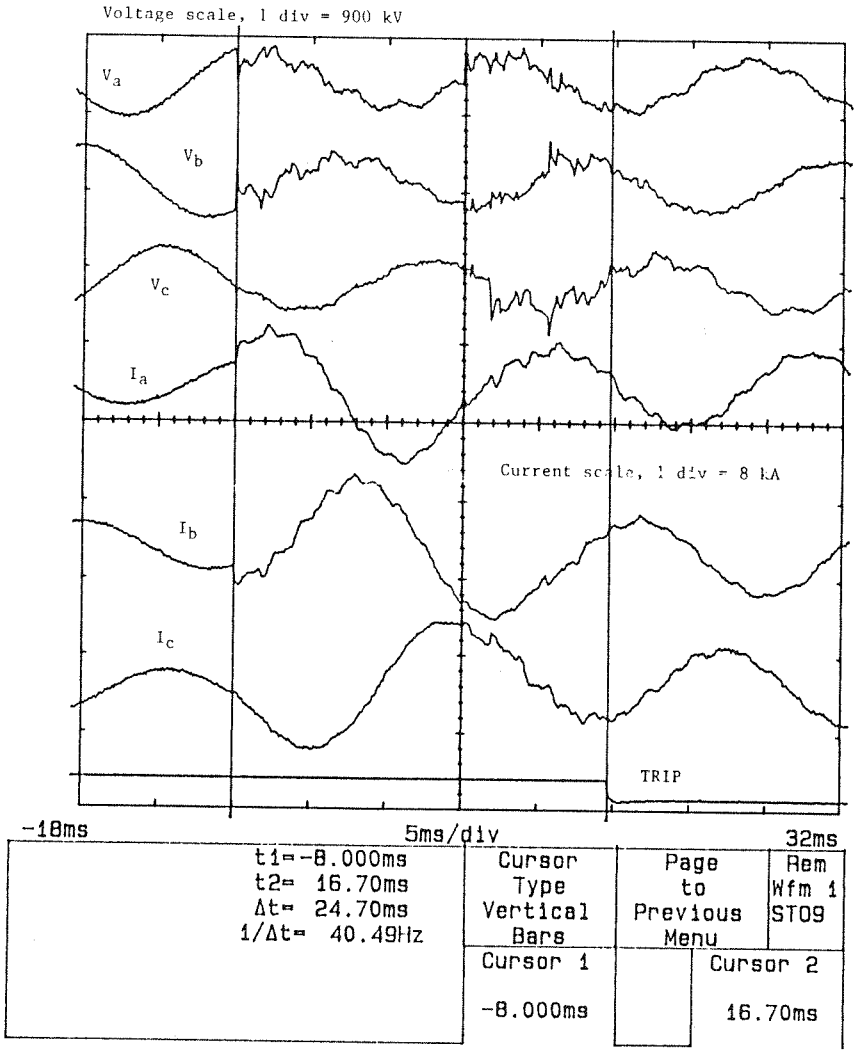

Figure 12. Relay voltages, currents and trip for a three phase fault at T2B.

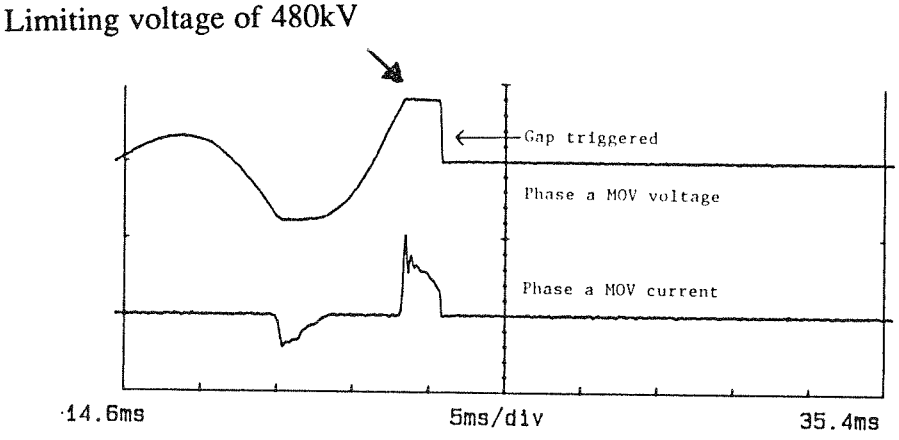

Figure 13. MOV voltage and current showing gap triggerring.

CONCLUSIONS

The sample results shown illustrate the capability of the DTNA to run real time simulations for testing relays. The size of the DTNA should be clear from Figure 1 and the fact that it has already been used to test two completely different power system devices, [6], indicates its versatility. The prototype DTNA is small enough to be taken to a substation and it has recently been used at the Dorsey converter station of Manitoba Hydro to check the performance of the existing relays on a future series compensation upgrading of the line. The DTNA can also be interfaced to existing analogue simulators to greatly enhance their capability and it is likely to be used in this way with present day HVDC analogue simulators. It can also be interfaced to exisiting analogue TNA's.

The simulator described in this paper is the first prototype of its kind with adequate capability for testing relays. A second simulator is now under development using a more capable DSP which is software compatible with the present DSP and each PE card will have 2 DSP's instead of the present single DSP. This will increase the size of the system under study and/or allow smaller time steps to be used in the simulations. Future improvements in digital hardware can only lead to more powerful real time digital simulators. There is little doubt that such simulators will find increasing use in power system analysis, investigation and control.

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