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PROTECTIVE RELAY
DIGITAL FAULT RECORDING AND ANALYSIS

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Protective Relay Digital Fault Recording and Analysis

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Introduction

The application of the DFR function to the protective relay has considerably increased the availability of data for system disturbance analysis. It has broadened the range of DFR application to well beyond just the large critical substation at a reasonably low cost. Improvements in communications, the declining cost of technology and the connectivity of "smart" devices in the substation have made fault data readily accessible for quick and more intelligent analysis. Analysis programs utilizing relay DFR data have proven to be valuable tools in analyzing protective relay and power system operations. New capabilities using distributed data allow new approaches to disturbance analysis using multi-terminal data to provide more accurate solutions. This trend will continue.

This paper discusses digital fault recording capabilities and analysis tools in two generations of microprocessor relays and how fault data is used for product development testing and real system application analysis. There are four parts. These are:

- A discussion of the relay digital fault record . . . important elements and how the event data is recorded,
- Fault recording used as a product development tool,
- Fault analysis tools and system fault analysis with fault analysis examples, and
- Trends

The purpose is to bring the relay engineer to a higher level of understanding of the fault record and its use for system and application analysis.

The Digital Fault Record

An adequate fault record for protective relay operation and system analysis requires data recorded before, during and after a system disturbance. There should be sufficient information in the form of analog and digital status (on/off) data to analyze and, if necessary, recreate the event. It may also be necessary to coordinate the relay operation with other devices around the system. The protective relay can do this. Its primary purpose, however, is to reliably clear the fault and restore the system with minimum outage time and system damage. Design limitations imposed by competitive market pressures limit the capabilities of functions secondary to protection such as fault recording. These limitations, however, may be addressed by a better understanding of fault recording usage and a more practical fault recording design. The following discussion addresses data requirements for a protective relay fault record.

Analog and Digital (on/off) Signals

Analog Signals

Analog signals are the digitally sampled voltage and current inputs into the relay. The sample frequency is limited by the relay design. The need to filter out higher frequencies in the analog signals that are detrimental to accurate sampling measurement of the fundamental frequency is dependent on the relay's algorithm. Typically, a filtering method is applied to limit the analysis frequency to half the sample frequency for anti-aliasing. Other considerations may also reduce the analysis frequency even more. Table 1 shows the Nyquist limit frequency for specified sample rates.

Table 1. Analysis Frequency and Resolution Based on Sample Frequency

Samples per Cycle	Sampling Frequency, Hz	Nyquist Limit Frequency, Hz	Digital Analysis Resolution, ms
4	240	120	4.167
8	480	240	2.083
12	720	360	1.389
16	960	480	1.042
20	1200	600	0.833

There are other techniques that allow the collection of sampled data before filtering is employed for the protection algorithm. In any case, the sample frequency directly affects the relay's memory requirements for recording and the frequency range that can be analyzed with the fault record.

Another factor to consider is the effect of sample frequency on the analysis being performed. Table 2 reflects the typical use of conventional [non-protection] DFR data. It is based on a 1992 substation automation survey of 20 utilities compiled by the author.

Table 2. Use of DFR Data

% of Use	Type of Analysis	Comments
70	Fault analysis	Fault type, location, sequence of events, etc.
15	System parameter verification	Line impedance, Fault current levels, etc.
8	Harmonic analysis	Limited to distribution by respondents
7	Other	Switching transient analysis, Troubleshooting

Eighty-five percent of the usage is for 60 Hz analysis. Of the remaining usage 8% was for harmonic analysis . . . determining the harmonic content of the analog signals. This analysis is generally limited to special applications usually on the distribution system or major industrial load points. Trouble shooting is defined as checking the status of contacts, presence of voltages, sequence of events, etc. and is not generally frequency dependent. It can be observed from the data that the Nyquist frequencies listed in Table 1 for analog data are adequate for most analysis uses, particularly for transmission line faults.

Digital (on/off) Signals

Figure 1 is an example of a typical relay logic structure. The operating elements are the impedance, voltage, current, directional or other measuring units that operate based on input analog signals and a set threshold value. They are either on or off. The binary inputs are voltage inputs into the relay to provide status information from external devices. The relay logic is usually modular in structure utilizing inputs from the operating elements, binary inputs, or outputs from other logic modules. The individual relay outputs operate based on the assertion of specific logic signals.

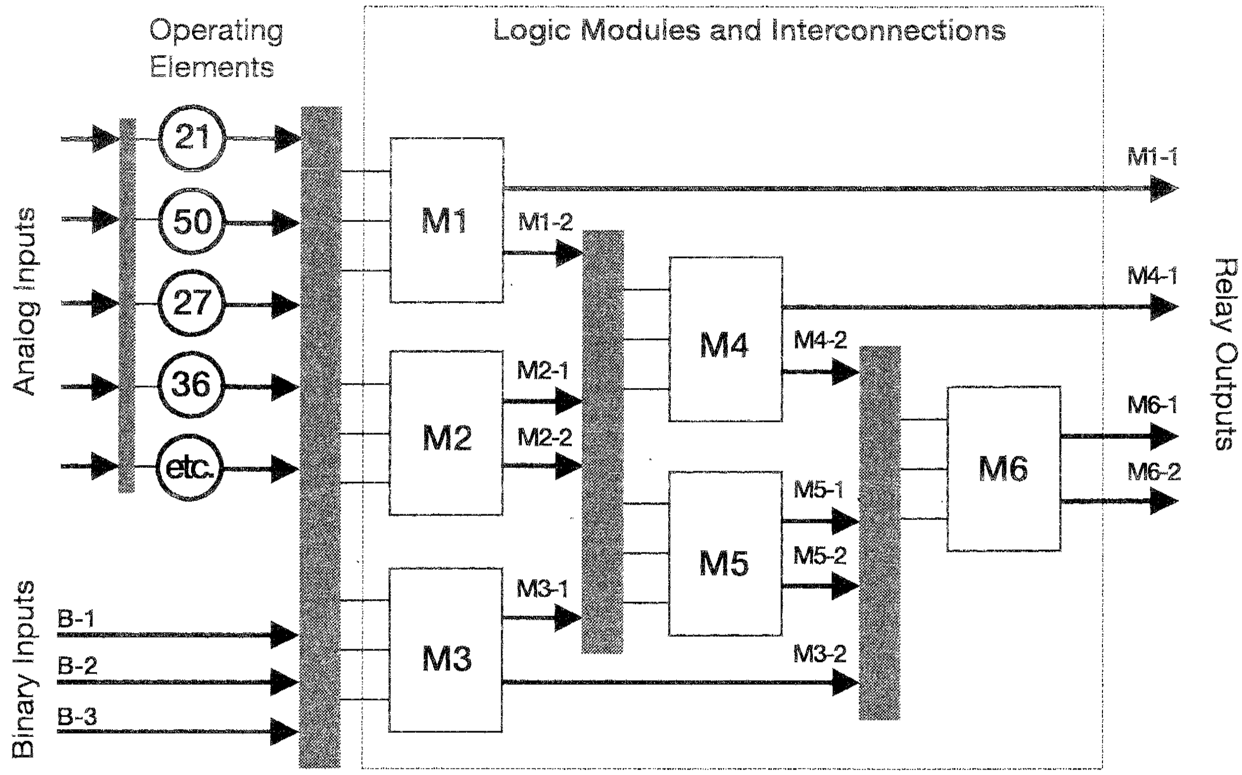


Figure 1. Relay Logic Structure

The resolution of relay operating elements and logic status is generally provided at the interval the elements or logic is computed. If an element is computed once every cycle then its resolution is approximately 16.67 ms. It is either on or off for the full cycle. If the element or logic is evaluated every sample then the resolution is the period of the sample frequency. Different relay operating elements can have different resolutions. Understanding the resolutions of a particular relay's digital status data ... operating elements, I/O and logic, is important for analyzing the relay's performance. Table 1 shows the minimum digital signal analysis resolution (time between samples). It should be noted that the greater number of operating element and logic status signals available to analyze an operating process the easier the analysis.

Coordination of Digital and Analog Signals

The operating unit signal status is generally the result of a computation using several samples of data that are collected previous to the operating unit calculation. For example, it may be that an impedance unit is computed only once a cycle and that it uses sampled data collected in the previous cycle. This is illustrated in Figure 2. The shaded region shows the collected samples for the next impedance unit (Z) computation. The computation is made every cycle using the corresponding cycle of sampled data. This shows how the impedance unit output Z is asserted at some time after fault initiation and is de-asserted at some time after the fault clears. This delay is dependent on the relay design and should be considered in the analysis process.

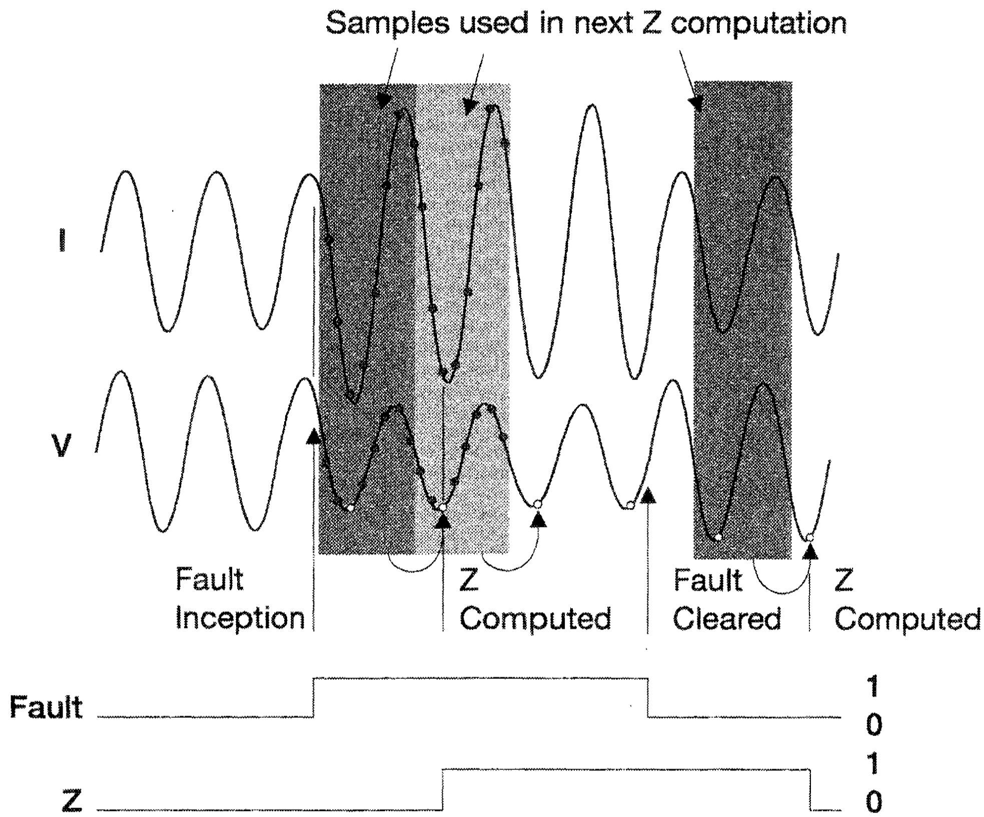


Figure 2. Coordination of Digital and Analog Signals

The Relay Fault Record

The following is provided to enable the protective relay engineer to develop an understanding of key fault record elements and how a fault record is produced in a relay. It is provided only as an example as it will differ to some extent from equally good solutions provided by other relay manufacturers. There are four basic issues to contend with. These are the:

1. System coverage,
2. Event initiation detector,
3. Pre- and post-initiation data requirements, and
4. Date and time of event.

System Coverage

Due to limited relay memory it may be desirable to limit the fault records saved to faults on the protected line or in close proximity to the line. Collecting data for remote faults can fill the memory buffers fast. There are a number of ways to restrict coverage utilizing relay operating elements. A typical method might be to use a forward overreaching and a reverse impedance zone to define the boundary for saved fault records. This insures saving records for faults on the protected line, the next bus and the reverse bus. The saving of a record may also be restricted to only those conditions where the relay is called to trip. In some cases it just may be desirable to capture all remote faults possible or those within the starting zone. The relay, however, should be checked often for data in the later case as frequent recording may result in over-writing fault records. Most relays have settings to provide some degree of flexibility.

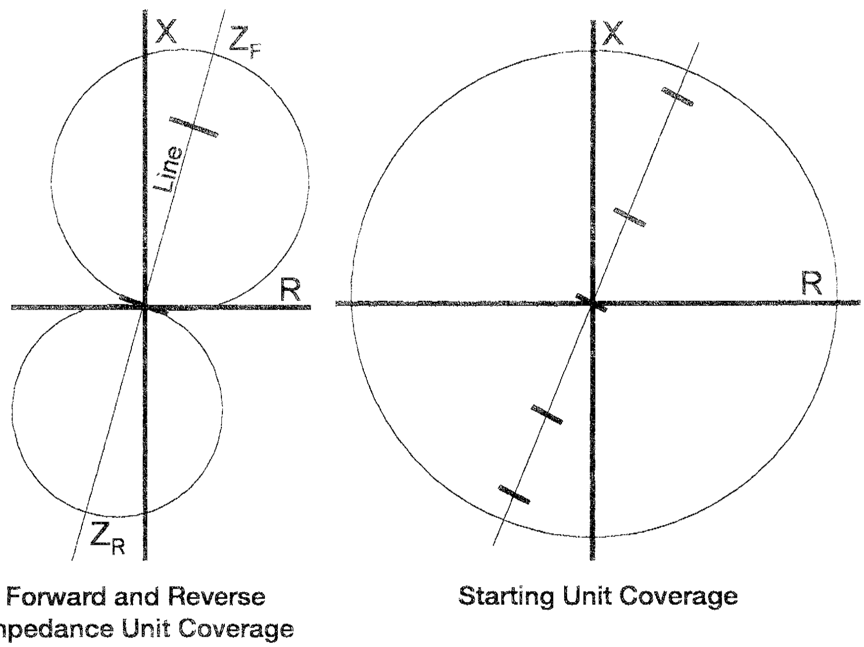


Figure 3. DFR Coverage

Event Initiation Detector

The event initiation detector, often called the starting unit or general start, is an overcurrent detector, undervoltage detector, rate-of-change detector, or other means to detect a fault inception or other event where a fault record is desired. The rate-of-change detector has been used effectively to identify fault inception times and other sudden system parameter changes with one sample period resolution. Following is an explanation of the rate-of-change detector.

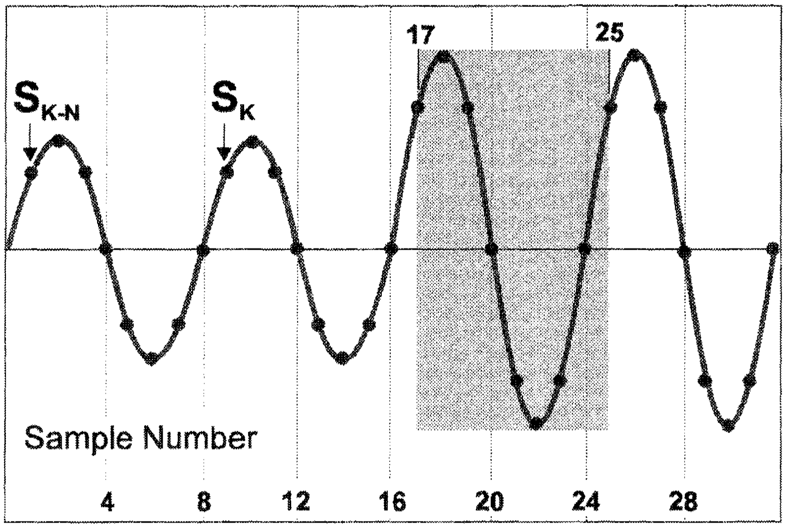


Figure 4. Operation of a Rate-of-change Detector

Figure 4 shows a typical periodic sine function being sampled at 8 samples per cycle. In the general case, under steady state conditions each sample's magnitude is measured as

$$S_K = A \sin(K2\pi / N + \theta)$$

where A is a constant, representing the peak amplitude of the function, θ is a constant depending on where sample 0 is taken within the cycle, K = 0, 1, 2, ..., N-1, and N is the number of samples per cycle.

From one cycle to the next, the respective sample magnitudes S_K and S_{K-N} are equal if there is no disturbance between them. The change detector continually compares the current sample S_K with S_{K-N} one cycle back. If there is a difference greater than a specified value then the change detector will operate. In this case, with a sample rate of 8 samples per cycle, the first change occurs when comparing sample 17 with 9. The change detector is asserted as the function transitions to the new steady state [fault] condition and the difference between S_K and S_{K-N} goes back to zero. This is indicated by the shaded area between samples 17 and 25. The steady state fault condition will continue after sample 25 until there is another parameter change created by either a subsequent fault condition or fault clearing. Again the change detector will operate until a new steady state operating condition is established. The resolution of the fault detection is the period (1/f) of the frequency at which the change detector is checked. This has proven to be a very reliable form of fault detection at a response less than 1.0 ms.

Pre- and Post-initiation Data Requirements

Pre-Initiation Data

Prefault [initiation] voltage and current data are the steady quantities that existed immediately prior to the fault inception. The prefault condition has not changed for a long time except for variations due to load changes. These changes are measured in seconds rather than cycles and are therefore unseen. The cycle immediately preceding fault inception, as measured by a high speed rate-of-change detector as described above, will be the same as the prior 10 or 20 cycles. Therefore, minimum prefault data is required.

The prefault data required is defined by the relay's faulted phase selection and fault location algorithm or the off-line fault data analysis program. For correct analysis that requires the use of prefault phasor quantities computed from one cycle [period] of sampled data, it is necessary that the prefault samples have correct phase alignment with the fault cycle [period] of sampled data used in the calculation. The fault cycle used could be any cycle during the fault. Correct phase alignment requires that the two sample sets, prefault and fault, are taken from the same time points in their respective cycles. This is shown in Figure 5. If you were to start counting from one with the first prefault cycle sample up to and not including the first selected fault cycle sample and divide that number by the sample rate (samples/cycle) the remainder must be zero.

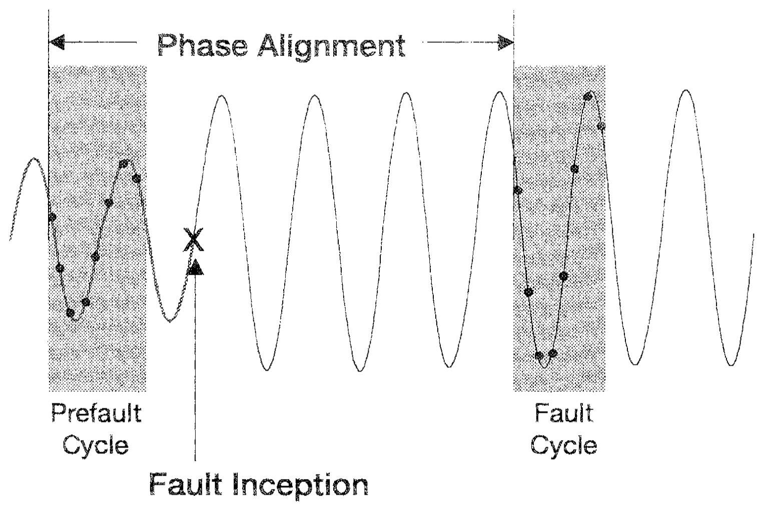


Figure 5. Prefault and Fault Cycle Phase Alignment

Two methods can be used to provide the required prefault data. The first is to use only one cycle of prefault data and rearrange the sample order by shifting the appropriate samples as illustrated in Figure 6.

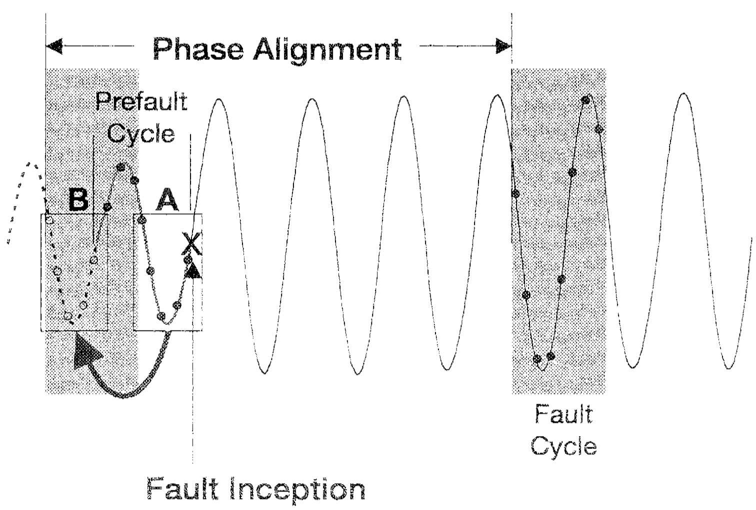


Figure 6. Altering the Sample Order for One Cycle Prefault Data

In this case of eight samples per cycle, the last five samples of the recorded prefault data enclosed in block A are equal to the last 5 samples in block B preceding the prefault record that were not recorded. The samples can be reordered before phasors are computed to produce the same result as correct phase alignment. The phasors can also be directly computed from the samples of the pre-fault cycle and then the appropriate phase shift can be added to provide the correct phase alignment.

The second method is to use 2 cycles of prefault data. With two cycles there will always be a full cycle of prefault data that will have correct phase alignment with any selected fault cycle.

Post Initiation Data

It is desired to capture the fault for its full duration from inception through clearing and reclosing. Forty-five cycles is recommended for conventional DFR applications. For protective relays this is not always practical to do with one continuous record. Correct zone 1 tripping for microprocessor relays would be expected to be in the two to three cycles. This is typically followed by two to four cycles of breaker clearing. Therefore, a 7 cycle post-initiation data record is adequate for most zone 1 or other three cycles or less tripping function. One level greater would be to capture data for sequential tripping on the protected line. Sequential tripping is when a remote terminal clears a line end fault and the local end responds to the system voltage and current changes and trips. An example would be a loss-of-load trip function where the remote end trips and the local end responds after remote breaker clearing. Considering that the trip logic and breaker trip will be sequential (one after the other) for the line terminal relays, 14 cycles of post-initiation should be considered. There is clearly no reason to save 45 or more cycles of data for zone 2 faults to capture line end conditions and/or reclosing if there is a more practical way to get the needed information.

For a zone 2 fault a record with pre- and post-initiation data can be recorded for the fault inception. The change detector will operate again on the breaker clearing at the end of zone 2 time and can be used to initiate a second record. Also, a reclose into a fault condition will produce an additional record. A successful reclose need not generate a fault record. There is no real need for the interim steady state fault data except as a means for maintaining time coordination. The new generations of line relays are able to time coordinate these records to less than a millisecond.

Date and Time

Date and time of the events can be time tagged with an accuracy limited by the relay's sampling rate. The fault occurs at some time between two samples. The first sample after the fault operates the change detector. This sample initiates the record and is tagged with the time of the relay's clock. Multiple records from the same event can be coordinated using the time tags. The relay's clock is periodically set with an IRIG, GPS or other synchronizing time signal to provide coordination with other system devices.

Recording the Fault Record

The following is a scenario for a typical fault recording using the four elements discussed above. Once a fault inception has occurred a two cycle prefault [initiation] record is held and post fault data is collected for the next 14 cycles. The fault impedance is calculated at each post-fault sample during the 14 cycles and if determined to be within the reach of the fault record zone the 16 (2 pre- and 14 post-fault [initiation]) cycle record is time tagged and saved. Change detection is not required while recording, but after the 14 cycles (the end of the record) the change detector is monitored again. If there are no changes (Figure 7) the fault has cleared the event is over with a successful reclose.

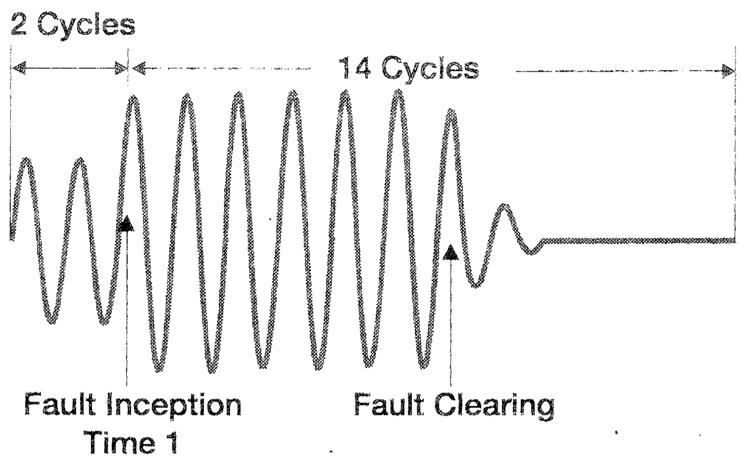


Figure 7. Typical Single Record Event

If the faults still persist (Figure 8), such as a zone-2 fault, the change detector will not operate until fault clearing [or other interim disturbance]. At that time a second record for the zone-2 event is saved and time tagged. In the event of reclosing additional fault records will be recorded if the fault is still present.

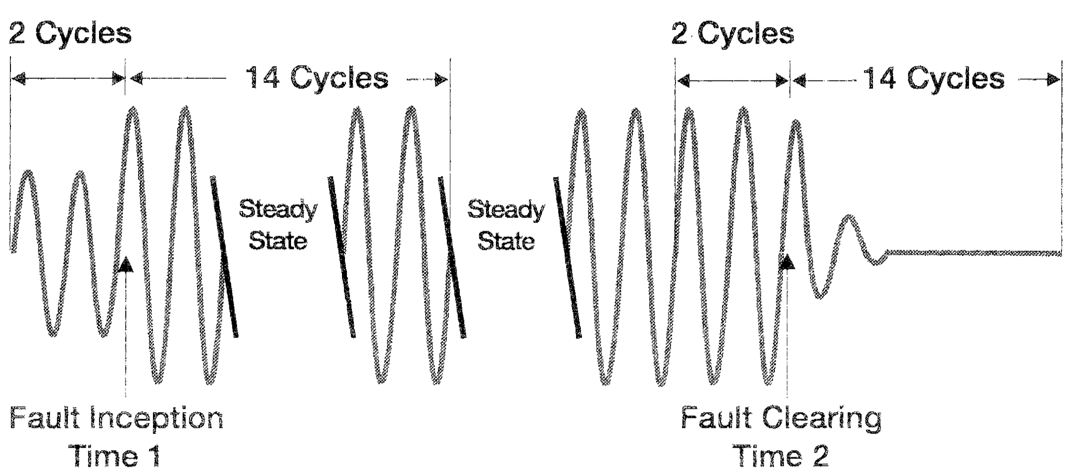


Figure 8. Typical Two Record Event

Relay Digital Fault Record Examples

Examples of two generations of line distance relay fault records are provided in Appendix A. Table 3 summarizes improvements made in the second generation relay. There are increases in the sample frequency and the cycles of fault data stored. In addition, the most significant change is in the number of digital signals recorded. This enables a more comprehensive understanding of the relay operation and easier fault analysis. These capabilities will continue to increase with each new generation of protective relays.

Table 3. First and Second Generation Relay DFR Comparison

Element	Generation 1	Generation 2
Sample Frequency	480	1200
Prefault Cycles	1	2
Post Fault Cycles	7	14
Analog Signals	7	9
Digital Signals	24	165

Fault Recording Used as a Product Development Tool

The relays digital fault record is key to the development process. The development of the relay is done in several phases for both hardware and software. This discussion, however, will be limited to the protection software that runs on the hardware platform and operating system that includes data recording and communications. The relay logic structure shown in Figure 1 can be used as an example. Analog inputs, operating element outputs, binary inputs, module output logic signals and outputs that are to be captured for the fault record can be identified from the relay logic structure.

Adequate design procedure dictates computer simulation and testing of operating elements and logic modules using modern computer mathematical tools prior to implementation on the hardware platform. Performance can be evaluated and benchmarks defined, such as element operations and operating times, for platform real-time testing. With the models developed and tested, sequential implementation and testing on the platform can be performed. The comparison can be done using the model and platform output [DFR] records. Testing the relay operating elements is illustrated in Figure 9 - a.

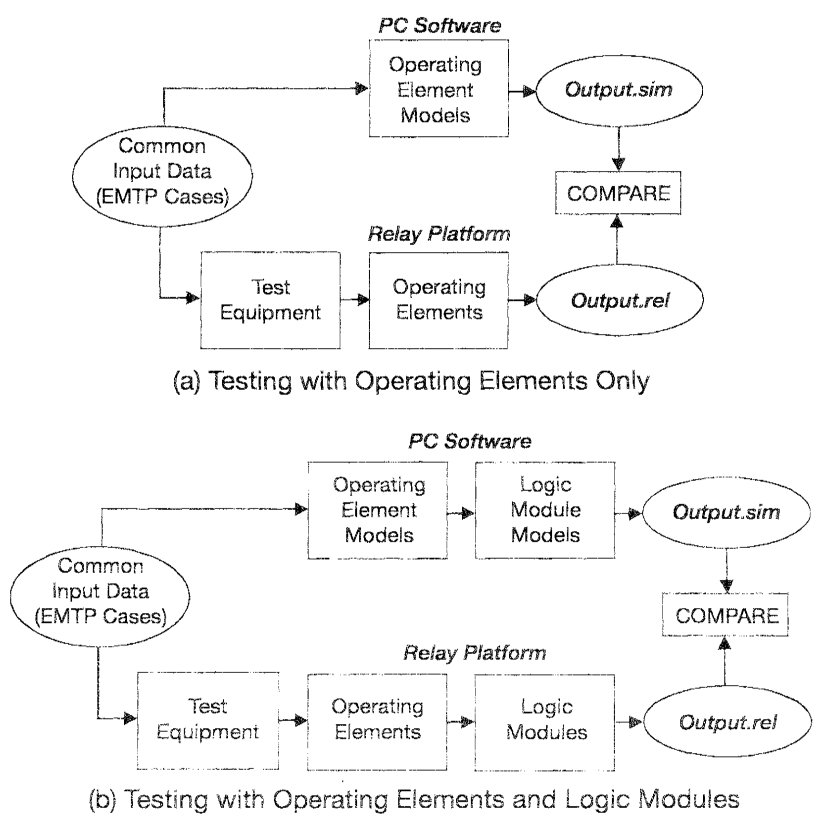


Figure 9. Testing the Relay Operating Elements and Logic

Common input data files containing the appropriate analog information are used for model and platform testing. Test results showing the sample-to-sample analog values and digital status (on or off) of the operating elements are collected in the respective output files, *output.sim* and *output.rel.* The files are compared. Differences are analyzed, explained, and if necessary, corrected. Once the operating elements are verified, logic modules are implemented and tested in a similar sequential fashion as illustrated in Figure 9- b. Each logic module is implemented such that it depends only on the elements and modules that have been implemented and tested to that point.

In the end system testing is still required on the final product. This approach allows significant debugging and points quickly to needed design modifications. This minimizes problems at system testing. Also, in the end we have a relay model on the PC that allows detailed evaluation of operating element performance using the relay's fault records. This is illustrated in Figure 10.

Figure 10 illustrates the analysis of a phase comparator operating element that operates based on the phase comparison of an operating and restraining quantity and the derived torque. This could be an impedance, directional, current, voltage or any other operating element. Inputs to the operating element are the appropriate voltages and/or currents required for computing the operating and restraining torques. The net torque is computed and if positive it will start integrating over time (rotating in the direction to operate). When the operation threshold (setting) is reached the unit operates (outputs a logical 1).

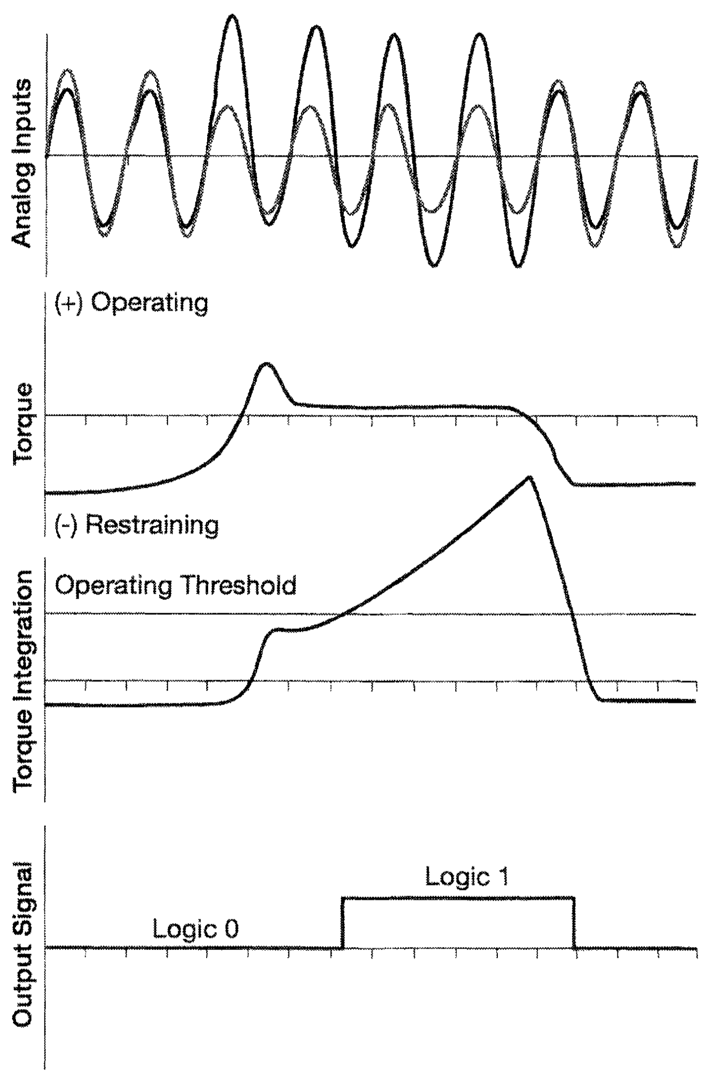


Figure 10. Evaluating Relay Operating Element Performance

Fault Analysis

Much is to be learned by analyzing data for all faults, not just those faults where operational problems occur. Protective relay DFR data, presented appropriately, can be used to:

- Analyze the performance of the relay and the protection scheme,
- Verify system (line) impedance parameters,
- Provide more accurate fault location,
- Aid in analyzing the power system response to system events . . . undervoltage, underfrequency, power swings,
- Solve problems that could otherwise not be solved,
- Forecast potential problems, and
- Provide data for relay testing

It is with these uses in mind that analysis tool functions are defined and examples are provided for their use.

Fault Analysis Tools

Following is a list of basic desired functions for a fault analysis tool using relay generated data.

Graphical display of analog and digital data

Graphical display of analog and digital data as a function of time (samples) allows a quick visual review of the event. Fault and prefault analog magnitudes and relay element, key logic signals and I/O operation can be easily observed. The analog plots should include all the phase voltage and current inputs, auxiliary inputs such as transformer polarizing current if used, and computed [from phase samples] zero and negative sequence quantities. An example is shown in Figure 11.

Multiple Record Analysis

The ability to analyze multiple records produced by all line end terminal relays for the same event allows more accurate fault location, analysis of pilot operations, and analysis of more complex events. An example is shown in Appendix A.

Calculation of Fault Quantities

The phasors for all of the analog quantities should be computable for any one cycle set of sampled data over the length of the record. Correct phase aligned prefault phasors should also be computable for correct phase selection and fault location computations.

Calculation of Fault Impedance and Location

Fault impedance and fault location should be computable for any one cycle set of sampled data over the length of the record. This should be done for each fault type . . . AG, BG, CG, AB(G), BC(G), CA(G), ABC. Fault resistance should be calculated from multi-terminal data records. Synchronized record from the line terminal relays allows accurate fault location and fault resistance calculations.

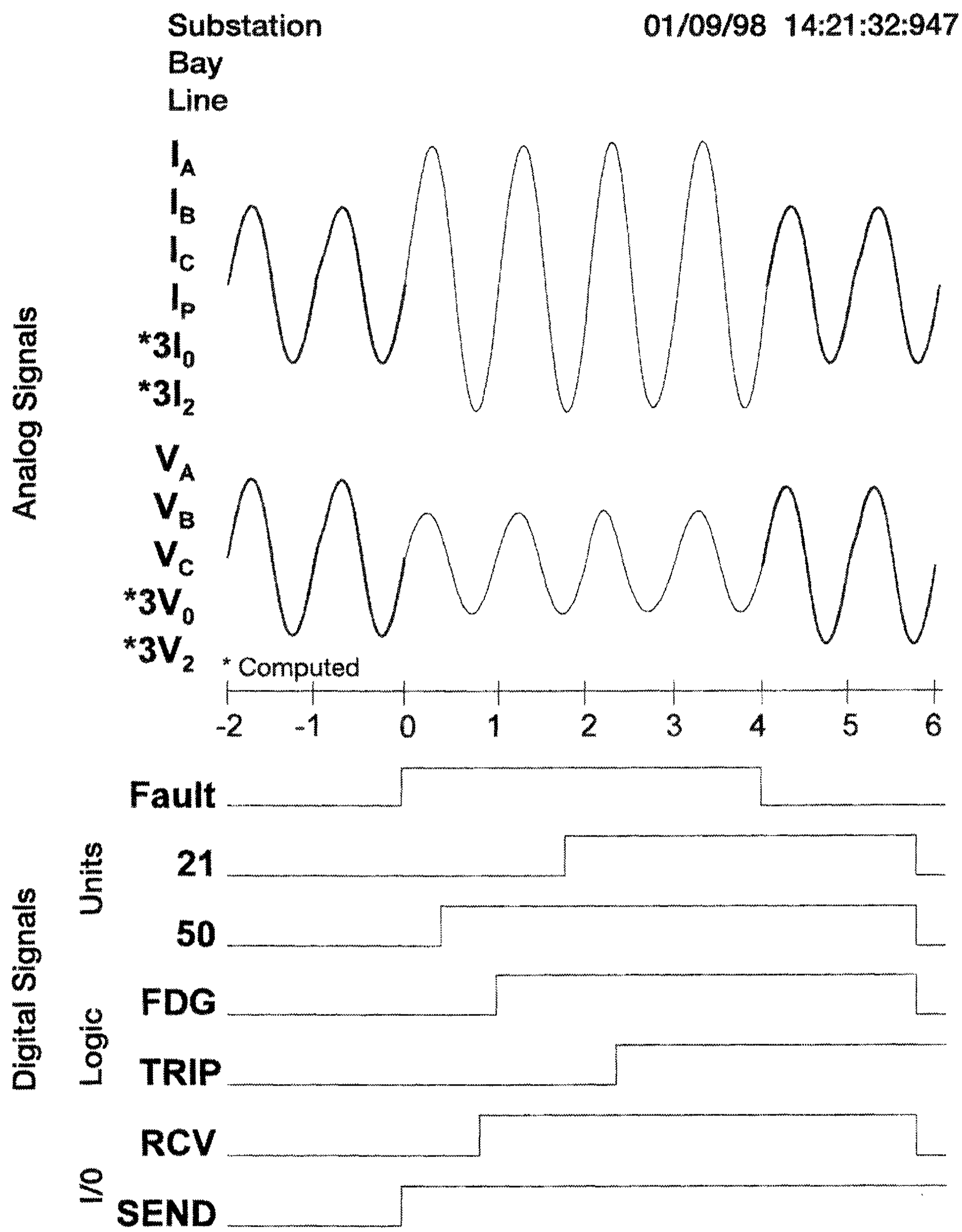


Figure 11. Typical Fault Recording Graphical Display or Printout

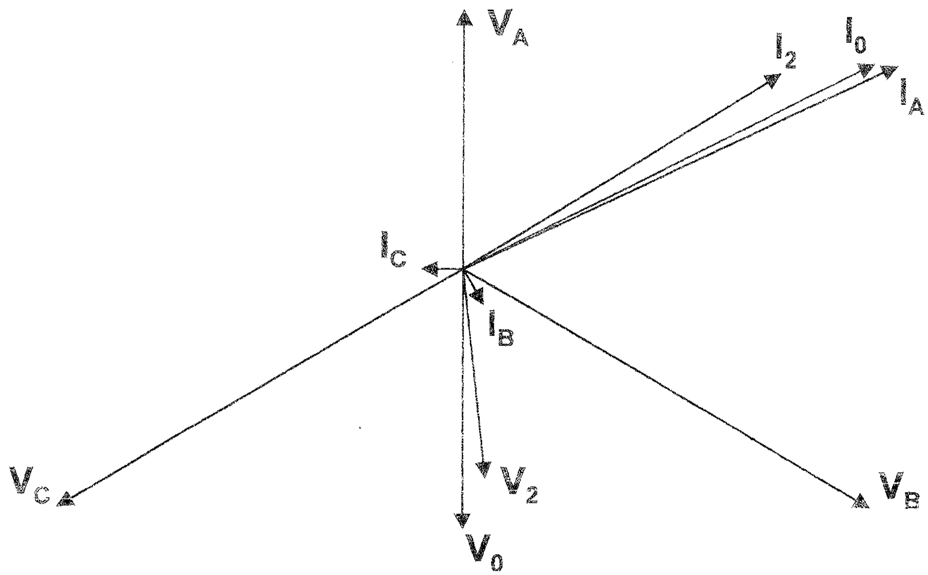


Figure 12. Typical Phasor Diagram for an AG Fault

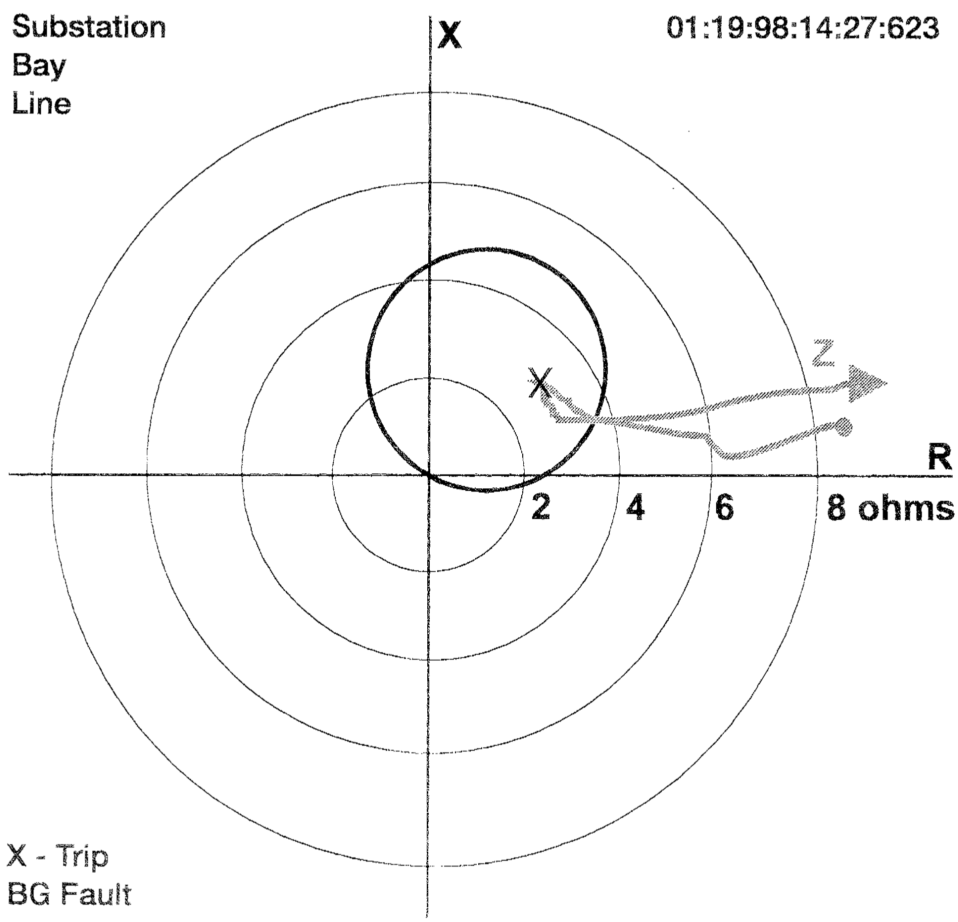


Figure 13. Typical Impedance Locus Diagram

Phasor Plots

Plotting the voltage and current phasors defined above on a polar plot to visually show their angular relationship is useful. This data can be useful when analyzing the performance of directional and other operating units, and records of two different relays that responded to the same event. An example is shown in Figure 12.

Plot of Fault Impedance Locus

Plotting the fault impedance locus over a specified range of the record provides the ability to determine the impedance location in the impedance (R,X) plane at a specified time and its effect on operating elements. This should be done for each fault type . . . AG, BG, CG, AB(G), BC(G), CA(G), ABC. The intersection of the impedance locus and the set impedance operating characteristics can be observed for both faulted and non-faulted phases. An example is shown in Figure 13.

Frequency Analysis

The ability to measure the frequency and harmonic components of the analog inputs should be provided limited only by the protective relay filtering.

COMTRADE Files

It is important to provide standard COMTRADE output files for playback into computer controlled test sets. With this capability the fault recorded by the relay can be reproduced for additional testing analysis. Also the COMTRADE file can be used by other analysis software.

Fault Analysis Examples

Four examples are discussed to show different examples of fault analysis. The examples are taken from fault data recorded by the first generation line protection product. Any problem discussed that resulted in an undesired operation has been corrected. Also, rather than providing detailed analysis of each example, only the key points of the analysis are discussed.

Example 1. Potential Circuit Grounding

This problem involved two numerical relays providing redundant protection at the same line terminal as shown in Figure 14. The backup relay consistently computed a fault location for single phase-to-ground faults farther than the actual fault location while the primary relay was consistently accurate. The analog data from the two relays for one specific event were plotted superimposed as shown in Figure 15. Immediate inspection reveals a zero sequence voltage problem. The current and voltage phasors were then computed from the same cycle of fault data. The results are shown in Table 4.

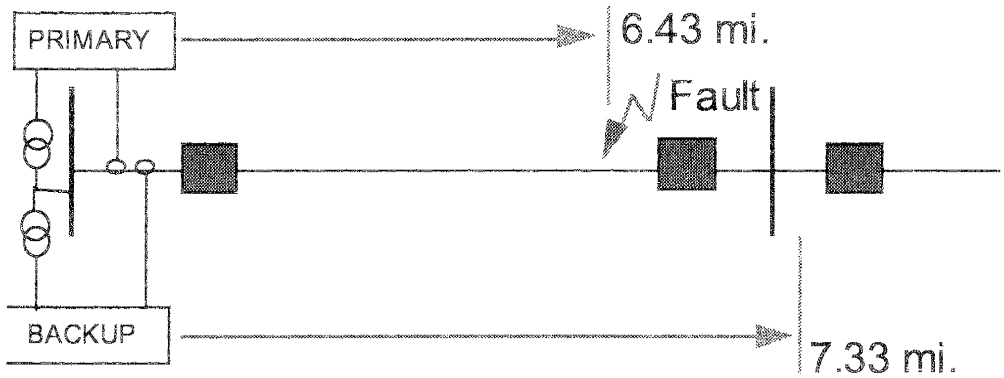


Figure 14. Redundant Protection with Different Fault Location Computations

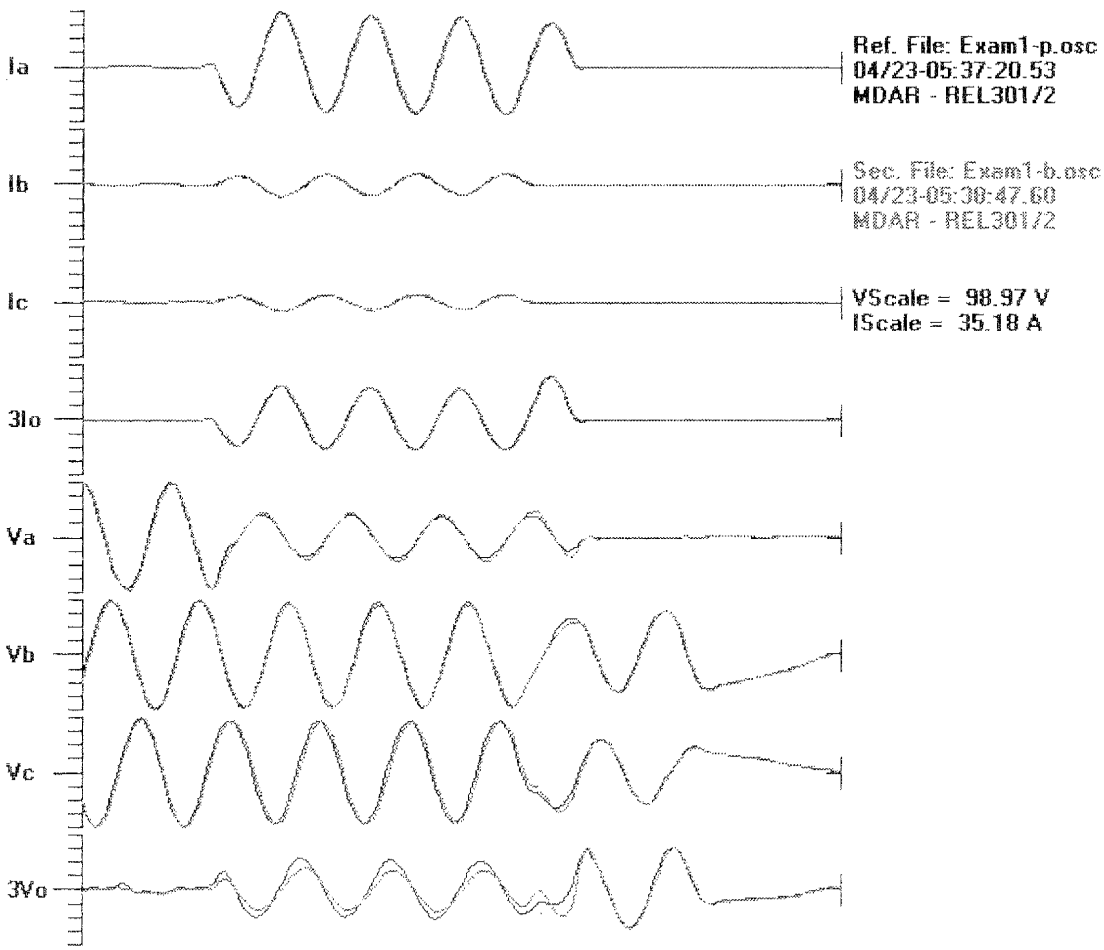


Figure 15. Plot of Primary and Backup Analog Data

Table 4. Comparison of Phasors

Phasor Quantity	Primary	Backup
Va	$27.76 \angle 0^0$	$31.01 \angle 3^0$
Vb	$67.64 \angle 251^0$	$64.9 \angle 253^0$
Vc	$66.45 \angle 126^0$	$66.31 \angle 123^0$
3V0	$35.71 \angle 197^0$	$24.64 \angle 192^0$
V1	$53.82 \angle 7^0$	$53.87 \angle 7^0$
V2	$14.66 \angle 193^0$	$14.86 \angle 194^0$
Ia	$22.35 \angle 284^0$	$22.23 \angle 284^0$
Ib	$4.82 \angle 101^0$	$4.82 \angle 101^0$
Ic	$3.45 \angle 100^0$	$3.45 \angle 100^0$
3I0	$14.08 \angle 286^0$	$13.99 \angle 287^0$
I1	$8.84 \angle 281^0$	$8.8 \angle 281^0$
I2	$8.83 \angle 286^0$	$8.78 \angle 287^0$

As can be observed from Table 4 all current quantities compare excellently. This rules out a current circuit problem. Likewise the positive (V1) and negative (V2) sequence voltages compare excellently. This rules out a phase voltage connection problem. This leaves the neutral of the backup potential circuit as suspect. The difference in the zero sequence voltage (ΔV_0) of the primary and backup relays was computed by:

$$\Delta V_0 = [3V0(\text{Primary}) - 3V0(\text{Backup})]/3$$
$$\Delta V_0 = (35.71 \angle 197^0 - 24.64 \angle 192^0)/3 = 3.79 \angle 208^0$$

Adding ΔV_0 to each backup phase voltage clearly gives comparable quantities seen and recorded by the primary relay. Therefore, something is generating this voltage in the backup potential circuit.

Table 5. Effect of ΔV_0

Phasor	Backup	ΔV_0	Backup + ΔV_0	Primary
Va	$31.01 \angle 3^0$	$3.79 \angle 208^0$	$27.61 \angle 0^0$	$27.76 \angle 0^0$
Vb	$64.9 \angle 253^0$	$3.79 \angle 208^0$	$67.63 \angle 251^0$	$67.64 \angle 251^0$
Vc	$66.31 \angle 123^0$	$3.79 \angle 208^0$	$66.72 \angle 126^0$	$66.45 \angle 126^0$

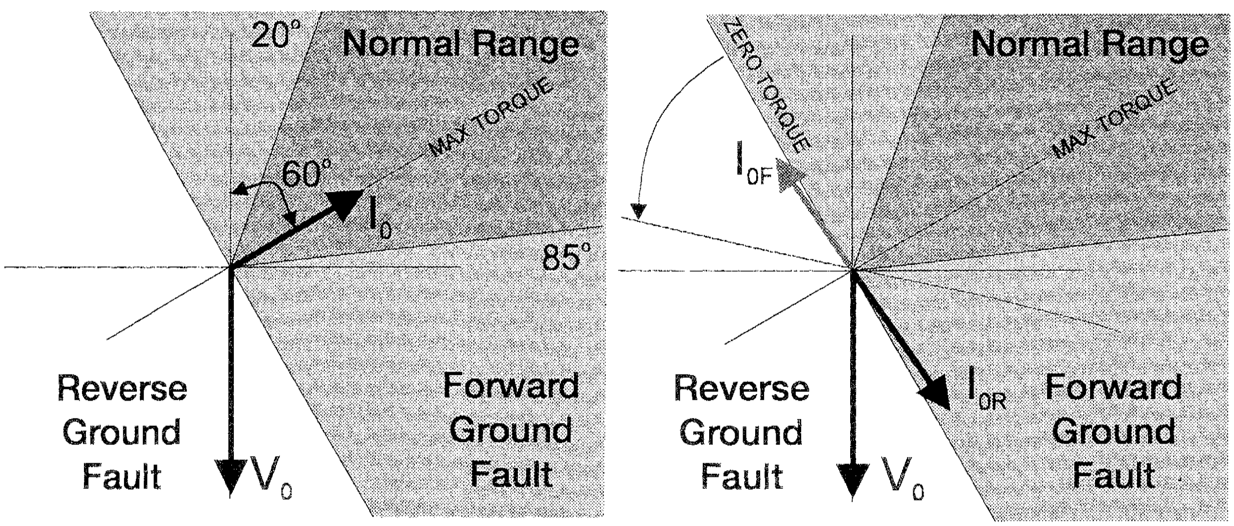
The two relays were provided voltage from separate secondaries of one potential transformer. Inspection of the potential circuit revealed multiple grounds on each circuit, one at the voltage transformer and one at the relay panel. This condition will most certainly produce a potential difference between the ground points due to ground potential rise during ground faults. This problem is addressed in the IEEE Guide for the Grounding of Instrument Transformer Secondary Circuits where single point grounding is recommended at the first point of application of secondary potential circuit in the control house (panel).

Example 2. Incorrect Directional Unit Operation on a Resistance Grounded System

Figure 16 - a shows the operating region of the forward and reverse directional units as defined by the zero sequence voltage and current phasor relationship during a ground fault. A ground fault is defined as forward when I_0 leads V_0 by 30^0 to 210^0. The normal region of operation defines the region where I_0 is expected, relative to V_0, for ground faults on effectively grounded transmission systems at all voltage levels. Figure 15-b shows I_{0R} and V_0 relationship for a reverse ground fault that occurred on a resistance grounded cable transmission system. This resulted in the forward directional unit operation and an undesired trip. A review of many fault records of forward (I_{0F}) and reverse (I_{0R}) faults at several locations showed that I_0 occurred close to the balance point (zero torque line) between forward and reverse.

Analysis showed that the transformer neutral ground resistors not only introduced resistance into the zero sequence network, but also caused the cable shunt capacitance to become significant. This caused a phase shift in the resulting I_0 from the normal range to that observed in Figure 16-b.

The solution was simply to rotate the zero torque line, the boundary between forward and reverse operation, as shown in Figure 16-b. This enabled correct directional sensing for this unique system.



(a) Directional Unit Design

(b) Recorded Zero Sequence Fault Phasors

Figure 16. Directional Unit Operation

Example 3. Mis-operation Due to Isolated Ground Source

The following example discusses a mis-operation that was the result of undesired, but real, operating condition. The system as shown in Figure 17 was set up when the breaker as indicated at Sub 1 was opened. This left only a zero sequence source for the Sub 1 to Sub 2 line at Sub 1.

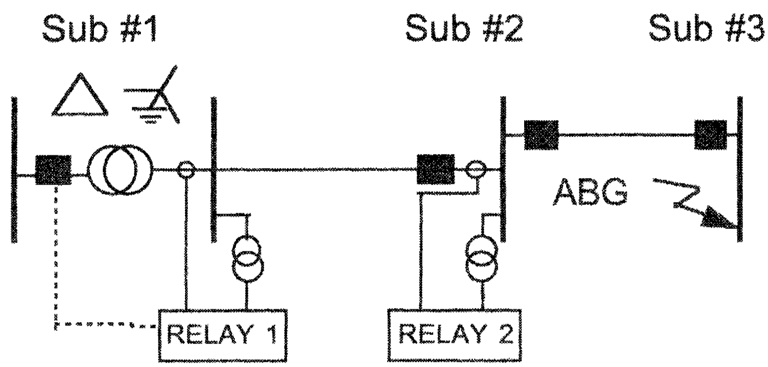


Figure 17. Isolated Ground Source at Sub 1

When the two phase-to-ground fault occurred at Sub 3 approximately 0.4 secondary amperes of zero sequence current flowed in the line. The fault type selections of both Relay 1 and Relay 2 were three phase. The phase selector could not determine any fault type and defaulted to three phase because of the small and relatively equal phase current magnitudes. The operation of the zone-1 phase unit requires only one of 3 three phase units to operate with three phase fault type selection. Using the following three phase unit equations and data of Table 6, analysis shows a three phase unit operation to occur at both relays.

$V_O = V_{XG} - I_X Z_R$ Operating

X = A, B, C and ZR = Relay impedance setting

$V_Q = V_{XY}$ Polarizing

XY = CB for A, AC for B, BA for C phase unit

Table 6. Fault Voltages

Phase Voltage	Relay 1 Mag.	Relay 1 Angle	Relay 2 Mag.	Relay 2 Angle
A	10.5	0	9.7	0
B	10.9	311	10.3	311
C	62.5	204	62.5	208
BC	60.2	214	61.0	217

The unit operates where V_O leads V_Q. Neglecting the effect of current, it is quickly seen that the operating quantity V_A leads the polarizing quantity V_{BC} for both relays. These satisfied the relays will trip. Relay 2 DFR data shown in Figure 18 shows the zero sequence current, the three phase fault type selection MP (multi-phase) signal, and the zone-1 three phase logic pickup Z1P. A similar record for Relay 1 shows the same results.

The most immediate solution to the problem was to enable supervising of the three phase tripping logic with phase overcurrent units set to an appropriate value. Three phase trip logic can also be modified requiring all 3-phase units to operate, all three phase directional units to operate or trip blocking when zero sequence current is present.

Although this is not a complex problem it illustrates how a protective relay fault record allows a quick visual analysis of analog and digital quantities to point quickly to what elements need to be studied.

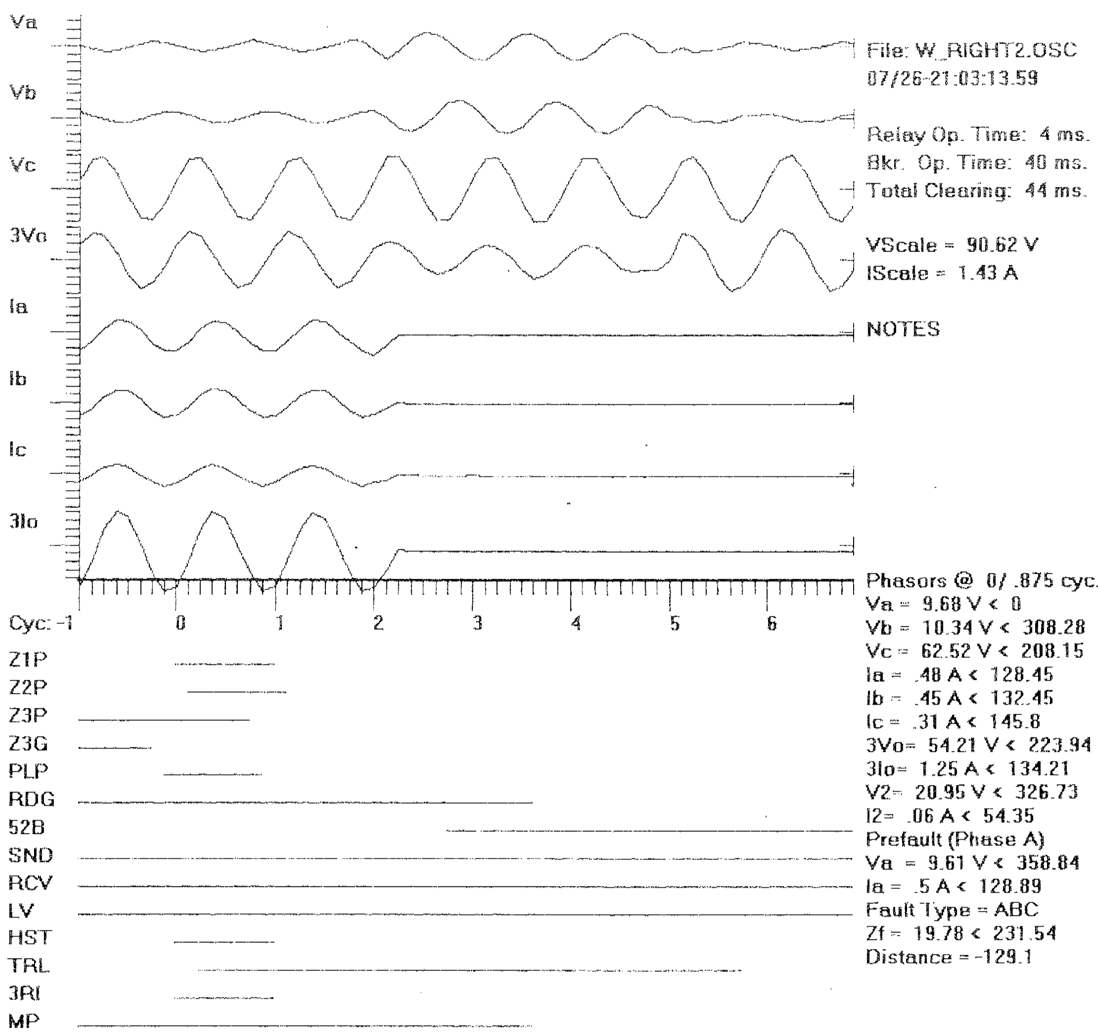


Figure 18. Relay 2 Digital Fault Record

Example 4. Dual Polarization and Unbalanced Phase Voltages

Dual polarization is the utilization of two directional sensing units. The first directional unit uses a polarization current source external to the relay and the internally derived zero sequence current. The external polarization source provides greater sensitivity to ground faults and is usually a ground current source such as a wye-grounded-delta power transformer or other grounding transformer. The second directional unit uses internally derived zero sequence current and voltage. Both unit's directional characteristics are defined in Figure 19.

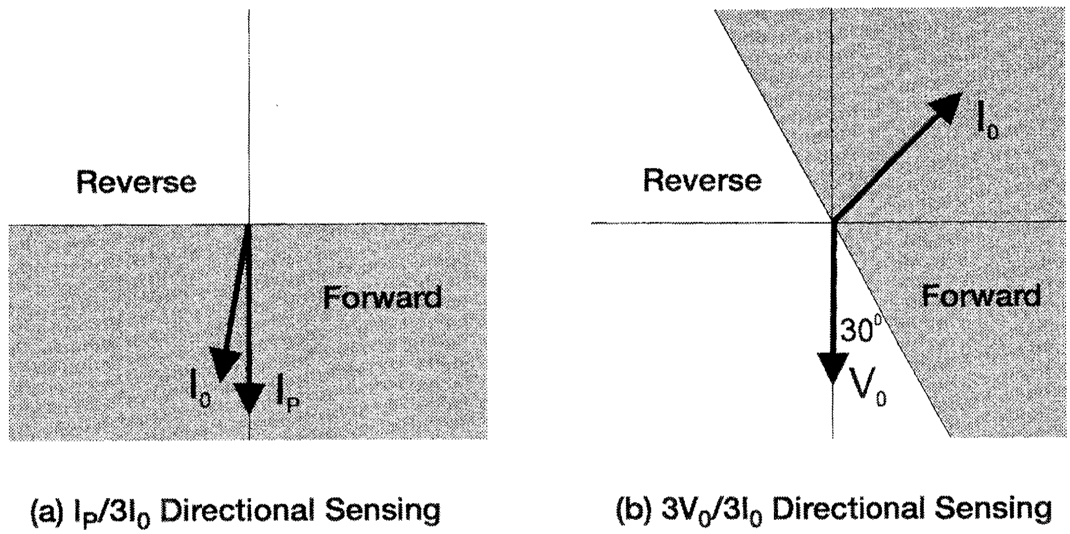


Figure 19. Dual Polarizing Directional Characteristics

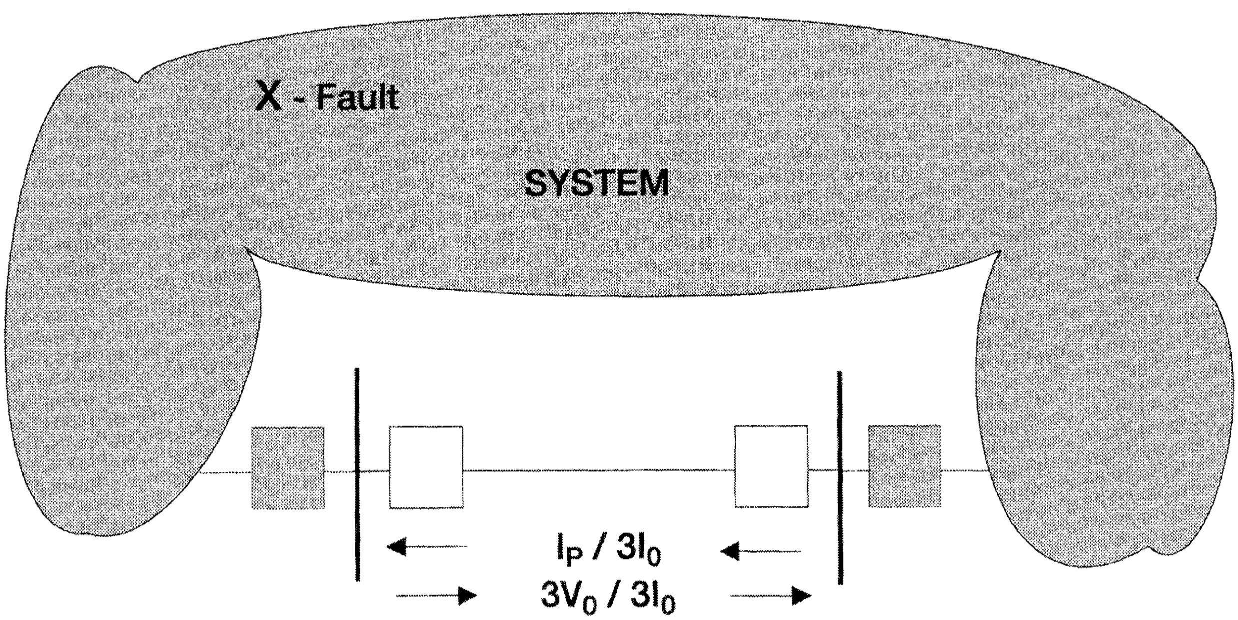


Figure 20. External Single Phase-to-ground Fault

Incorrect pilot tripping occurred on a typical two terminal transmission line protection scheme for a distant remote fault as illustrated on Figure 20. The data from both terminal relays indicated a forward fault that enabled pilot tripping. A review of the appropriate phasor relationships and the operating characteristics defined in Figure 19 showed forward $I_P/3I_0$ and reverse $3V_0/3I_0$ operation at one terminal, and reverse $I_P/3I_0$ and forward $3V_0/3I_0$ operation at the other terminal. The fault quantities from one terminal are shown in Table 7. I_0 leads V_0 by 203^0 (112 + 91), therefore the $3V_0/3I_0$ unit is forward. I_0 leads I_P by 191^0 (112 + 79), therefore the $I_P/3I_0$ unit is reverse. Since one unit sees the fault as forward at both terminals, pilot tripping resulted. Both unit types, individually as a two terminal system, operated correctly at each terminal . . . one forward and one reverse, for the external fault. Operating together, however, resulted in erroneous operation. Therefore, analysis determining why the two units differ in directional sensing for this fault was needed.

Table 7. Recorded Fault Quantities and Directional Unit Operation

Quantity	V_{MAG}	V_{ANG}	I_{MAG}	I_{ANG}	$I_{P\text{-}MAG}$	$I_{P\text{-}ANG}$
Phase A	59.6	0^0	5.0	133^0	-	-
Phase B	64.8	-116^0	2.0	72^0	-	-
Phase C	64.4	119^0	2.3	-55^0	-	-
Zero Seq.	0.64	-91^0	1.32	112^0	5.5	-79^0

Directional Unit		$I_{0\text{-}ANG}$ leads reference		Operation
Zero Sequence	$3V_0/3I_0$	$I_{0\text{-}ANG} - V_{0\text{-}ANG}$	203^0	Forward
Ext. Current Pol.	$I_P/3I_0$	$I_{0\text{-}ANG} - I_{P\text{-}ANG}$	191^0	Reverse

Table 7 also shows an unbalance in the non-faulted phases. This unbalance, although small, introduces enough effect on the "expected" zero sequence voltage angle at these small values causing the forward directional sensing. This is illustrated by changing the V_{ANG} values of Table 6 for phases B and C from -116^0 and 119^0 to -120^0 and 120^0, respectively, and computing the zero sequence voltage. This results in zero sequence voltage angle of 184^0 which is very close to what is normally expected. For this illustration, I_0 lags V_0 by 72^0 (112 - 184) which results in a reverse operation by the $3V_0/3I_0$ directional unit and agreement with the $I_P/3I_0$ unit.

It should be clearly understood that the $3V_0/3I_0$ units at both terminals are equally affected by the unbalance and operate correctly as a system ... one forward and one reverse. Likewise the $I_P/3I_0$ units operate correctly, but are immune to any unbalanced voltages. Applied together in dual polarizing logic, however, the discussed operating differences need to be considered.

The solution is to provide logic that detects the presence of the external polarizing current and giving the $I_P/3I_0$ unit operating priority. The $3V_0/3I_0$ directional unit can only operate if there is no external polarizing current. This implies that the polarizing current source, usually a transformer, has been removed from service. This contingency still leaves the exposure to the same problem until the settings are changed. This, however, is better than having no polarization source at all.

Trends

Advancements in the protective relay digital fault recording function will follow advancements in technology, the increasing requirements of merging substation protection, control, data acquisition and communication technologies into single systems, and the need for faster and more accurate solutions. With this will be increased amounts of information available to utility personnel. To reap the benefits of having this information requires the appropriate tools to analyze the large volume of data available from digital devices. Some anticipated tools are listed below. With them come the benefits of reduced outage time, improved power quality, reduced O & M cost, and a more productive technical staff.

Automated Data Collection and Synchronization

Collecting data from different remote fault recording devices at a master location for event coordination and analysis. All records for the same event are identified, synchronized, analyzed and saved. This will require automated data file recognition and translation for different product manufacturers and generations. Data management will also be required to organize the data and provide event summaries.

System Event Data Base

Not only are individual events analyzed, but a historical relational database maintained. This will permit statistical analysis of fault location, fault type, protection scheme performance, and other parameters possibly revealing areas to improve the system.

Wide Area Disturbance Analysis

Fault analysis tools currently provide two and three terminal fault analysis providing such functions as event record synchronization, accurate faulted phase selection, fault location and fault resistance, pilot channel coordination, terminal voltage phase displacement, and breaker operation sequence. This capability will expand to wide area solutions coordinating all system fault records generated from the same event.

Expert System Analysis

Records are automatically analyzed utilizing rules developed base on years of experienced engineering analysis. Problems are identified and solutions recommended. New rules will be continuously added as experience expands.

Protection Testing Database

Fault records of actual system events that produce undesired relay operations or test the performance boundaries of the relay will be developed, grown and maintained. These records will be used with modern test equipment to recreate the event during product development by the manufacturer or product evaluation by the user to reduce product acceptance time.

References

1. "Substation Control and Communications Survey", ABB Power T&D Company Inc., 1992.

2. "IEEE Guide for the Grounding of Instrument Transformer Secondary Circuits and Cases", ANSI/IEEE C57.13.3, 1983, Section 2.

3. "Fault and Disturbance Data Requirements for Automated Computer Analysis", IEEE Power System Relaying Committee Special Publication, IEEE Catalog No. 95 TP 107.

Biography

Elmo Price received his BSEE degree from Lamar University in 1970 and MSEE degree in Power Systems from the University of Pittsburgh in 1978. He began his career with Westinghouse in 1970 and worked in several engineering positions including: Design Engineer and Sales Engineer for the Small Power Transformer Division in South Boston, Virginia; Electrical Systems Design Engineer for the Gas Turbine Systems Division in Philadelphia, Pennsylvania; T&D Systems Engineer for T&D Systems Engineering, Pittsburgh, Pennsylvania providing design and application support for T&D product manufacturing divisions and their customers; District Engineer and Advanced Technology Specialist for T&D Marketing in New Orleans, Louisiana providing product sales, application and service support. With the consolidation of the Westinghouse T&D divisions into ABB in 1989 Elmo assumed regional responsibility for product application support for the ABB Protective Relay Division. In 1992 he joined the Substation Control and Communications group in Coral Springs, Florida. In 1994 he became the Manager of Product Management and Consulting which is responsible for protective relay application support, defining and developing functional specifications for new concepts of system protection to meet new market and technical requirements, performance verification testing of new products, and protective relay application schools. Elmo is a registered professional engineer and a member of the IEEE.

Reserved for Notes

Appendix A. Digital Fault Record Examples

First Generation Protection Digital Fault Recording

This case is the result of a zone-1 CG Fault on 230 kV system as determined by the digital zone-1 ground signal Z1G and the faulted phase selection signal CG. The relay tripped the breaker at Point 1 in 28 ms. This is determined by the trip seal digital signal TRL. The breaker cleared the fault at point 2 in 54 ms. This is determined by the open breaker digital signal 52b and the voltage and current analog signals. The breaker operating time is 26 ms. There are 8 analog signals and 9 of 24 possible digital (on/off) signals. FDG indicates forward ground fault, HST is high speed trip, and LV is low voltage.

Second Generation Protection Digital Fault Recording

This case is the result of a Model Power System test using the system diagram shown below. The fault locations indicated are approximate as they are based on positive sequence pi-section impedances and do not include lead and fault switching impedances. Impedances are shown in primary ohms. The line length in secondary ohms is 5.75 ohms and the relay's zone-1 impedance reach setting is 5.46 ohms -- 95% of the line length. The case is an AG fault applied at fault location F3 with 10 ohms primary fault resistance (2.5 ohms secondary) plus additional lead and connector resistances. The fault location is at about 85% of the relay setting from the Left Bus and 20% of the relay setting from the Right Bus. The scheme is step distance (non-pilot). Distance calculations are based on 100 mile line.

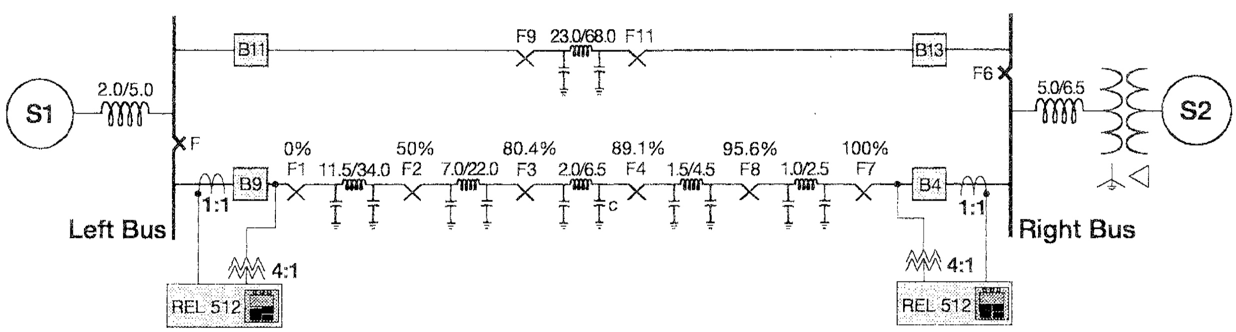


Figure A1. Model Power System Two Terminal Configuration

The attached DFR record shows the operation of both line terminal relays. Tripping is confirmed by the DSP TRIP SEAL signal in Word (group) #10, Combined Logic Output. These signals assert the trip outputs. Fault clearing from the Right Bus occurred in 49 ms. (Point #1) and clearing from the Left Bus occurred in 166 ms. The breaker operating time is fixed at two cycles plus time to next current zero.

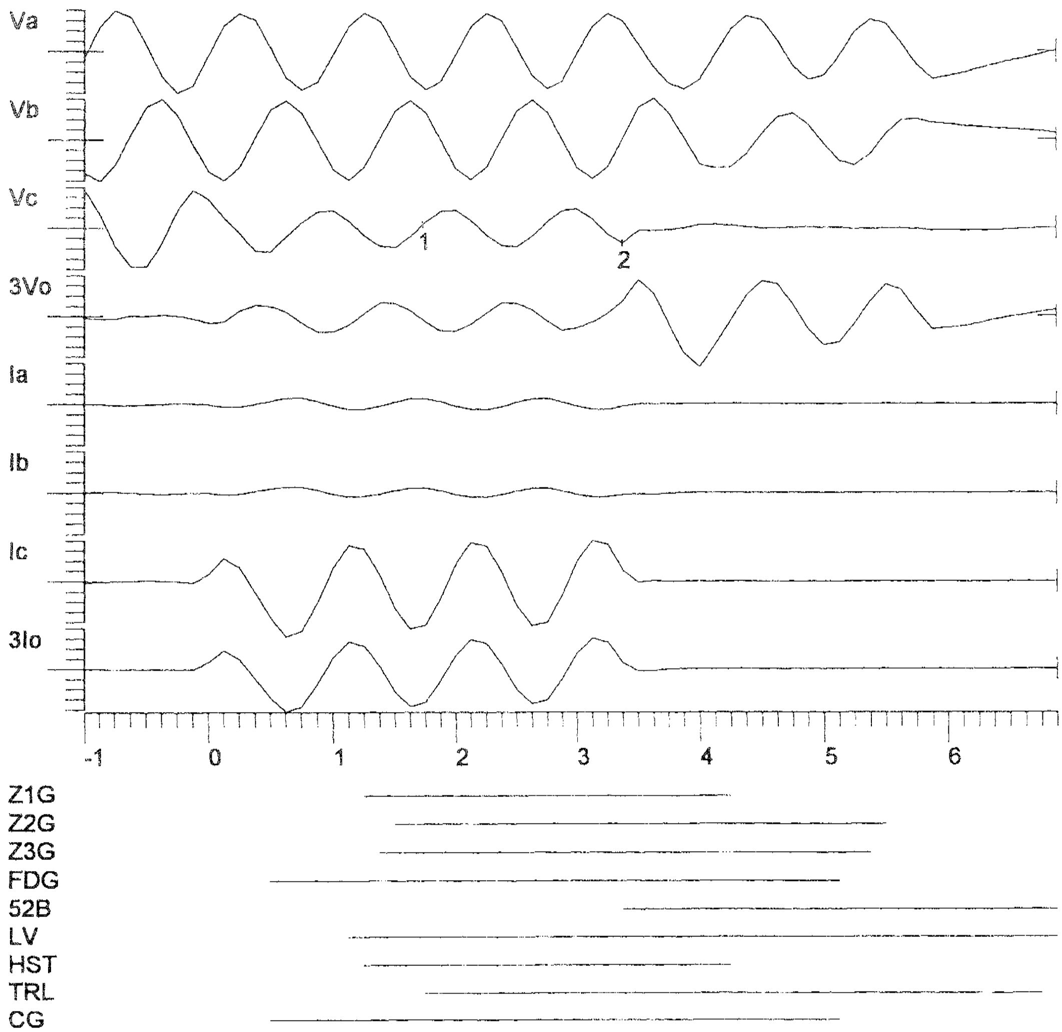
Single ended fault location computation in the relay includes the effect of prefault load current and fault resistance. From the Right Bus the single ended fault location was computed to be 16.4 miles. From the Left Bus the fault location was computed to be 91.6 miles. The fault location was computed again from the Left Bus to be 81.0 miles at a time after the Right Bus cleared removing the load current and Right Bus contributions. The fault location using the two terminal computation was 83 miles from the Left Bus. The fault resistance was computed to be 2.8 ohms secondary.

Reserved for Notes

First Generation Protection
Digital Fault Record

File: MDAR.OSC
04/08-08:50:31.02

VScale = 94.36 V
IScale = 35.11 A



Phasors @ 1.125/ 2 cyc.

Va = 62.5 V < 0 Ia = 3.42 A < 206.72
Vb = 64.94 V < 232.29 Ib = 2.76 A < 208.99
Vc = 31.44 V < 115.13 Ic = 26.56 A < 35.93
3Vo= 24.77 V < 292.35 3Io= 20.46 A < 38.41

Sequence Quantities

V1 = 52.86 V < 355.88 I1 = 9.82 A < 274
V2 = 13.21 V < 59.88 I2 = 9.93 A < 156.15
Vo = 8.25 V < 292.35 Io = 6.82 A < 38.41

Prefault (Phase A) @ -1/-.125 cyc.

Va = 67.66 V < 311.53
Ia = .65 A < 115.53

Operation:

Relay Op. Time: 28 ms.
Bkr. Op. Time: 26 ms.
Total Clearing: 54 ms.

Fault @ 1.125/ 2 cyc.

Type = CG
Zf = 0.78 < 78.35
Distance = 6.38

Notes:

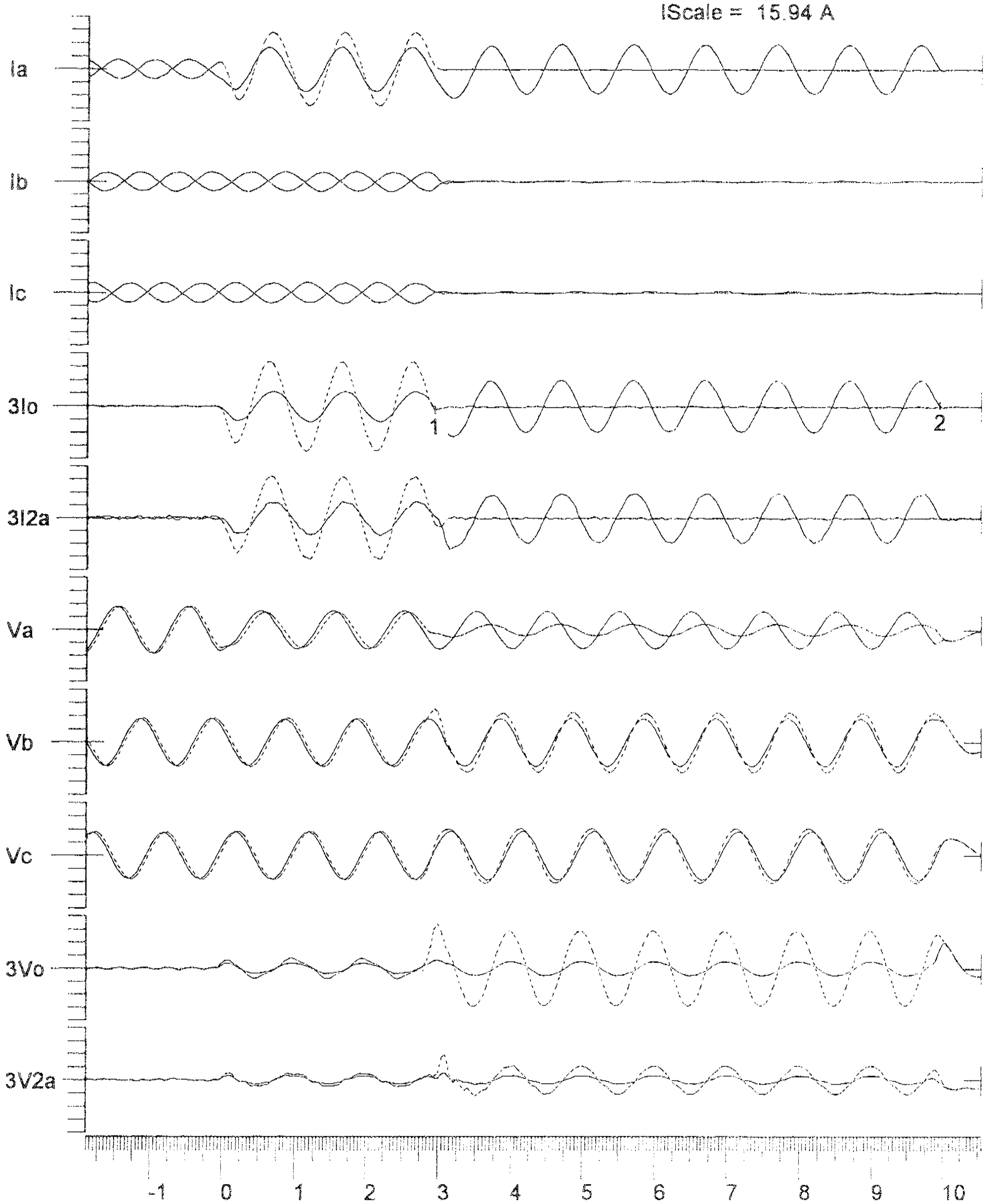
1. 7.24 V, 27.6 ms.
2. -35.86 V, 53.9 ms.

Reserved for Notes

Second Generation Protection
Digital Fault Recording

File: F3956r.rel (Dotted Line)
File: F3956l.rel (Solid Line)
12/02/1997,-11:12:32.52174
MPS SOURCE 2
RIGHT BUS
B4 BREAKER

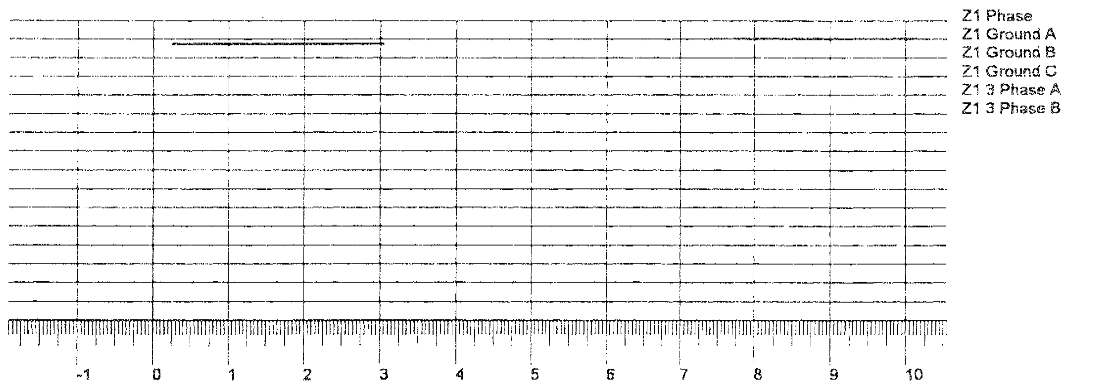
VScale = 186.9 V
IScale = 15.94 A



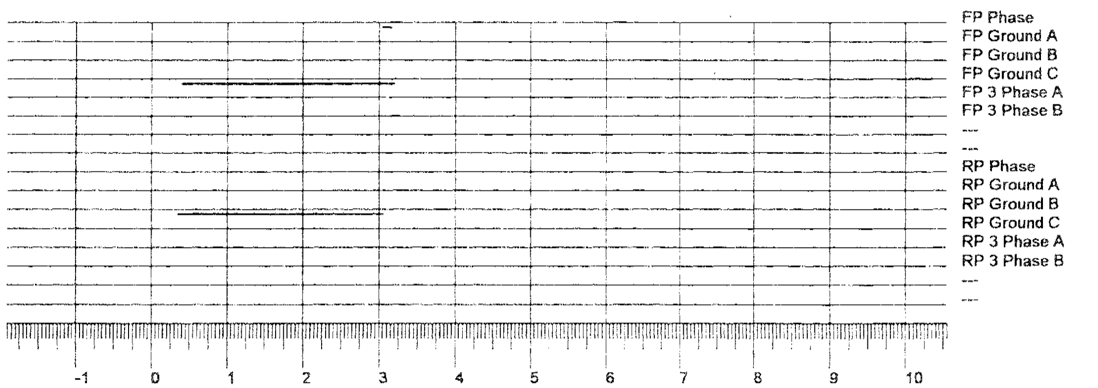
Reserved for Notes

File: F3956r.rel (Lower Line)
File: F3956l.rel (Upper Line)
12/02/1997,-11:12:32.52174
MPS SOURCE 2
RIGHT BUS
B4 BREAKER

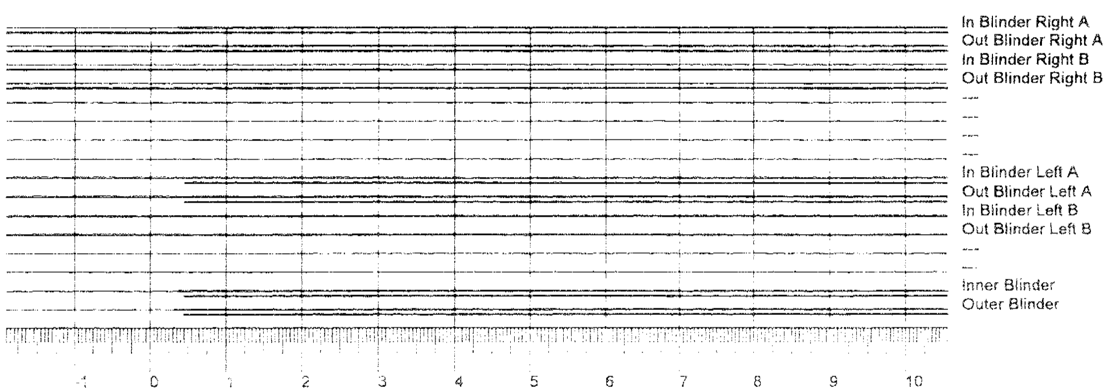
Zone 1 Units (1)



Pilot Forward/Reverse Units (2)



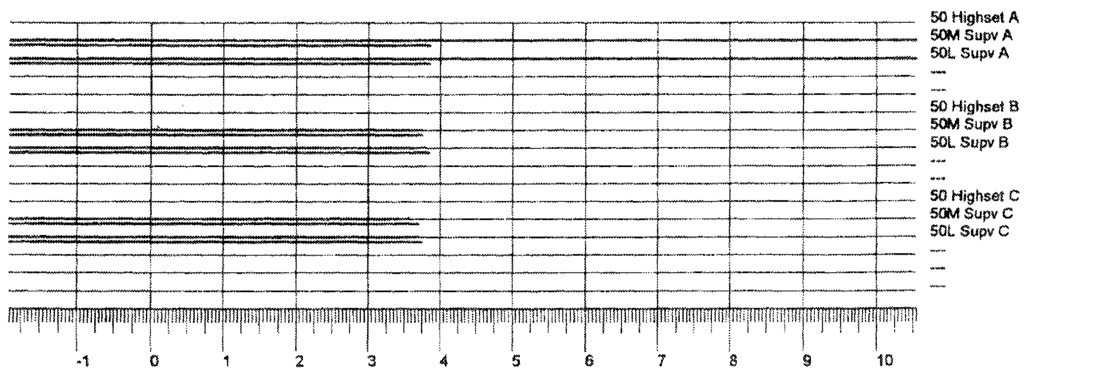
Blinders Right/Left Units (3)



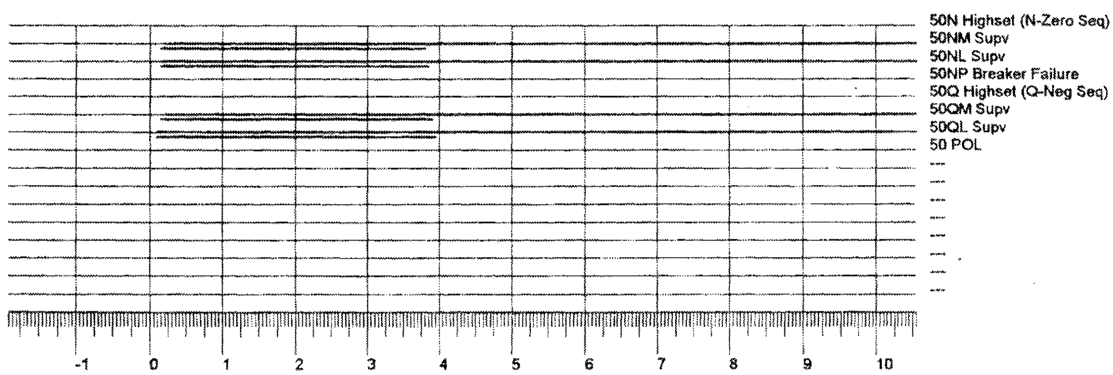
2

File: F3956r.rel (Lower Line)
File: F3956l.rel (Upper Line)
12/02/1997,-11:12:32.52174
MPS SOURCE 2
RIGHT BUS
B4 BREAKER

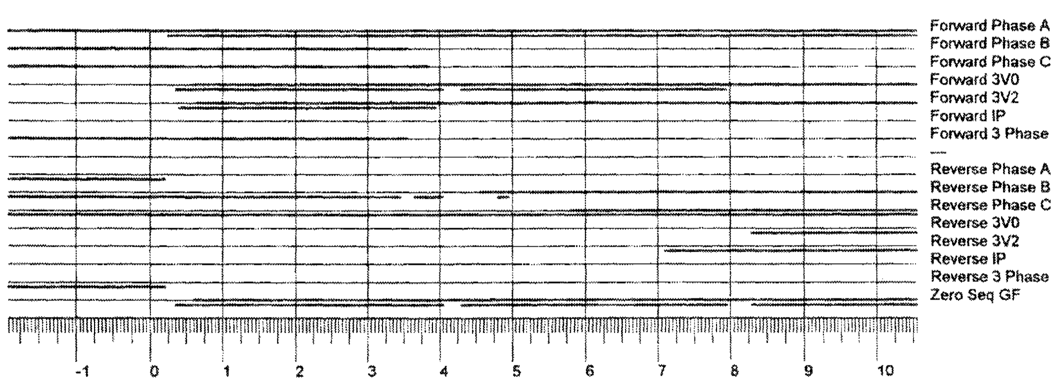
Type 50 Phase A,B,C Current Units (4)



Type 50 Ground and Negative Sequence Current Units (5)

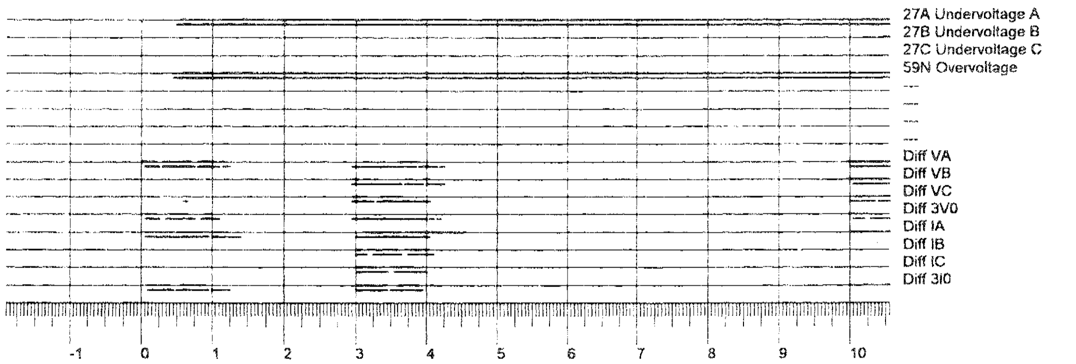


Directional Forward/Reverse Units (7)

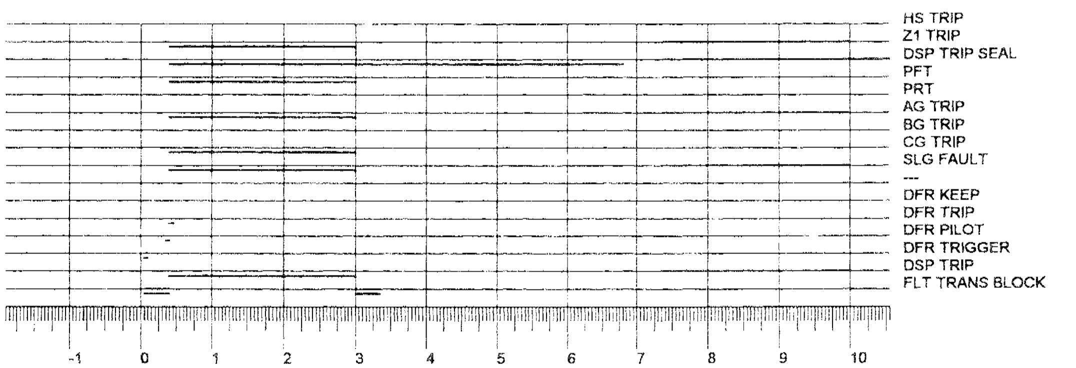


File: F3956r.rel (Lower Line)
File: F3956l.rel (Upper Line)
12/02/1997,-11:12:32.52174
MPS SOURCE 2
RIGHT BUS
B4 BREAKER

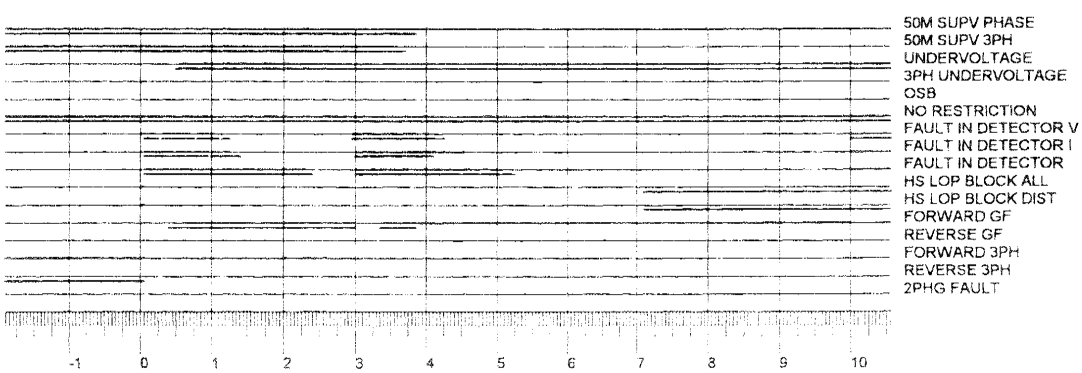
Voltage and Fault Detector Units (8)



Combined Logic Outputs (10)

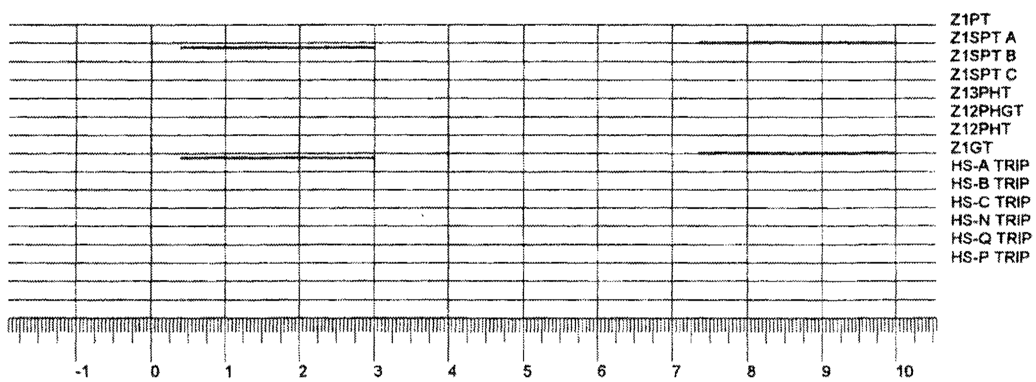


HS Supervisory Logic (11)

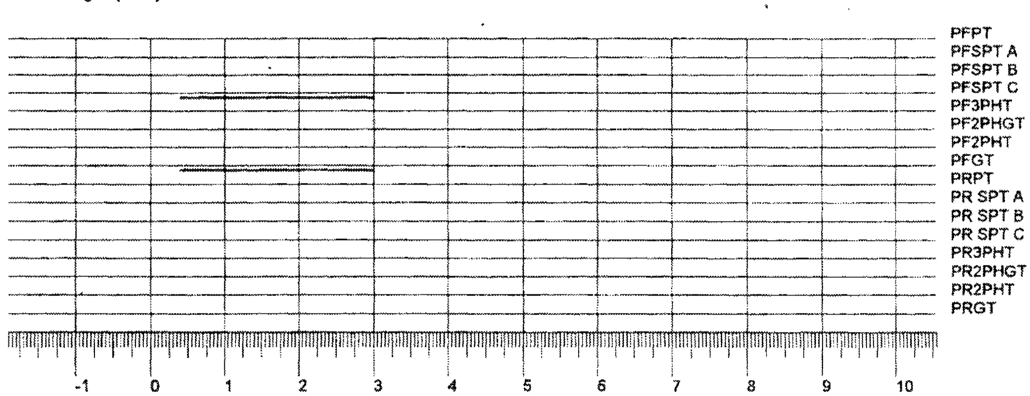


File: F3956r.rel (Lower Line)
File: F3956l.rel (Upper Line)
12/02/1997,-11:12:32.52174
MPS SOURCE 2
RIGHT BUS
B4 BREAKER

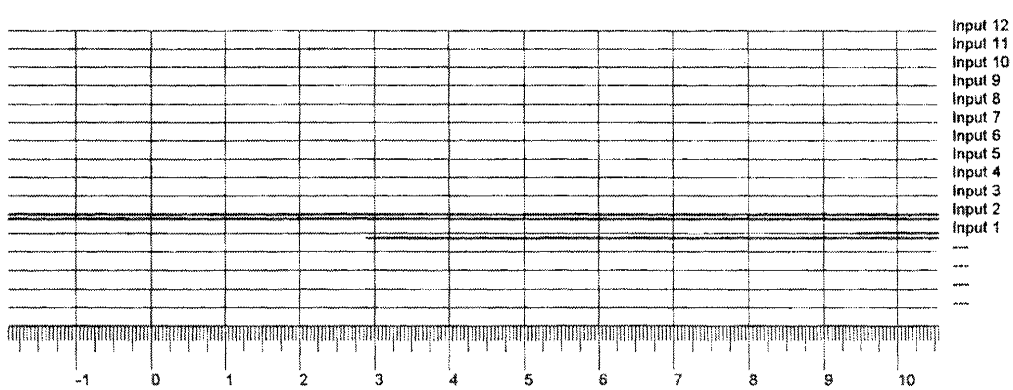
Zone 1 and High Set Logic (12)



Pilot Fwd/Rev Logic (13)

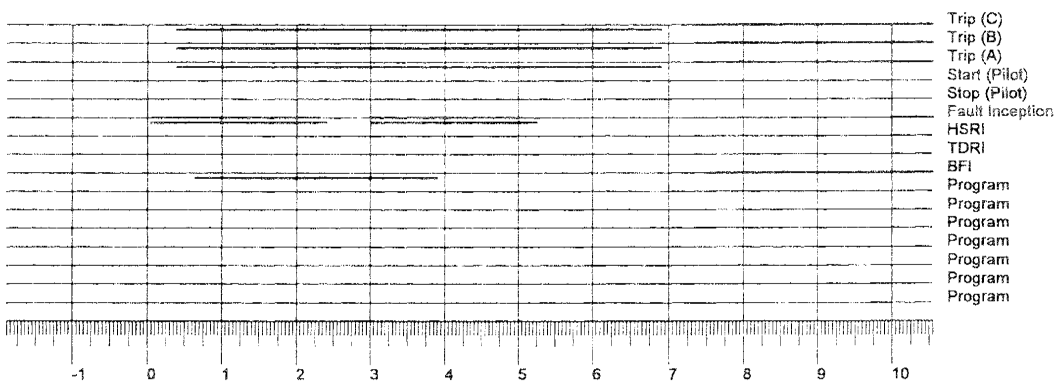


Digital Inputs (14)

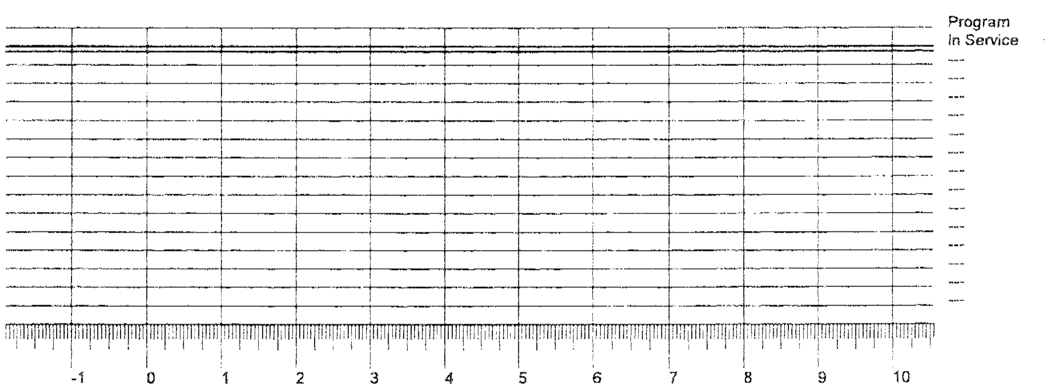


File: F3956r.rel (Lower Line)
File: F3956l.rel (Upper Line)
12/02/1997,-11:12:32.52174
MPS SOURCE 2
RIGHT BUS
B4 BREAKER

Digital Outputs (16)

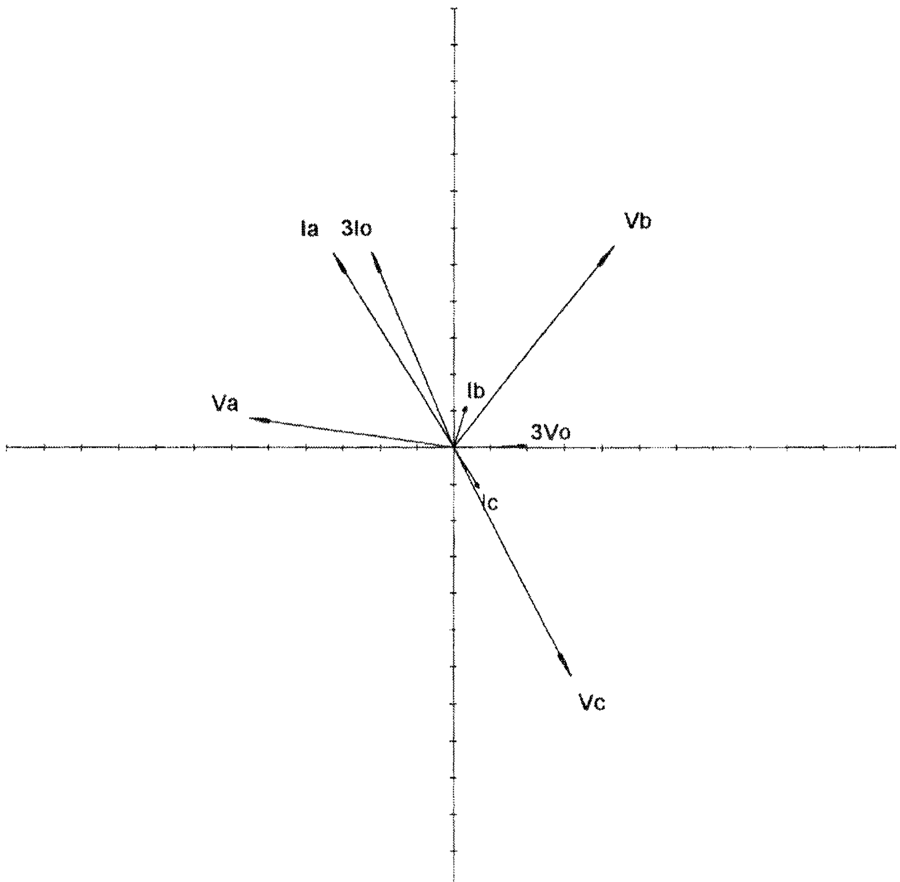


Digital Outputs (17)



File: F3956I.rel
12/02/1997,-11:11:21.17391

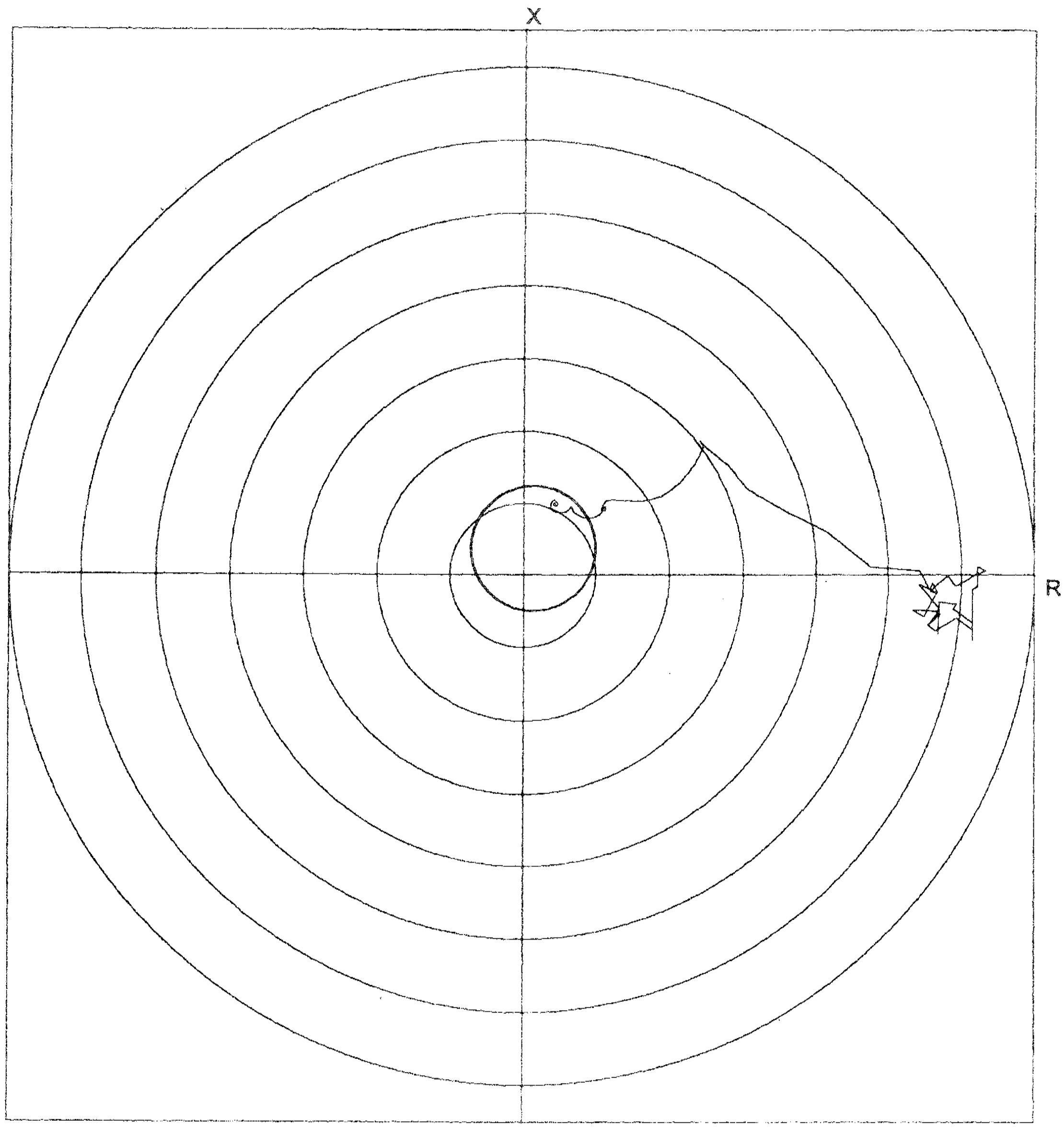
Cycle 02.550 to 03.500 (Scale: V x 1, I x 10)



PHASORS

Va = 055.6 < 172	Ia = 006.2 < 122
Vb = 070.0 < 052	Ib = 001.2 < 073
Vc = 070.1 < 297	Ic = 001.3 < 302
3Vo= 019.9 < 001	3Io= 005.8 < 113
	Ip = <

File: F3956I.rel
12/02/1997,-11:11:21.17391
MPS SOURCE 1
LEFT BUS
B9 BREAKER



Max. Impedance magnitude = 35 ohms
Grid Lines spaced at increments of 5 ohms.

Fault Type = AG
R = 2.1891 at sample 234
X = 4.6092 at sample 234

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ABB

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