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Comparison of CT Saturation Analysis Methods and DC Offset Factor "k" to Enhance CT Saturation Analysis

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By
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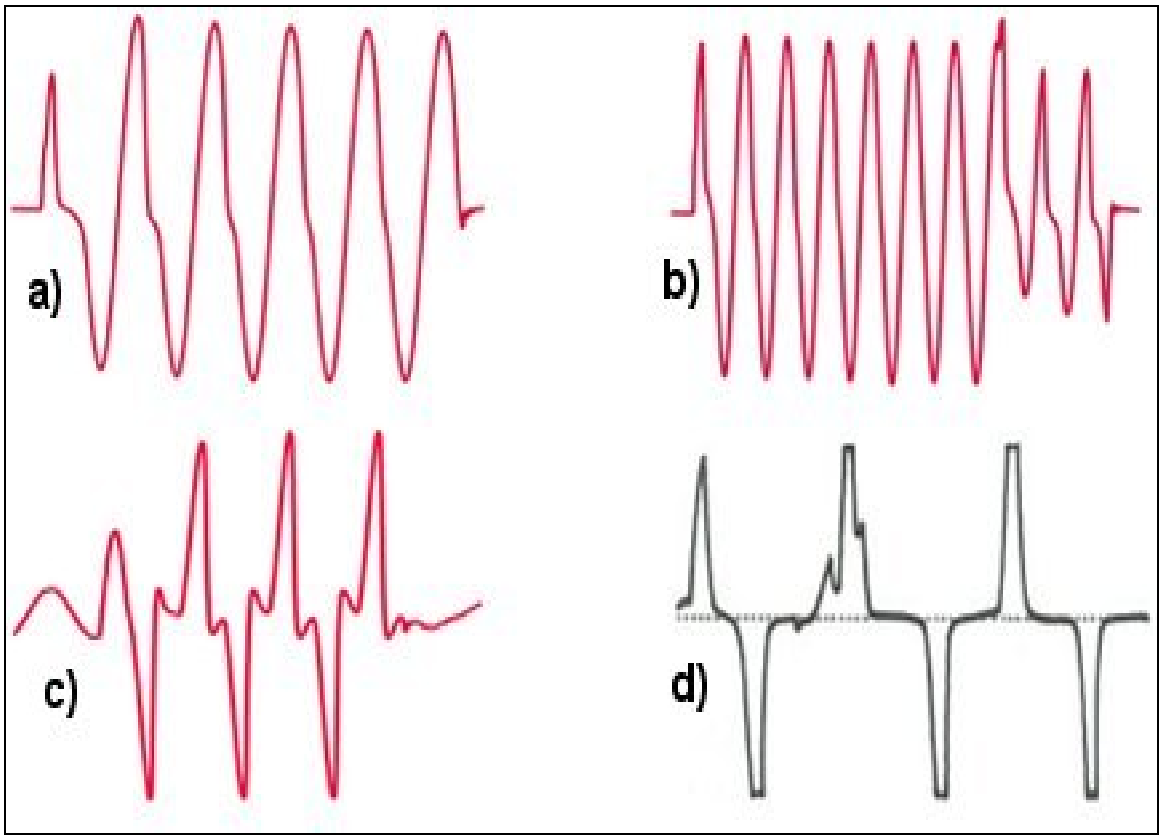
I. Introduction

In the old days (and even now for some), relay application engineers used to size current transformers based on the conventional Ohm's Law method with some margin of safety (typically, 30 – 50%). Even though the margin of safety was built in to accommodate system growth (or fault current increase) and DC offset, fault recordings shown in Figure 1 below indicate that those CTs may saturate under certain operating conditions. Definitely, CT saturation due to DC offset may have serious relaying impacts in the areas of fault detection, fault direction, fault type identification, fault location and fault clearing time.

These days, NERC/WECC reliability standards require relay application engineers to analyze all critical fault events and develop corrective action plans. In addition, ensuring timely and fast operation of all protective devices is getting more important to minimize arc flash hazards.

For the purpose of CT sizing and CT saturation analysis, there are two CT saturation analysis methods, **Ohm's Law method** and **volt time area method,** in our relaying industry. Based on the author's recent review of hundreds of real-life recordings and simulation results, the volt time area method appears to be much more accurate than the Ohm's Law method, but it may not be widely accepted by relay application engineers due to the potentially large volt time area multiplier (X/R + 1). Therefore, this paper is intended to address the following and document highlights of the author's findings:

- Fundamental differences or similarities between Ohm's Law method and volt time area method.
- Factors affecting CT saturation: CT accuracy, DC offset, system X/R ratio, fault current, CT burden, CT secondary x/r ratio, and remanent flux.
- Three (3) distinct shapes of saturated-CT waveforms: **chopped, decaying and flat-topped**.
- Defining X/R in cycles as **saturation recovery time**.
- **Half saturation recovery time** for relaying coordination purposes.
- Development of **DC offset factor "k"** and enhanced volt time area method: $(k \cdot X/R + 1) \cdot I_f \cdot Z_b \leq 20$ or $(k \cdot X/R + 1) \cdot I_f \cdot Z_s \leq V_s$
- Other application factors: CT connection, digital filtering, A/D converter saturation (at 109A, 154A, 174A, 224A, etc.) and peak detector.
- Corrective options.



a) Moderate saturation of a neutral CT due to DC offset.
b) Extreme saturation of the same neutral CT due to initial DC offset followed by additional remote breaker opening-caused DC offset.
c) Extreme saturation of a bus tie breaker CT due to DC offset, low CT accuracy and excessive fault current level.
d) Extreme saturation of an auto-transformer tertiary winding CT due to DC offset, excessive fault current level and low ratio CT tap. Clamping due to A/D converter saturation.

Figure 1. Distorted current waveforms due to CT saturation (*recorded by digital fault recorders*)

II. Comparison of Two CT Saturation Analysis Methods

As shown below, the Ohm's Law method and the volt time area method look alike except that the volt time area method has the additional volt time area multiplier, (X/R + 1), and uses 20 instead of V_b. Even though derivation of the volt time area method is quite different from the Ohm's Law method, the Ohm's Law method with inclusion of the volt time area multiplier, (X/R + 1), is practically the same as the volt time area method.

Ohm's Law Method	**Volt Time Area Method** [1]
$\mathbf{I_f \cdot Z_s \leq V_s}$ where: I_f is the maximum CT secondary current in amps. Z_s is the CT secondary impedance including the CT winding in ohms. V_s is the CT saturation voltage for a CT tap used in volts and **read from the excitation curve at 10 amps**.	$\mathbf{(X/R + 1) \cdot I_f \cdot Z_b \leq 20}$ where: I_f is the maximum fault current in p.u. of CT rating. Z_b is the CT burden in p.u. of standard burden. X/R is the X/R ratio of the primary fault current.
Application Notes: • Time to saturation should be taken into consideration for DC offset. • As a rule of thumb, $I_f \leq 75$ amps to accommodate DC offset and fault current increase in the future. • As a rule of thumb, $Z_s \leq$ adjusted secondary impedance for a specific tap used. • As a rule of thumb, $I_f \cdot Z_s \leq 0.75 \cdot V_s$ to accommodate burden increase in the future. • Some CTs meeting the Ohm's Law method have saturated under certain operating conditions. • It has been suggested recently that the volt time area multiplier should be used for certain applications, re-written as "$(X/R + 1) \cdot I_f \cdot Z_s \leq V_s$." [2][7]	**Application Notes:** • The volt time area multiplier, (X/R + 1), takes care of DC offset. • The standard burden does not include the secondary winding impedance. • CTs meeting the volt time area method will not saturate. • For a high X/R value, it may be impossible to find any CT meeting the above criteria. • The volt time area method can be re-written as "$(X/R + 1) \cdot I_f \cdot Z_b \leq V_b$" if I_f is defined as p.u. of 100 amps and V_b is defined as the CT burden voltage in p.u. of C-rated CT burden voltage.

III. Factors Affecting CT Saturation

3.1 CT Accuracy

In accordance with IEEE Std C57.13 [3],

- **Secondary terminal voltage rating for C-rated CT**: This is the voltage (*Note: Not the knee voltage*) the current transformer will deliver to a standard burden (1, 2, 4 and 8 ohms) at 20 times rated secondary current without exceeding 10 percent ratio correction. Furthermore, the ratio correction must be limited to 10

percent at any current from 1 to 20 times rated secondary current at the standard burden.

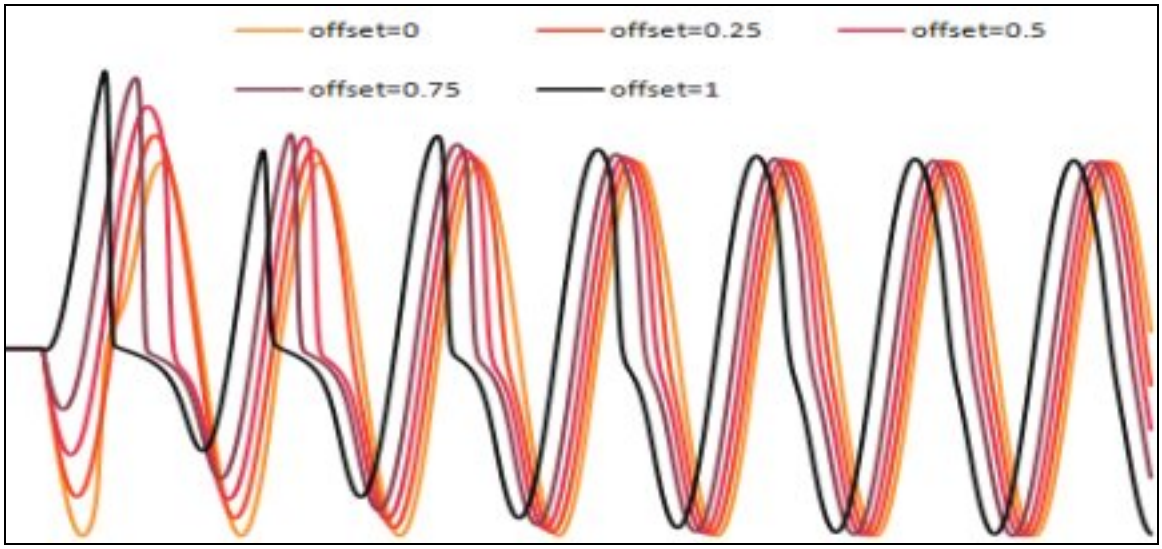
- **Standard burden**: Standard burdens (1, 2, 4 and 8 ohms) for current transformers with 5A-rated secondary current shall have resistance and inductance with 0.5 power factor or an impedance angle of 60 degrees.

Referring to Figure 5, the above secondary terminal voltage for C-rated CT is the burden voltage V_b, which is different from the secondary exciting voltage or saturation voltage V_s. Based on the above, **the secondary exciting or saturation voltage V_s can be read directly from the excitation curve at 10 amps of excitation current and then V_b is calculated by subtracting the internal winding voltage drop from V_s.**

3.2 DC offset and its impacts on CT saturation

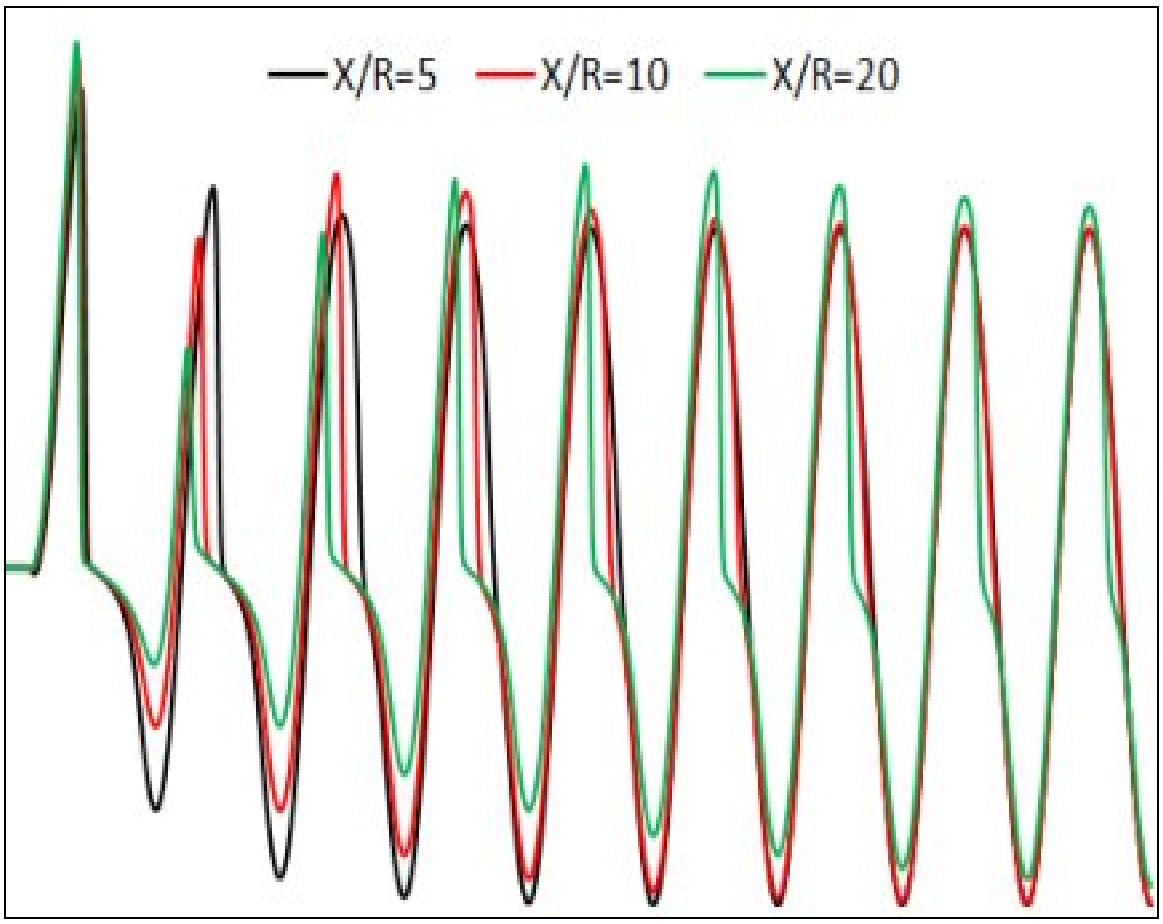
Figure 2 graphically illustrates impacts of DC offset magnitude variation, based on the author's simulation, and noteworthy highlights of the simulation are:

- The higher the DC offset level is, the worse the CT saturation is.
- The higher the DC offset level is, the bigger the peak value of 1st-half-cycle current is. This indicates that the peak detector may be an effective means of instantaneous fault detection in case of extreme CT saturation.
- DC offset is practically 0 at the point of X/R in cycles (or 2π times DC offset time constant) for all cases. (*Note: The X/R in cycles is defined later in Section 3.9 as saturation recovery time.*)



(*Note: For the above case studies, V_s=400, N=240, I_f=100A secondary, system X/R=8, Z_b=R_b=2.5 ohms, and no remanent flux are assumed.*)

Figure 2. Waveforms illustrating impacts of DC offset magnitude variation (*simulated results*)



(*Note: For the above case studies, V_s=400, N=240, I_f=100A secondary, DC offset=1, Z_b=R_b=2.5 ohms, and no remanent flux are assumed*.)

Figure 3. Waveforms illustrating impacts of system X/R ratio variation (*simulated results*)

3.3 System X/R ratio and its impacts on CT saturation and saturation recovery time

Figure 3 graphically illustrates the impacts of system X/R ratio variation, based on the author's simulation, and noteworthy highlights of the simulation are:

- The higher (or more inductive) the system X/R ratio is, the worse the CT saturation is.
- The volt time area method, $(X/R + 1)\cdot I_f \cdot Z_b \leq 20$, implies that CT saturation of X/R=20 is almost 4 times worse than X/R=5. However, as illustrated in Figure 3, it is not mathematically obvious.

- The higher (or more inductive) the system X/R ratio is, the bigger the peak value of 1st-half-cycle current is. This indicates that the peak detector may be an effective means of instantaneous fault detection in case of extreme CT saturation.
- DC offset is practically 0 at the point of X/R in cycles (or 2π times time constant) for all cases. (*Note: The X/R in cycles is defined later in Section 3.9 as saturation recovery time*.)

In the volt time area method, $(X/R + 1)\cdot I_f Z_b \leq 20$, X/R is the DC offset-caused volt time area multiplier and it has significant impacts on CT saturation because it can be a very large number as shown below [4]:

System Components	**X/R Ratio Ranges**	**Typical X/R Ratio Values**
Large generators and hydrogen-cooled synchronous condensers	40 – 120	80
Power transformers	10 – 50	15 - 25
Induction motors	5 – 35	
Small generators and synchronous motors	20 – 35	
Reactors	40 – 120	80
Open conductor lines	2 – 16	5
Underground cables	1 – 3	2

3.4 Fault current decrement and increment

It is known that fault currents decrease over time, but can also increase over time if a high initial response (HIR) excitation system is in use, as explained below:

- An excitation system has an HIR characteristic if it can force its output voltage from the rated voltage to the ceiling voltage within 0.1 second or less. A typical brushless exciter is not an HIR excitation system, but it is usually faster than other types of rotating exciters. A static excitation system is inherently an HIR excitation system.
- In general, the exciter ceiling voltage may range 1.5 to 5 times rated field voltage even though the stator voltage range is much smaller due to core saturation.
- In general, the over-excitation limiter (OEL) is time-delayed by 1 to 30 seconds (*e.g., 1 second time delay for 58MVA steam-turbine generator brushless excitation system, 30 seconds time delay for 25MVA hydro-generator static excitation system, etc.*).

- After the inception of a fault, the fault current starts decaying. In 0.1 second or less, the fault current will sharply increase due to HIR, remain high for the OEL time delay duration, and then decrease due to the OEL. (*Note: In reality, the power system stabilizer is likely to lower the field voltage before the OEL does*.)

In general, the fault current decrement or increment may not be noticeable at transmission switching stations and distribution substations, but it should be taken into consideration at generating stations for time-delayed relaying schemes.

3.5 CT secondary x/r ratio and its impacts on the shape of saturated-CT waveforms (3 distinct signatures: chopped, decaying, and flat-topped)

Figure 4 graphically illustrates a CT equivalent circuit and vector representation of various currents and voltages, especially the angular difference between the magnetizing current I_M and the secondary burden current I_S. For the resistive burden, the angular difference is close to 90 degrees and it is 0 for the inductive burden.

Figures 5 and 6 graphically illustrate the impacts of CT secondary x/r ratio variation, based on the author's simulation, and noteworthy highlights of the simulation are:

- For the resistive burden (e.g., X_b=0), the angular difference between the magnetizing current and the secondary burden current is approximately 90 degrees. If a CT with the resistive burden saturates, the secondary burden current has a **chopped** wave characteristic.
- For the inductive burden (e.g., r_b=0), the angular difference is approximately 0 and the saturated secondary burden current has a **flat-topped** wave characteristic. It is important to recognize that there are two inductive circuits in parallel (e.g., CT magnetizing circuit and inductive burden circuit) and the secondary burden current is also the magnetizing current of the inductive burden.
- For the mixed burden such as x/r=1, the angular difference is approximately 45 degrees and the saturated secondary burden current has a **decaying** wave characteristic.

In general, the current time area of the inductive burden is actually larger than that of the resistive burden. Therefore, it is justified to use the volt time area method for all burden types without sacrificing any accuracy even though the volt time area method was primarily developed for the resistive burden.

It is interesting to note that the current time area of the inductive burden is actually larger than that of the resistive burden, which means that electromechanical relays may see more current than digital relays. Why don't digital relay manufacturers make the current input circuit inductive?

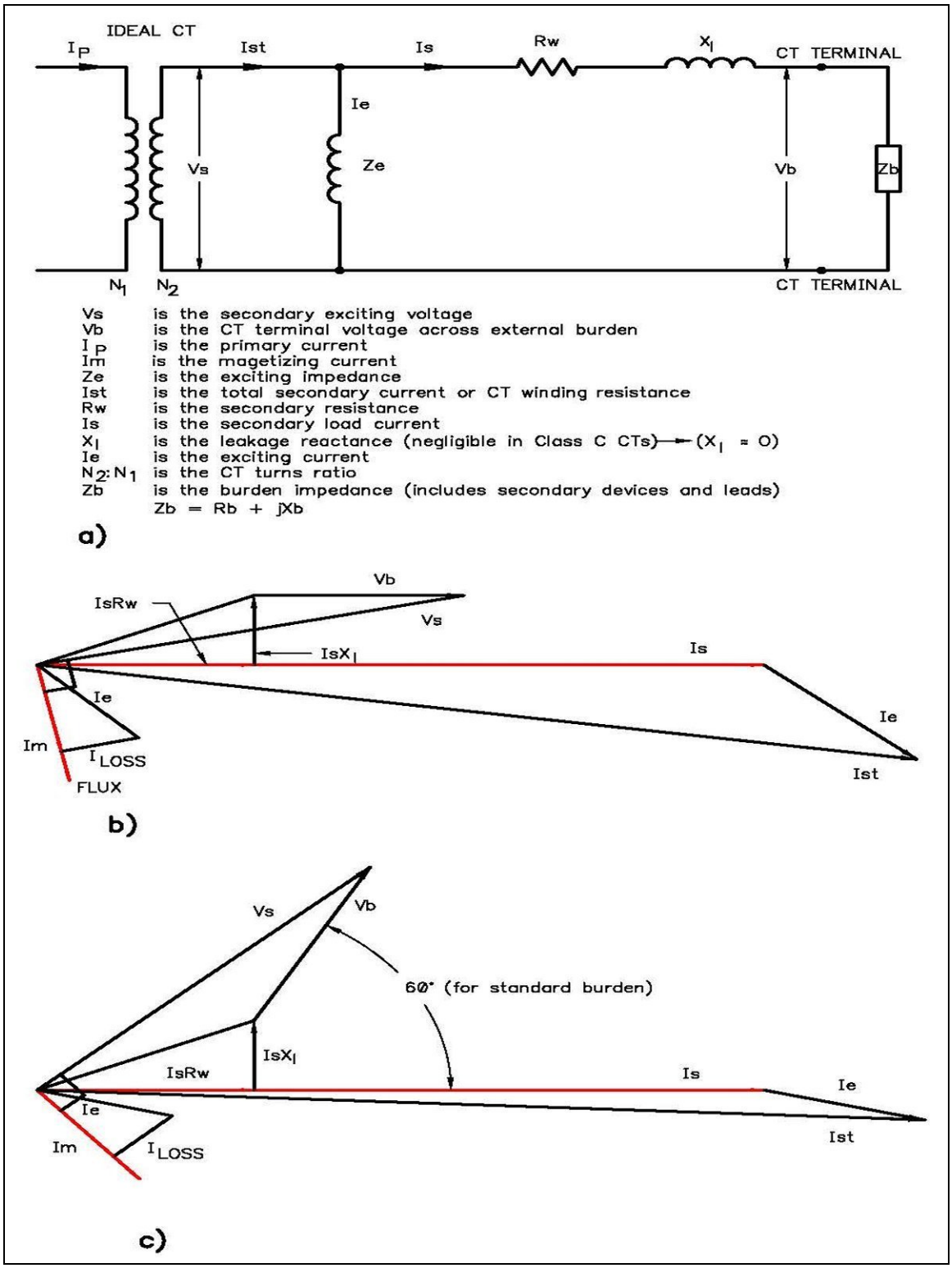
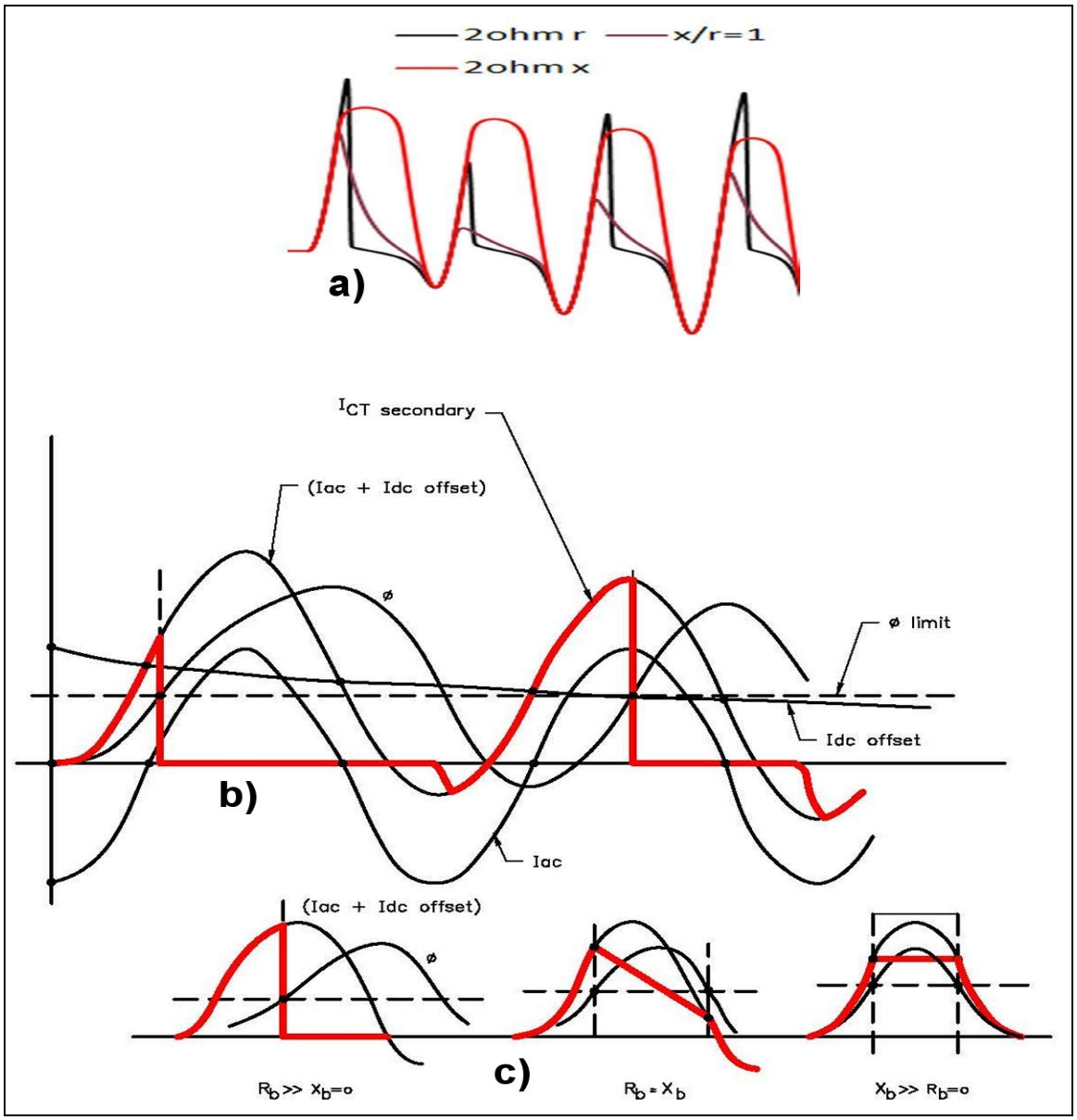
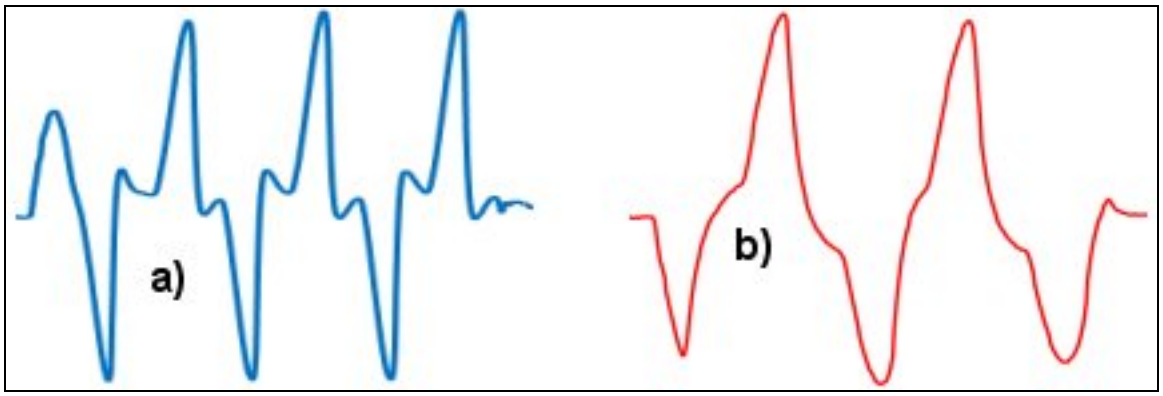


Figure 4. CT equivalent circuit and vector representation (*similar to Figures 1 – 3 in IEEE Std C37.110* [2] *and Figure 5-1 in Applied Protective Relaying* [5])



a) Simulated wave shape variation: **chopped** for 2ohm resistive burden, **decaying** for 2ohm x/r=1 burden, and **flat-topped** for 2ohm inductive burden. The more inductive the burden is, the bigger the current time area is. (*Note: For the above case studies, V_s=400, N=240, I_f=200A secondary, system X/R=20, DC offset=1 and no remanent flux are assumed*.)
b) Hand-sketched secondary current waveform for resistive burden.
c) Hand-sketched wave shape variation. Notice that the wave shape is dictated by the angular difference between (I_{ac} + I_{dc} offset) and Φ.

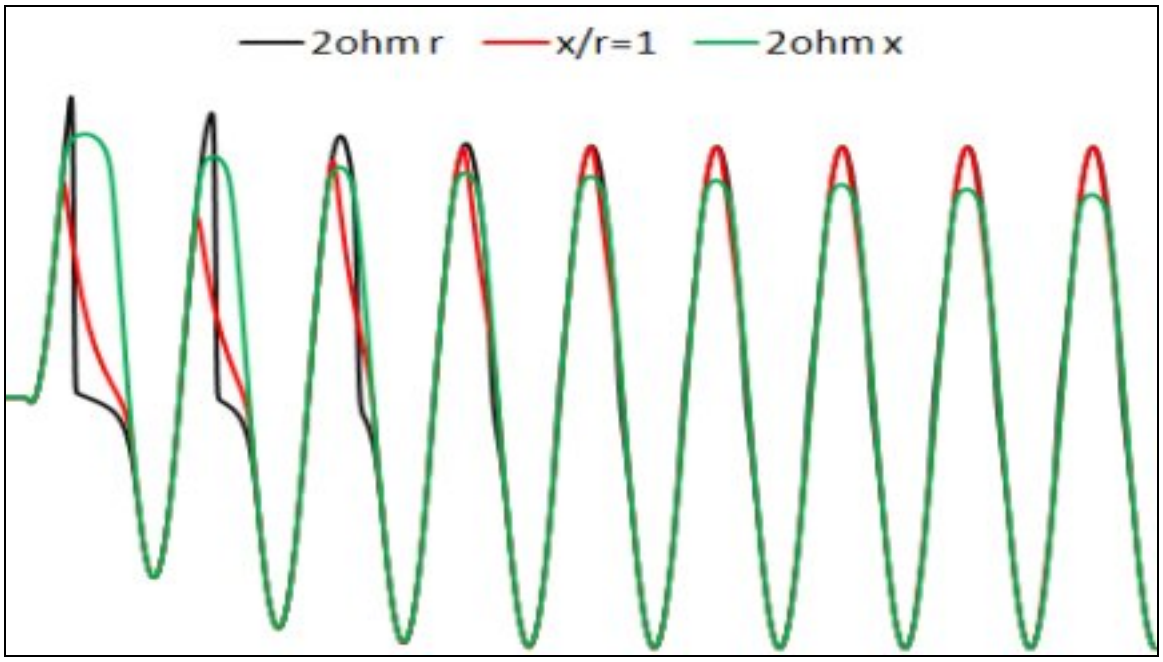
Figure 5. Illustration of 3 distinct wave shapes (chopped, decaying and flat-topped) due to CT secondary X/R ratio variation (*simulated and hands-sketched results*)



a) Chopped saturated-CT waveform: digital relay ($x \approx 0$).
b) Decaying saturated-CT waveform: electromechanical relay ($x \neq 0$ but $x/r < 1$)

Figure 6. Illustration of "**chopped**" and "**decaying**" saturated-CT waveforms (*recorded by digital fault recorders*)

3.6 CT secondary x/r ratio and its impacts on saturation recovery time



(*Note: For the above case studies, V_s=400, N=240, I_f=200A secondary, system X/R=5, DC offset=1, Z_b=2 ohms and no remanent flux are assumed.*)

Figure 7. Illustration of impacts of CT secondary X/R ratio variation (*simulated results*)

Figure 7 graphically illustrates impacts of the CT secondary x/r ratio variation, based on the author's simulation, and noteworthy highlights of the simulation are:

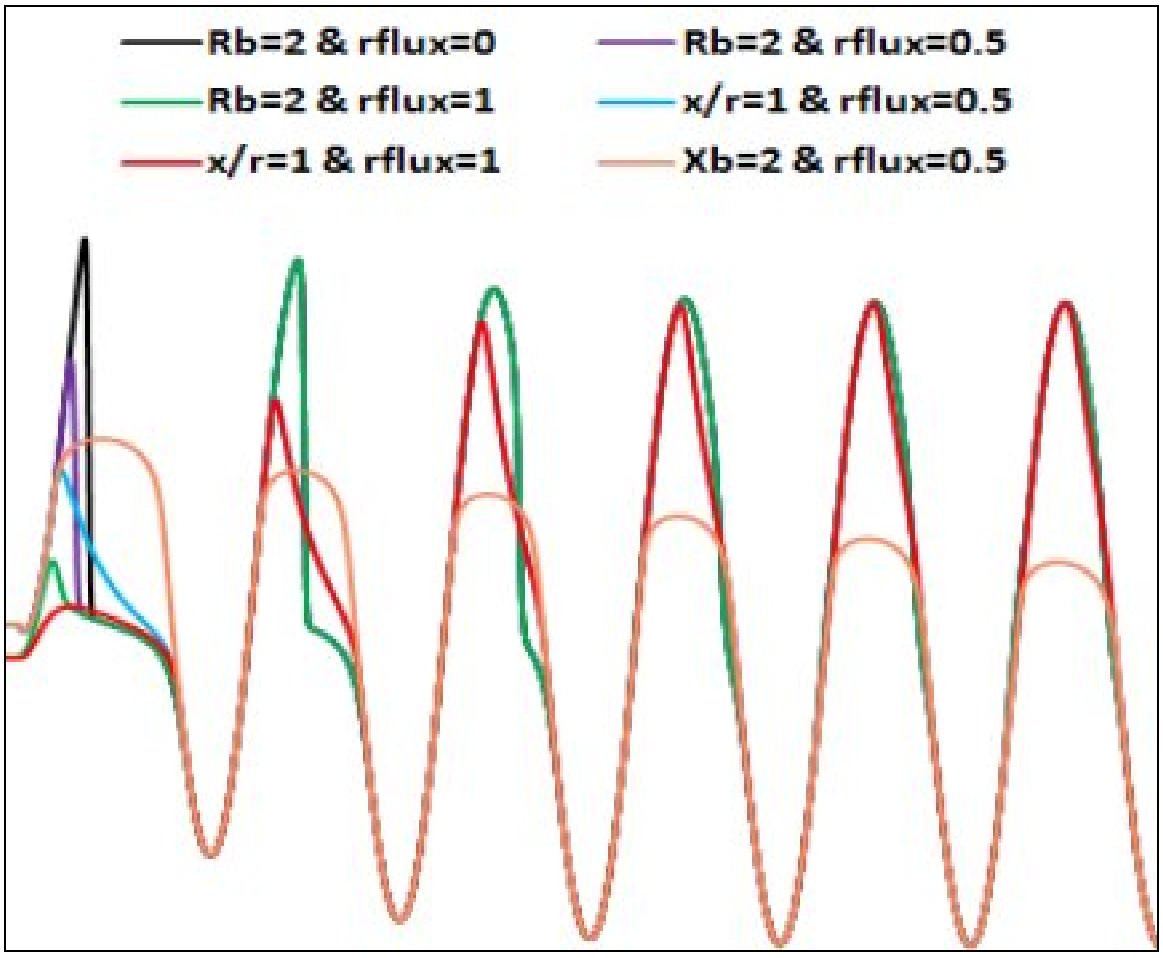
- DC offset is practically 0 at the point of X/R in cycles (or 2π times time constant) for all cases. Therefore, CT secondary x/r ratio's impacts on saturation recovery time are negligible. (*Note: The X/R in cycles is defined later in Section 3.9 as saturation recovery time*.)
- The higher (or more inductive) the CT secondary x/r ratio is, the bigger the current time area is.
- The smaller (or more resistive) the CT secondary x/r ratio is, the bigger the peak value of 1st-half-cycle current is.
- For the 2ohm inductive burden, the positive current time area gradually decreases over time even though the negative peak envelope indicates that DC offset is practically 0 at the point of X/R in cycles.

3.7 Remanent flux of CT and its impacts on CT saturation recovery time

Figure 8 graphically illustrates remanent flux variation and its impacts on saturation recovery time, based on the author's simulation, and noteworthy highlights of the simulation are:

- The higher the remanent flux level is, the worse the CT saturation is.
- In general, the remanent flux impacts are noticeable but only last 1 to 2 cycles.
- The higher (or more inductive) the CT secondary x/r ratio is, the bigger the current time area is.
- The smaller (or more resistive) the CT secondary x/r ratio is, the bigger the peak value of 1st-half-cycle current is.
- DC offset is practically 0 at the point of X/R in cycles (or 2π times time constant) for all cases. Therefore, CT remanent flux's impacts on saturation recovery time are negligible. (*Note: The X/R in cycles is defined later in Section 3.9 as saturation recovery time*.)
- For the 2ohm inductive burden, the positive current time area gradually decreases over time even though the negative peak envelope indicates that DC offset is practically 0 at the point of X/R in cycles.

It is interesting to note that CT remanent flux does not increase the saturation recovery time very much and, in fact, the saturation recovery time is really dictated by the system X/R ratio.



(*Note: For the above case studies, V_s=400, N=240, I_f=200A secondary, system X/R=5, DC offset=1 and Z_b=2 ohms are assumed*.)

Figure 8. Waveforms illustrating impacts of remanent flux variation (*simulated results*)

3.8 Saturation recovery time

Mathematically, the time constant of $e^{\frac{-Rt}{L}}$ is L/R in seconds, but the time constant expressed in cycles is more intuitive to relay application engineers.

$$\text{Time Constant} = \frac{L}{R} \text{ seconds} = \frac{fL}{R} \text{ cycles}$$

$$\therefore \frac{X}{R} = 2\pi \cdot \frac{fL}{R} \text{ cycles} = 2\pi \cdot (\text{Time Constant in cycles})$$
$$= 6.28 \cdot (\text{Time Constant in cycles})$$

For exponentially decaying DC offset current, the resulting magnitudes are:

26.8%	at the point of 1 times time constant
7.2%	at the point of 2 times time constant
1.9%	**at the point of 3 times time constant**
0.5%	at the point of 4 times time constant
0.14%	at the point of 5 times time constant
0.04%	at the point of 6 times time constant

In general, it has been a widely accepted concept that the resulting magnitude of exponential decaying is 0 at the point of 5 times time constant. Therefore, it is justified to consider the "5 times time constant" as DC offset recovery time.

As illustrated in Figures 2, 3, 7 and 8, DC offset is practically 0 at the point of X/R in cycles (or 2π times time constant), the remanent flux's impacts on DC offset recovery time are negligible, and also the high CT secondary x/r ratio's impacts on DC offset recovery time are negligible. Definitely and intuitively, high secondary x/r ratio and remanent flux are supposed to slow down the exponential decaying. However, based on the author's simulation, the exponential decaying is largely dictated by the system X/R ratio.

Based on all the above theories and simulation results, the author would like to define "**system X/R in cycles as saturation recovery time**" even though the author strongly recommends using the **half saturation recovery time** (or 50% of the saturation recovery time = π times time constant = $\frac{1}{2} \cdot$ X/R in cycles) for relaying coordination purposes. At the half saturation recovery time, DC offset should be practically 0 or below 1.9%. If DC offset is a primary cause of CT saturation, the half saturation recovery time can be used for relaying coordination purposes as described below:

- Delay the instantaneous operation by the half saturation recovery time if feasible.
- Increase the coordinating time interval by the half saturation recovery time if feasible.

Delaying may increase the arc-flash hazard, so it may not be feasible in certain applications even though it is a very inexpensive solution for most DC offset-caused CT saturation problems.

3.9 Saturated-CT waveform analysis

As presented so far, CT saturation factors essential to size CTs and also to analyze saturated-CT waveforms are:

- CT accuracy rating
- DC offset
- System X/R ratio

- Saturation recovery time
- Fault current decrement and increment
- CT burden
- CT secondary x/r ratio-dependent wave shape
- Remanent flux
- A/D converter saturation (*explained later in Section 5.1*)

Figure 9 graphically illustrates how the above factors along with the volt time area method can be used to systematically analyze saturated-CT waveforms and also to develop corrective action plans.

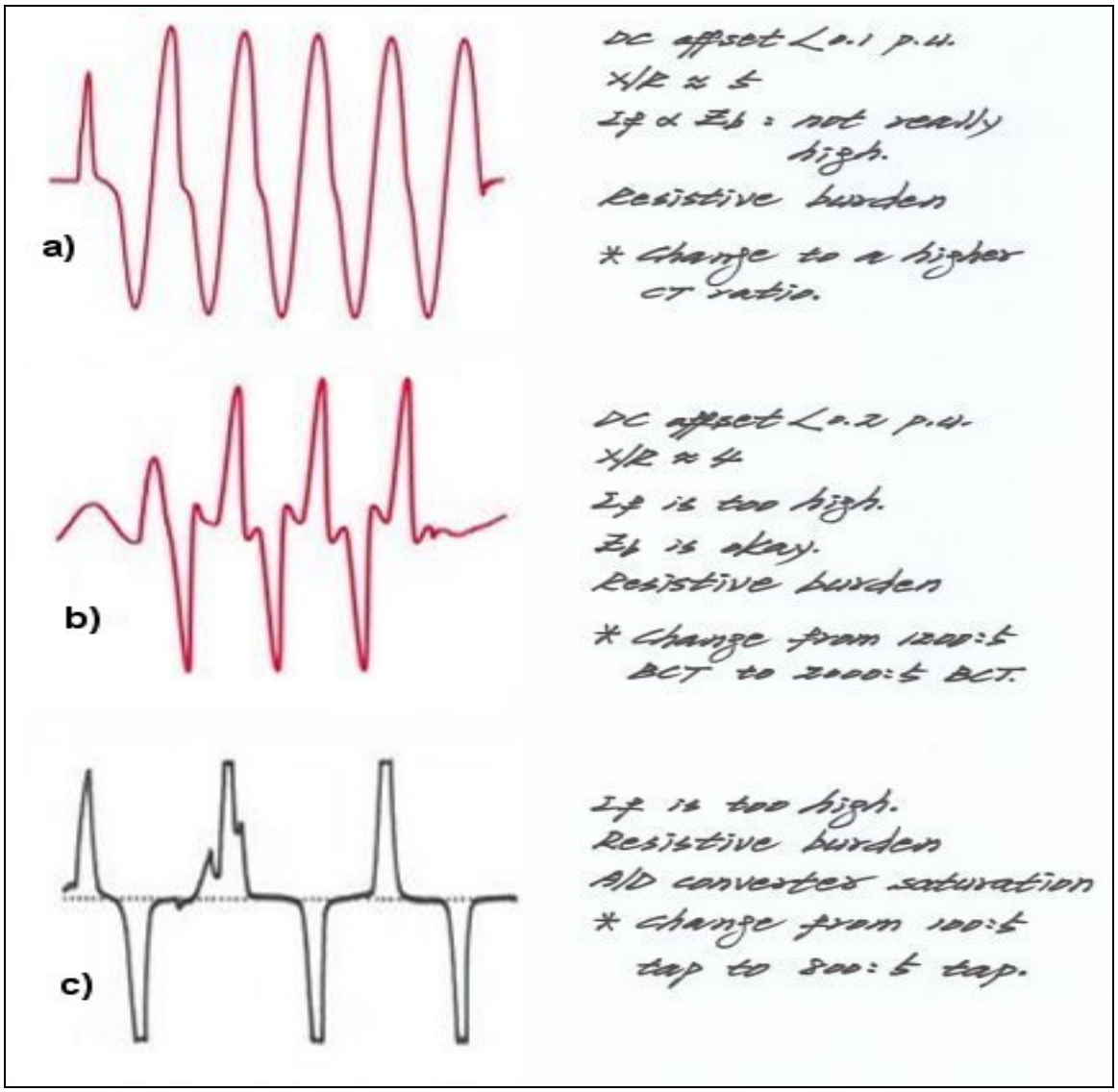


Figure 9. Iillustration of CT saturation analysis by using the volt time area method (*hand-written notes*)

IV. Development of DC Offset Factor "k"

4.1 Volt time area multiplier, (X/R + 1)

Derivation of the volt time area method is described in details in Stan Zocholl's Analyzing and Applying Current Transformers [1], but it is re-written here due to the importance of understanding it thoroughly and also due to the author's proposed enhancement of the volt time area method with inclusion of the DC offset factor "k."

(Burden Voltage) $\propto$ (Core Turn) $\cdot$ (Core Flux Rate of Change)

$V \propto N \cdot (d\Phi/dt)$

$N \cdot \Phi \propto N \cdot \{$(Flux Density) $\cdot$ (Core Cross-sectional Area)$\} = N \cdot (B \cdot A)$
$= \int_0^t V\,dt$

(Burden Voltage) $\propto$ (CT Secondary Fault Current) $\cdot Z_b = I_f \cdot Z_b$
$= (I_{dc\ offset} + I_{ac}) \cdot Z_b = \left[I_f \cdot \{e^{\frac{-Rt}{L}} - \cos(\omega t)\}\right] \cdot Z_b$

where $\frac{L}{R}$ = time constant.

Volt Time Area $= \int_0^t V\,dt = I_f \cdot Z_b \cdot \int_0^t \{e^{\frac{-Rt}{L}} - \cos(\omega t)\}\,dt$

$N \cdot B \cdot A \cdot \omega = \left[I_f \cdot Z_b \cdot \int_0^t \{e^{\frac{-Rt}{L}} - \cos(\omega t)\}\,dt\right] \cdot \omega$
$= I_f \cdot Z_b \cdot \left[(-\frac{\omega L}{R}) \int_0^t e^{\frac{-Rt}{L}} (\frac{-R}{L})\,dt - \int_0^t \cos(\omega t)\ \omega\,dt\right]$
where the limit of $\left[(-\frac{\omega L}{R}) \int_0^t e^{\frac{-Rt}{L}} (\frac{-R}{L})\,dt\right]$ is $\frac{X}{R}$ and the limit of $\left[-\int_0^t \cos(\omega t)\ \omega\,dt\right]$ is 1.

$\therefore$ **$N \cdot B \cdot A \cdot \omega = (\frac{X}{R} + 1) \cdot I_f \cdot Z_b$**

As shown above, (X/R + 1) is the volt time area multiplier and X/R represents the DC offset-caused volt time area multiplier. The volt time area multiplier, (X/R + 1), implies that CT saturation of X/R=20 is almost 4 times worse than X/R=5. However, it is not mathematically obvious, as illustrated in Figure 3.

4.2 DC offset of naturally occurring faults

Figure 10 graphically illustrates fundamentals of DC offset which is the primary cause of CT saturation as shown in the volt time area method, $(X/R + 1)\cdot I_f \cdot Z_b \leq 20$, in which X/R represents the DC offset-caused volt time area multiplier. It illustrates that the theoretical DC offset peak can be as high as the peak of the sinusoidal fault current waveform.

Based on theories of insulation breakdown in high-voltage engineering, a fault or insulation breakdown occurs if the applied voltage across the insulation exceeds the insulation gap's electrical strength. Therefore, a naturally occurring fault is supposed to occur at or near the peak of voltage. Figure 10 illustrates that the maximum DC offset occurs at 0 voltage but no DC offset occurs at the voltage peak.

The theories also imply, "the higher the X/R ratio is, the smaller the DC offset is" because the current peak does not occur at 0 voltage for the low X/R ratio. However, fault recordings do not substantiate it.

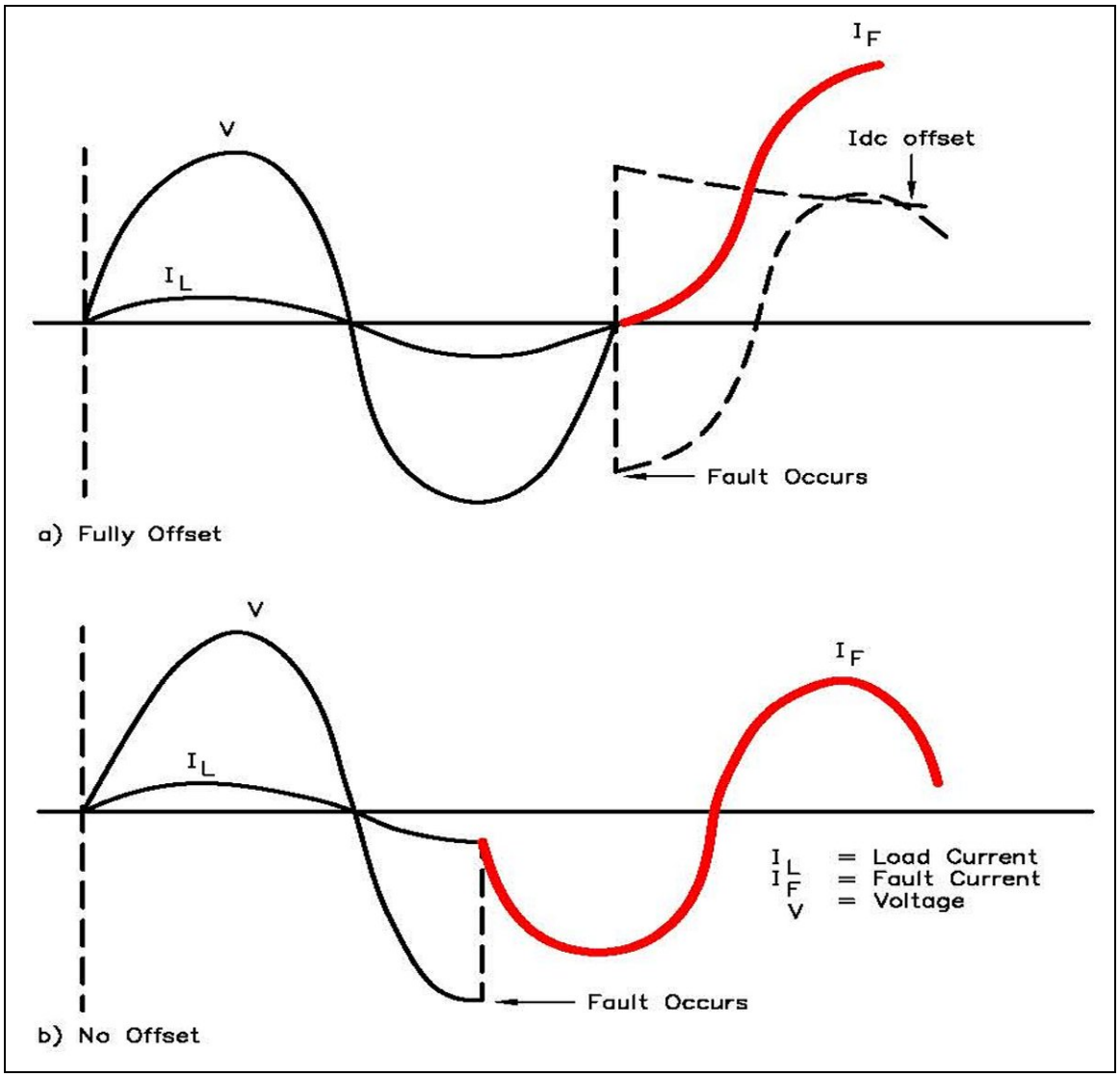
Over the past several years the author analyzed hundreds of short circuit faults, especially from the DC offset aspect, and concluded that naturally occurring short-circuit faults occur at or near the peak of voltage. Some short-circuit fault waveforms recorded by digital fault recorders are shown in Figures 11, 12 and 13.

Noteworthy highlights of the fault waveforms are:

- For SLG faults, all short-circuit faults except one (Figure 11.b) occurred at or near the voltage peak. Most DC offset values were 0.25 p.u. or smaller.
- Figure 11.b) illustrates that a SLG fault occurred at approximately 50% of the voltage peak and the corresponding DC offset was 0.33 p.u.
- For LL faults, all short-circuit faults occurred at or near the voltage peak of one phase. All DC offset values were 0.25 p.u. or smaller.
- For 3LG faults, all short-circuit faults occurred at or near the voltage peak of one phase. The worst DC offset value as shown in Figure 13.a) was 0.4 p.u.
- Referring to Figure 1.b), a series of DC offsets (one DC offset followed by another DC offset due to remote breaker tripping) may result in higher DC offset and more extreme CT saturation.

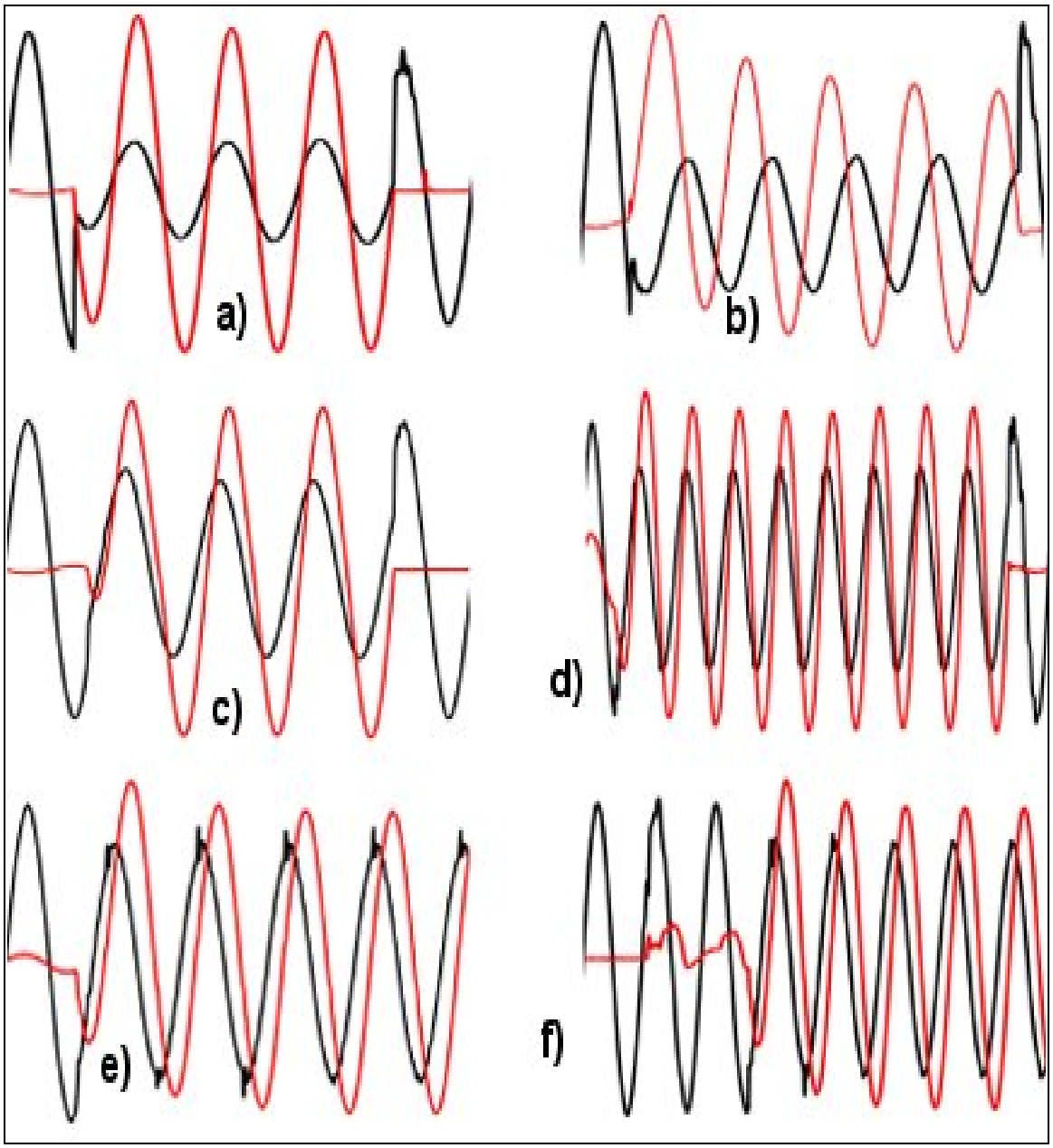
Based on the above highlights, **DC offset rarely exceeds 0.25 p.u. for all naturally occurring faults, especially SLG and LL faults**. Therefore, for the purpose of CT saturation evaluation, using a DC offset of 1 p.u. is unrealistic and so DC offset of 0.25 p.u. instead of 1 p.u. should be used as the practical worst-case DC offset.

Figure 11.e) represents a tree-caused SLG fault and Figure 11.f) represents a second or subsequent SLG fault upon reclosing. It is interesting to see that the second fault occurred right at the voltage peak in 2 cycles after breaker reclosing. It really verifies the insulation breakdown theory in which a fault or insulation breakdown occurs if the applied voltage across the insulation exceeds the insulation gap's electrical strength.



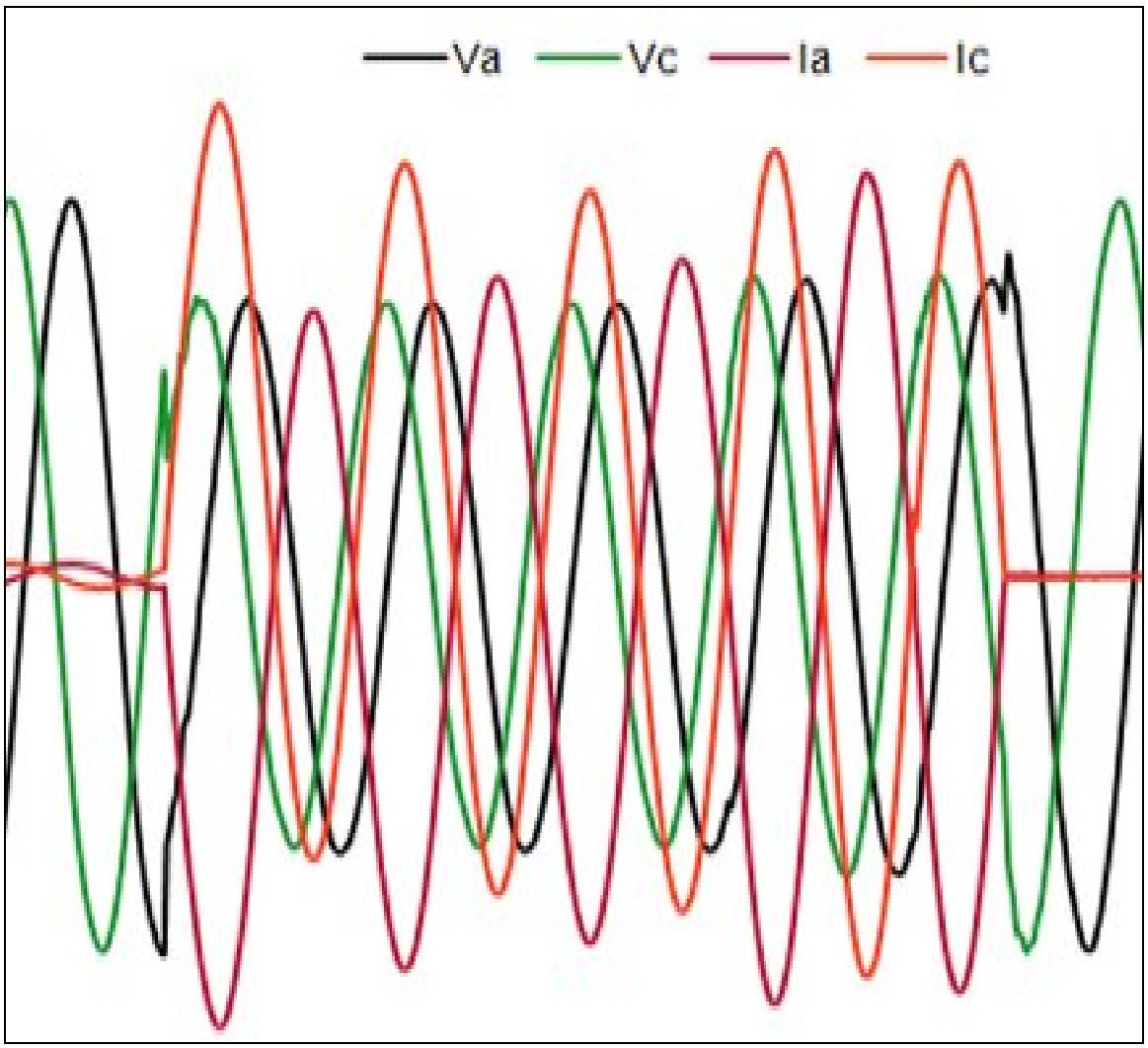
a) Maximum DC offset (1 p.u. being the peak of I_f) when a fault occurs at V=0.
b) No offset when a fault occurs at the voltage peak.
(*Note: For simplicity and illustration purposes, an impedance angle of 90 degrees or purely inductive circuit is assumed.*)

Figure 10. Fundamentals of DC offset (*hand-sketched and similar to Figure 5-8 in Applied Protective Relaying* [5])



a) Fault right at the voltage peak and corresponding DC offset ≈ 0.12 p.u.
b) Fault at approximately 50% of the voltage peak and corresponding DC offset ≈ 0.33 p.u.
c) Fault near the voltage peak and almost no DC offset.
d) Fault right at the voltage peak and corresponding DC offset ≈ 0.14 p.u.
e) 1st fault right at the voltage peak and corresponding DC offset ≈ 0.2 p.u.
f) 2nd fault right at the voltage peak even in 2 cycles after breaker reclosing and corresponding DC offset ≈ 0.2 p.u..

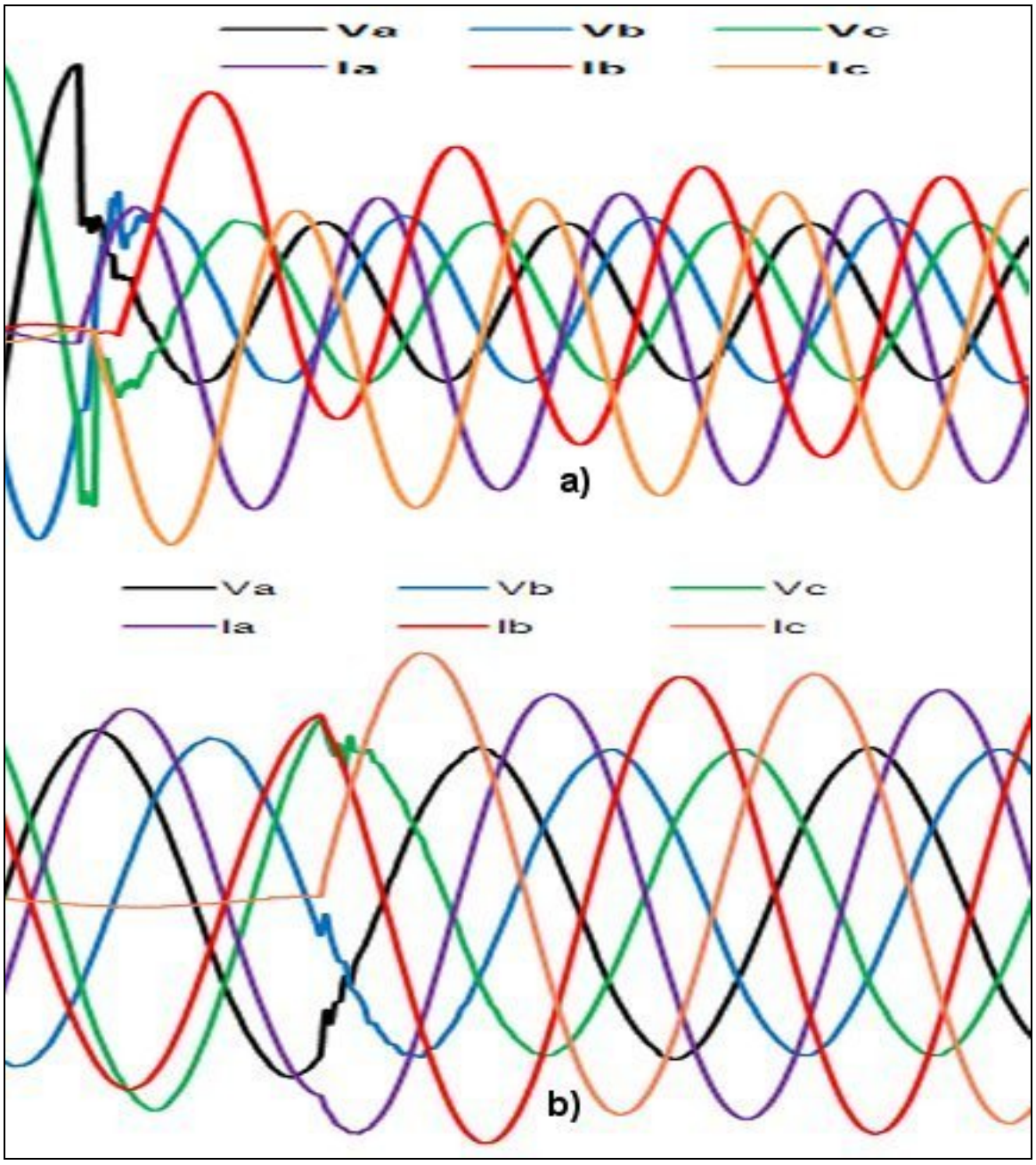
Figure 11. Naturally occurring single-line-to-ground fault waveforms with DC offset (*recorded by digital fault recorders*)



- Fault right at the a-phase voltage peak and at 50% of the c-phase voltage peak.
- Corresponding DC offset ≈ 0.19 p.u. for both a-phase and c-phase.

Figure 12. Naturally occurring line-to-line fault waveforms with DC offset (*recorded by a digital fault recorder*)

Previously, it was stated that all short-circuit faults occurred at or near the voltage peak of one phase. It is true, but it is more accurate to say that all multi-phase short-circuit faults occurred at or near the line-to-line voltage peak, referring to Figures 12 and 13.



a) Fault at the a-phase voltage peak, 50% of the b-phase voltage peak and 87% of the c-phase voltage peak. Corresponding a-phase DC offset ≈ 0.14 p.u., b-phase DC offset ≈ 0.4 p.u. and c-phase DC offset ≈ 0.2 p.u.
b) Evolving fault resulting in the fault type transition from a-to-b LL to 3LG. Even for this evolving fault case, the c-phase fault inception occurred near the c-phase voltage peak. Corresponding c-phase DC offset ≈ 0.08 p.u.

Figure 13. Naturally occurring 3-phase fault waveforms with DC offset (*recorded by digital fault recorders*)

4.3 DC offset factor "k" and enhanced volt time area method

As determined in Section 3.5, the current time area of the inductive burden is actually larger than that of the resistive burden. Therefore, it is justified to use the volt time area method for all burden types without sacrificing any accuracy even though the volt time area method was primarily developed for the resistive burden.

As determined in Section 4.2, it clearly appears that using a DC offset of 1 p.u. is unrealistic and unsubstantiated. Definitely, it is necessary to make the DC offset value more realistic. Therefore, based on all the theories, a review of real-life fault waveforms, and research results, the author would like to propose the following **enhanced volt time area method**:

$$(k \cdot X/R + 1) \cdot I_f \cdot Z_b \leq 20$$ if p.u. values are used as shown in Stan Zocholl's Analyzing and Applying Current Transformers.

Where: k is the DC offset factor (0 – 1.0).
I_f is the maximum fault current in p.u. of CT rating.
Z_b is the CT burden in p.u. of standard burden.
X/R is the X/R ratio of the primary fault current.

Or

$$(k \cdot X/R + 1) \cdot I_f \cdot Z_s \leq V_s$$ if amps, volts and ohms are used.

$$(0.25 \cdot X/R + 1) \cdot I_f \cdot Z_s \leq V_s$$ if k=0.25 is used for all practical purposes.

Where: k is the DC offset factor (0 – 1.0).
I_f is the maximum CT secondary current in amps.
Z_s is the CT secondary impedance including the CT winding in ohms.
V_s is the CT saturation voltage for the CT tap used, in volts, and can be read from the excitation curve at 10 amps of excitation current.

4.4 Application notes for enhanced volt time area method

In addition to CT saturation factors mentioned earlier, the following application notes are essential to properly apply the enhanced volt time area method:

- **Practical meaning of X/R ratio** – Mathematically, the limit of DC offset burden voltage integration is X/R p.u. and it is reached in X/R cycles, but the limit of AC sinusoidal burden voltage is reached in 1.5 cycles. Due to these two different integration time windows, the enhanced volt time area multiplier, $(k \cdot X/R + 1)$,

must not be used to calculate a true volt time area for any fixed integration time window.

Primarily due to the dissimilar integration windows and as illustrated in Figure 3, CT saturation of X/R=20 is not 4 times worse than that of X/R=5. It simply means that the saturation recovery time of X/R=20 is 4 times longer than that of X/R=5.

- **Realistic X/R ratio** – The enhanced volt time area multiplier, $(k \cdot X/R + 1)$, has significant impacts on CT saturation, as illustrated throughout this paper. For many large generators, a typical X/R ratio is 80, but it should be used only for faults on the load side of generator circuit breakers. For faults on the generator side, a typical X/R ratio may range 15 – 25 due to that of generator stepup transformers. (*Note: The X/R ratio is that of the primary fault current entering the CT*.)
- **Transformer differential relaying** – In general, it uses 2nd harmonic blocking which may block tripping for external faults causing CT saturation. Therefore, for the high-voltage side CT, a volt time area multiplier as low as 2 instead of $(k \cdot X/R + 1)$ may be used if feasible [1][2].
- **High impedance bus differential relaying** – In general, it is set not to trip for external faults causing saturation of one CT. Even though CT saturation is not desirable at all, it can tolerate saturation of one CT.
- **Staged fault at the generator terminal** – Earlier, the author made a point in which DC offset rarely exceeds 0.25 p.u. for all naturally occurring faults. For a real-life short circuit test of generator, the generator circuit breaker is closed into 3LG and so the actual fault inception can occur near 0 voltage. DC offset may reach 1 p.u. for this type of staged faults.
- **Half saturation recovery time** – It should be used only for solving DC offset-caused CT saturation problems.
- **No specific entry for CT remanent flux** – The (original or enhanced) volt time area method does not allow any remanent flux entry. If required, V_s should be lowered by the remanent flux amount (e.g., $(1 – 0.4) \cdot V_s$ for remanent flux = 0.4 p.u.) only for the 1st few cycles as a rule of thumb. As illustrated in Figure 8 and highlighted in Section 3.7, the CT remanent flux matters only for instantaneous relaying and it is insignificant for time-delayed relaying.
- **No specific entry for CT secondary x/r ratio** – It is not a significant issue because the current time area of the inductive burden is larger than that of the resistive burden. (*Note: As indicated earlier, the volt time area method was originally developed for the resistive burden*.)

V. Other Factors Causing Quantitative Errors

5.1 Filtering and A/D converter saturation

As illustrated in Figure 14, fault currents are transformed, low-pass filtered, sampled/held, amplified (if used), analog-to-digital converted, and digitally filtered.

Each element's role is to make quantitative conversion or transformation for computational accuracy/simplicity. Therefore, it is conceivable that any one of them can inject some unwanted quantitative error(s).

If the input to the A/D converter exceeds the A/D converter range, the A/D converter output is limited to the maximum value (e.g., 102A, 154A, 174A, 224A, etc.), which is termed "A/D converter saturation" in this paper.

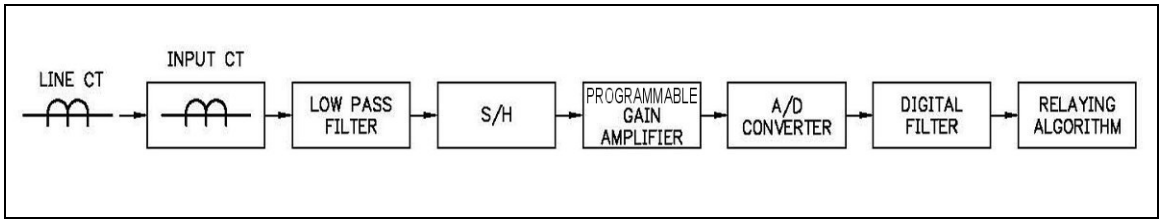
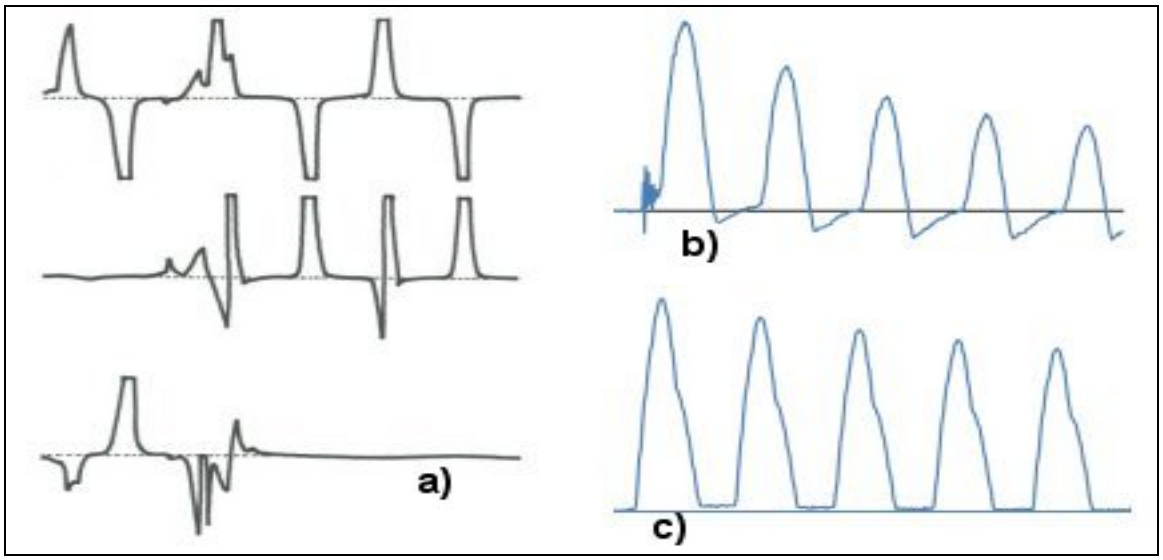


Figure 14. Signal propagation through various signal conditioning and processing elements of a modern digital relay



a) A/D converter saturation resulting in clamping, CT saturation resulting in chopping of the wave front, and evolving fault resulting in the fault type transition from c-to-a LL to a-to-b LL.
b) Energizing a radial transmission line with multiple 25MVA 3-phase stepdown power transformers with loads connected to their secondaries.
c) Energizing a radial transmission line with a 125MVA 3-phase stepdown power transformer without any load connected to its secondary.

Figure 15. Other sources of waveform distortion: A/D converter saturation and transformer energization inrush (*recorded by digital fault recorders*)

Figure 15.a) illustrates a real-life A/D converter saturation case in which fault currents were clamped or flat-topped at the A/D converter saturation value. {*Note: Due to metal oxide varistor clamping the input voltage to an acceptable level, the appearance of a high impedance bus differential relay input voltage waveform may look just like Figure 15.a).*}

5.2 CT saturation versus transformer inrush

Figure 15 illustrates a couple of transformer energization inrush waveforms which look somewhat similar with saturated-CT waveforms, because both CT saturation and transformer inrush are caused by core saturation. Some subtle differences are:

- Transformer inrush is caused by core saturation and core saturation is caused by remanent flux in the core, while CT saturation is often caused by DC offset as discussed and illustrated earlier in this paper.
- Transformer inrush is much larger than the load current, so it is practically pure magnetizing current whose tip looks like a needle. Therefore, the transformer inrush current waveform (primary to CT) contains a high degree of 2nd harmonic. Saturated-CT current is not the magnetizing current for the resistive burden even though it may contain a high degree of magnetizing current for the inductive burden. As presented earlier, the saturated-CT current waveform has one of three shapes (chopped, decaying or flat-topped).
- In general, transformer inrush is not distorted by the CT and the transformer inrush waveform width is typically larger than a half cycle width. In general, the chopped waveform due to CT saturation has a very narrow width.
- The transformer inrush damping coefficient, R_t/L_t, is not constant due to variation of the transformer inductance L_t. The transformer inrush is very high only for the 1st few cycles because the transformer inductance L_t is very small initially but quickly increases over time. DC offset-caused CT saturation is not damped as quickly as the transformer inrush because the system inductance L does not vary quickly.
- Most power transformers are 3-phase, so the interaction of 3-phase fluxes may introduce a shoulder on the rising or falling quarter-wave as shown in Figure 15.c). Most CTs are 1-phase, so there is not any flux interaction between phases.

VI. Options to Be Considered

To mitigate CT saturation problems, the following can be taken into consideration:

- Higher accuracy CT if available and feasible.
- Higher CT tap if available and feasible.
- Delay of the instantaneous relay operation by the half saturation recovery time if feasible.

- Increase of the coordinating time interval by the half saturation recovery time if feasible.
- Reduction of the CT secondary burden if feasible.
- Rogowski coil instead of CT.
- Optical transducer instead of CT.
- Process bus for the bus differential relaying.
- Reduction of fault currents (*by transmission grid configuration changes, bus configuration changes, installation of current limiting reactor, etc*.) if feasible. (*Note: Installation of a current limiting reactor may increase the X/R ratio which may worsen DC offset-caused CT saturation*.)
- Peak detector if available and feasible.

VII. Conclusion

CT saturation has been a well-known problem in our relaying industry and it has caused some inaccuracies in the areas of fault detection, fault direction, fault type identification, fault location and fault clearing time. It is getting more attention and becoming more visible, due to newly established NERC/WECC investigation/reporting requirements and use of digital fault recorders.

Some of the author's primary objectives were comparison of two dissimilar CT analysis methods, understanding all critical factors causing CT saturation, and making the volt time area method more realistic for relay application engineers. Therefore, the following conclusions are presented as a summary of this paper:

- The volt time area method represents CT saturation more accurately than the Ohm's Law method due to inclusion of the volt time area multiplier, (X/R + 1), but it is practically the same as the Ohm's Law method with inclusion of the volt time area multiplier.
- CT saturation can be systematically analyzed by thorough understanding of critical CT saturation factors such as CT accuracy rating, DC offset, system X/R ratio, fault current, CT burden, CT secondary x/r ratio, and remanent flux.
- The volt time area method does not allow any entry for DC offset level, CT secondary x/r ratio and remanent flux.
- 3 distinct wave shapes: **chopped, decaying and flat-topped**.
- Assuming DC offset of 1 p.u. may be unrealistic and impractical. Therefore, the author recommends use of a new **DC offset factor "k"** and corresponding **enhanced volt time area multiplier, (k·X/R + 1)**, and **k = 0.25** for all practical purposes.
- **Enhanced volt time area method**:

$$(k \cdot X/R + 1) \cdot I_f \cdot Z_b \leq 20 \text{ if p.u. values are used,}$$
$$(k \cdot X/R + 1) \cdot I_f \cdot Z_s \leq V_s \text{ if amps, volts and ohms are used,}$$
$$(0.25 \cdot X/R + 1) \cdot I_f \cdot Z_s \leq V_s \text{ if k=0.25 is used.}$$

- X/R in cycles as **saturation recovery time** and use of the **half saturation recovery time** (0.5X/R in cycles) for relaying coordination purposes.

The author sincerely hopes that this technical paper may be of some value to the 35th Western Protective Relay Conference attendees and may help relay application engineers fine tune their current transformer sizing and saturation analysis.

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