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SOME OBSERVATIONS ON BUS RELAYING

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SOME OBSERVATIONS ON BUS RELAYING

Walter A. Elmore

Abstract: The literature is replete with guidance on the subject of bus relaying. Because of the extremely detrimental results of incorrect operation of bus differential relaying, those giving such guidance have generally leaned in the direction of security. This paper is intended to point out the possibility of easing some of the useful, but not immutable restrictions that have been handed down from generation to generation.

In general, the bus configuration does not dictate any particular bus differential relaying concept. Voltage level and importance of the circuits connected to the bus are far more significant criteria. Speed and cost are key factors. Current transformer location and quality are important ingredients in the choice of a bus relaying scheme.

General Description

No task could be simpler than to design a relaying system for bus protection that would detect all internal bus faults and trip all of the appropriate circuit breakers at very high speed. The trick is to accommodate these two requirements while **always** avoiding misoperation for external faults and other "through" phenomenon, current transformer misbehavior, control circuit transients, and all types of primary circuit transients.

Differential protection for any type of apparatus or circuit involves the application of Kirchoff's Law, which says simply that the currents into a point must equal the currents out of that point. This applies to instantaneous currents, rms currents, or average currents. This is true for the case of an external fault as well as an internal fault. The problem, in the case of the internal bus fault, is that the relay has no access to information regarding the current in the fault, except as inferred by the non-zero summation of the total current into and out of the bus.

Perfect transformation of current from the primary circuits to the bus differential relays is required in the theoretical application of this concept. Unfortunately, current transformers have errors in the magnitude and in the preservation of the phase of the transformed current. These errors appear as differential current to a bus relaying system. The relay must accommodate these errors or ignore them in some chosen way.

Errors in the transformation of the ac component of primary current can be rather easily accommodated because they are small in properly applied current transformers. However, the dc component of the primary current may be devastating in its influence on the current delivered to the bus differential relaying system.

Bus Differential Types

Many ingenious methods of providing protection to station busses have been created. Some of those that are in common use are:

1. Simple Overcurrent
2. Multiple restraint
3. High Impedance
4. Differential Comparator
5. Partial Differential
6. Blocking

Each of these schemes has characteristics that are unique, but they all have the common frailty of dependence on the current transformers that feed them. Figure 1 shows that the critical fault is external to the bus and occurs on the circuit having the poorest current transformer performance. The generally accepted equivalent diagram is shown for that current transformer. Any current required to excite the core manifests itself as error current and encourages misoperation of the relay

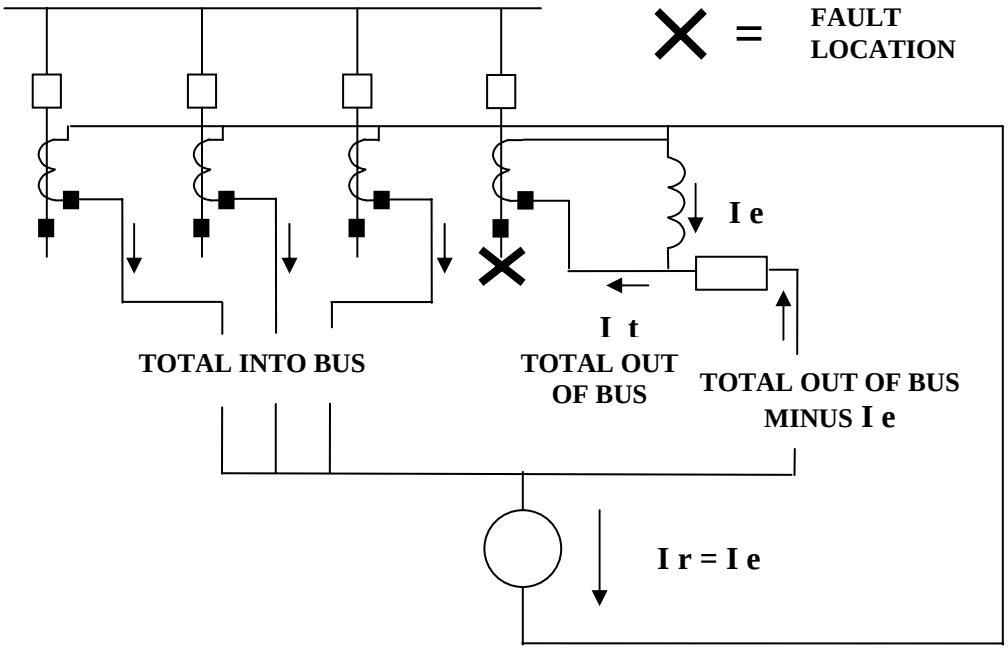


Figure 1 External Fault Case

For this fault, the currents into and out of the bus match. However, the current transformer in the faulted circuit has exciting current requirements well in excess of that for the other ct's. As

shown in figure 1, this error current flows in the relay. In the absence of dc saturation, this error current will not exceed 10 amperes if the burden voltage is less than $V_{CL,}$ the relaying accuracy class voltage. Thus, the setting of the relay can be roughly 12 amperes to override the long term error current. During the period in which the dc predominates other expediencies must be taken.

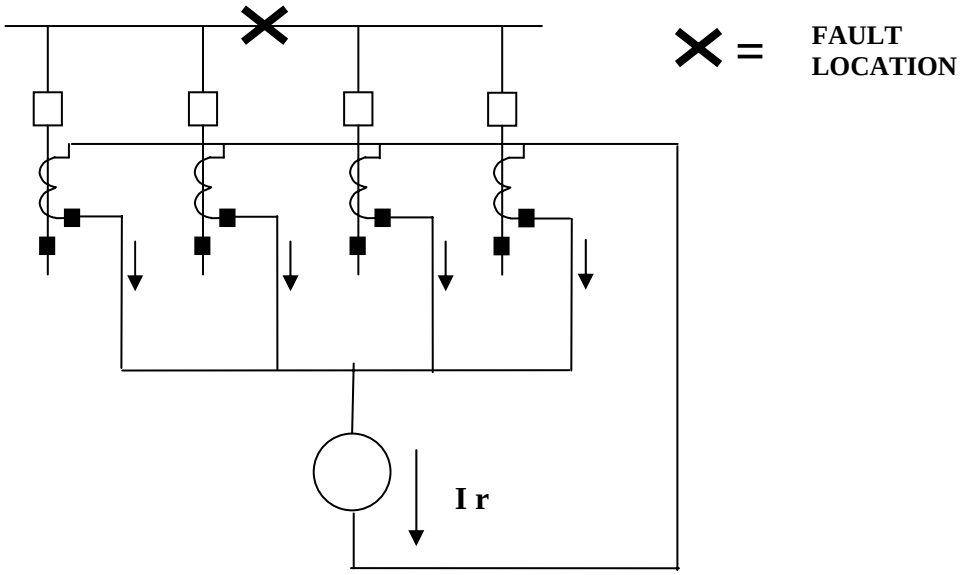
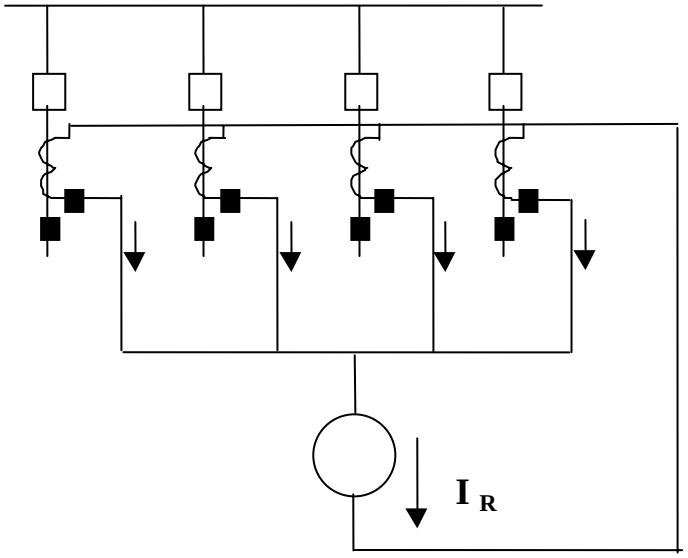


Figure 2 Internal Fault Case

Note that, for the external fault, the I t current does not contain the contribution to the fault from the faulted circuit. For an internal fault, the circuit contribution that was missing for the external fault is now added to the total current. However, the current in the circuit previously considered to have the external fault now, for the internal fault, has a much smaller current through it. The voltage across the magnetizing impedance is established primarily by the total fault current flowing through the combination of relay impedance and the resistor. If this voltage doesn't exceed the relaying accuracy class voltage rating of the ct's, severe saturation of all of the current transformers will not be expected. Less than 10 amperes of error current would be expected if the ct's are selected so that the total external fault current cannot exceed 100 amperes (using ANSI Standard ct's).

The approach thus far has assumed the unachievable circumstance that no dc component exists in the fault current. In general, dc will exist and it will persist in significant quantity for three time constants. Dc is devastating in its influence on the saturation of current transformers.
If this relaying scheme is to be used, it must be delayed by a time corresponding to three dc time constants (3 x L/R) of the primary circuit.



APPLICATION OK IF :

1. SYMMETRICAL SECONDARY CURRENT TOTAL LESS THAN 100 AMPERES

2. BURDEN LESS THAN RATED

3. RELAY SETTING GREATER THAN 10 AMPERES

4. TRIP DELAY GREATER THAN 3 DC PRIMARY TIME CONSTANTS

Figure 3 Simple Overcurrent Relay Bus Differential

Simple Overcurrent Relay Bus Differential

The overcurrent scheme has been employed with success in the protection of less critical buses. Examining the significant influences, it can be seen that considerable gain in security is possible by the simple addition of a resistor in series with the overcurrent relay.

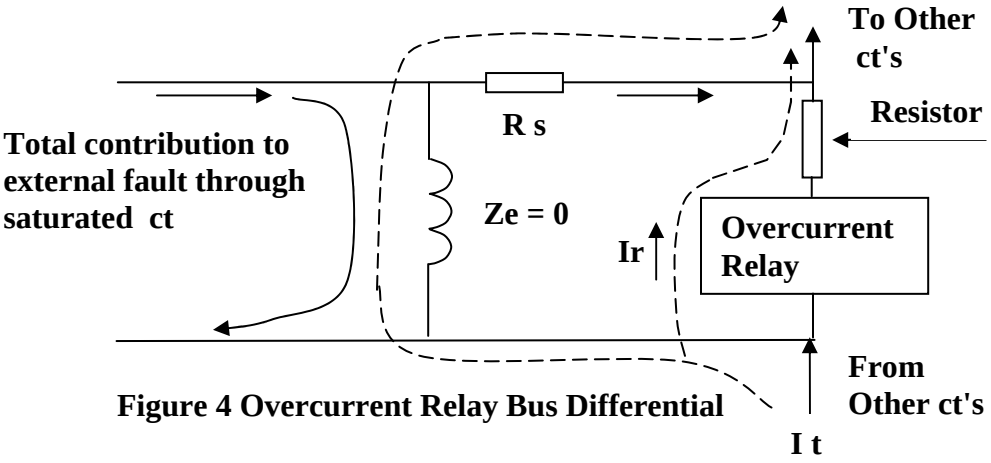


Figure 4 Overcurrent Relay Bus Differential

If the extreme assumption is made of total saturation of the ct associated with the faulted circuit, it can be seen that the voltage across the relay circuit will be**:**

$$Vr = \frac{Rs\ Zr}{R\,s + Z\,r}\ I\,t$$

The relay current will be**:**

$$I_r = \frac{R_s I_t}{R_s + Z_r}$$

Current to the relay, I r, in figure 3 can be reduced for an external fault by introducing the resistor in series with the relay. The current magnitude becomes **:**

$$I_r = \frac{R_s I_t}{R_s + R + Z_r}$$

where : I r = relay current
Rs = secondary impedance of this current transformer
R = resistance introduced for added security
Zr = Impedance of the overcurrent relay
I t = total current contributed to the external fault.

With this equation, a relay setting and resistor can be chosen that will allow an external fault to be ignored, even in the presence of total saturation. Typical constants for this arrangement, with 600:5 ct's and their accompanying secondary resistance allow the use of a setting of 10 amperes for the relay and a resistor of 3 ohms to be used to provide a secure application with little or no time delay.

For the internal fault, the presence of the series resistor decreases the sensitivity of the system because of the higher voltage across the relay branch and the resulting increase in the exciting current requirements of all of the ct's involved.

From this, we conclude that if insensitive, slow bus relaying can be tolerated, a simple, low cost overcurrent relaying scheme can be applied. Security can be enhanced by using a resistor in series with the relay and considerably faster tripping can be accomplished. Modern blocking schemes that will be described later, allow much faster and more sensitive bus protection for applications such as this.

Multiple Restraint Bus Relaying

Much of the vulnerability of the previous system stems from the absence of restraint in the relay. Highly sensitive internal fault detection can be achieved while ignoring external faults through the use of multiple restraints in the relay. One such arrangement uses six restraints arranged as depicted in figure 5.

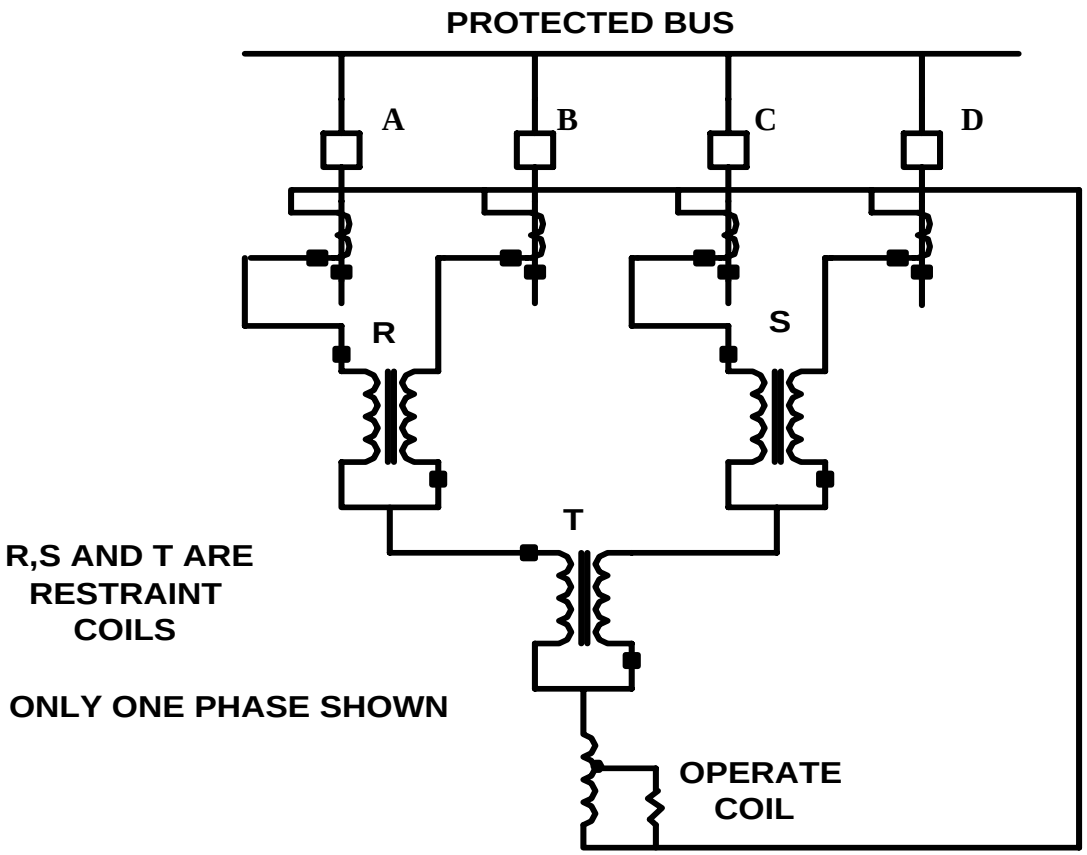


FIGURE 5 MULTIPLE RESTRAINT

The relay has three induction disks, each of which has two electromagnets. A fourth electromagnet receives the differential current and produces operating torque. No current can be delivered to the relay without passing through a restraint coil. The connection described by figure 4 is the appropriate connection for a four-circuit bus. The polarity marker on the restraint coil is significant only with respect to the polarity marker on the other coil on the same electromagnet. Currents into the polarity markers simultaneously produce an additive effect on restraint. Current into one polarity marker and an equal current out the other nullifies the restraint altogether provided by that particular electromagnet.

It will be observed that, for a bus fault, **equal** contributions from all four circuits produce a complete absence of restraint when this connection is used. Very sensitive protection can be provided by this arrangement. Too much restraint can be a detriment in the electromechanical implementation of this relay. If, for example, circuit A is the only source of fault current to the bus, two restraints become involved, and this double restraint will delay the operation of the relay undesirably because of the reduction of net restraint. Pairing of the currents on the

individual electromagnets may, at times, become tedious, but the task is actually quite straightforward.

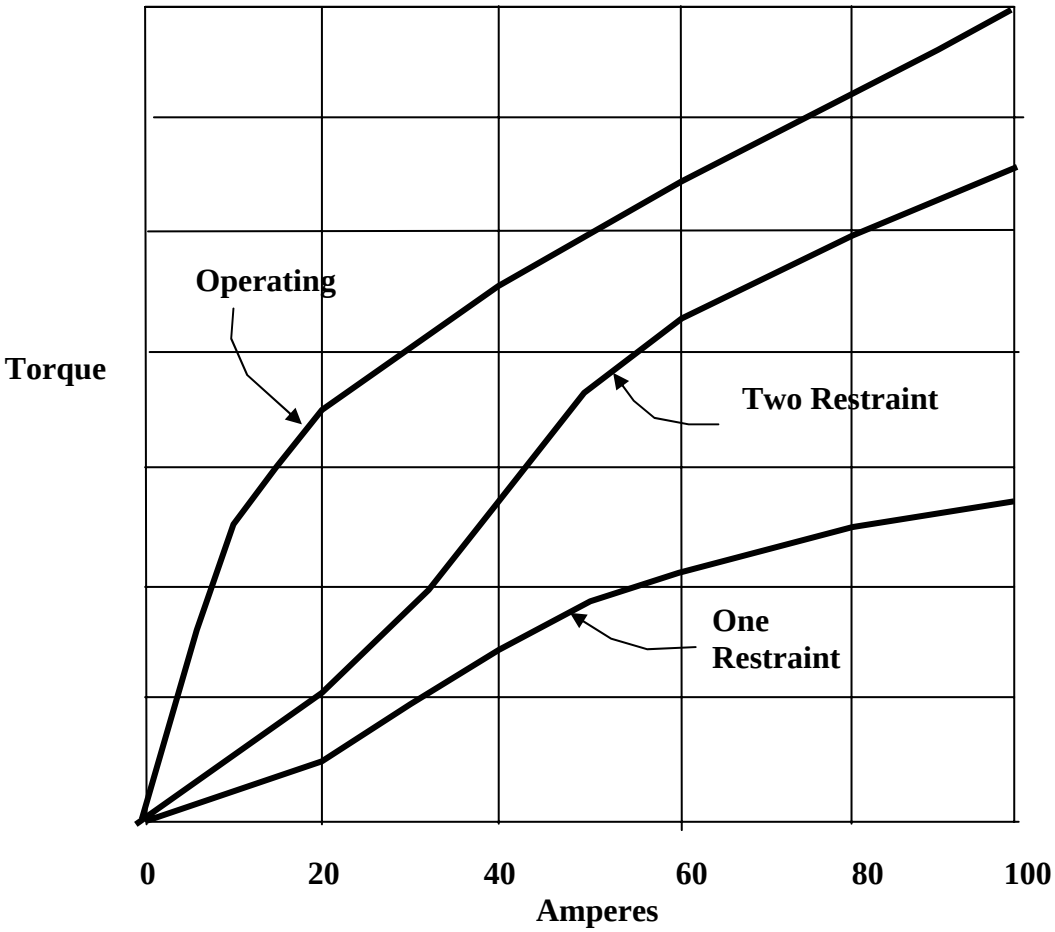


Figure 6 Torque for Typical Multi-Restraint Relay

This can be observed in figure 6. The cumulative restraint, taking into account the possible important influence of the polarity marks, compared to the operating torque is what determines whether the relay will operate or not. If the operating torque exceeds the restraining torque, the excess establishes the speed of operation.

The other side of this condition needs to be explored also. Too much restraint for an external fault imposes the hazard of a possible rebound contact closure for an electromechanical relay. This too is unacceptable. Adequate restraint must be the goal, not overpowering restraint for an external fault.

Each case must be examined to assure that the restraining torque is limited for an internal fault and yet is not excessive for an external fault. Since this relay has no settings, these requirements must be satisfied by knowledge of the fault contributions for each circuit connected to the bus so that the appropriate connection may be chosen.

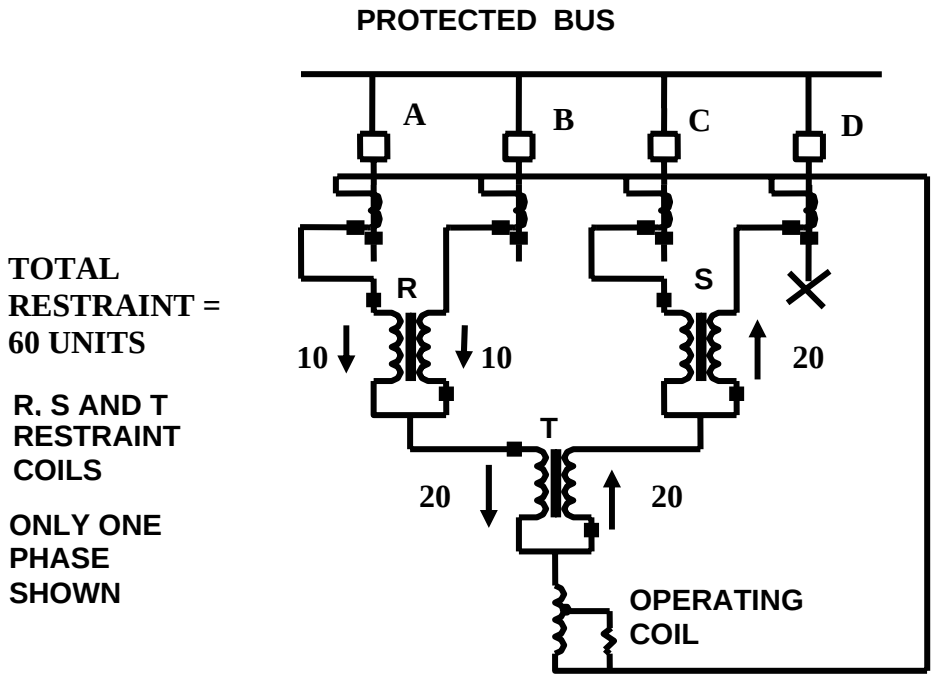


Figure7 Multiple Restraint Example (Sources on A&B)

Figure 7 is an example of this. Circuits A&B are sources and each delivers 10 amperes to restraint R. By the nature of their contributions, complete cancellation of restraint in this electromagnet results. In "T", the net effect is 40 amperes of restraint, and in "S", another 20 amperes of restraint is developed.

The total restraint for this external fault is approximately the equivalent of that which would be produced by 60 amperes flowing in one restraint. The operating current is established by the error currents of the current transformers. From figure 6, it can be seen that 60 amperes of restraint would overcome the effect of approximately 7 amperes in the operating circuit. Note that ct's such as those in circuit D of figure7 may actually be the representation of several ct's in parallel from minor circuits beyond D. This connection for this version of the multiple restraint relay is referred to as the "4 circuit connection."

Examination of other combinations of possible external fault conditions will show the degree of security that will exist using this arrangement. Figure 8 demonstrates that similar restraint will be produced with other possible current contributions than those of figure 7.

The total restraint corresponds to that which would be produced by 60 amperes in one restraint winding. With this connection and a much larger contribution through the bus to an external

fault, the restraining torque may be overwhelming, and the possibility of a rebound trip may exist. By rebound trip, it is meant that the torque holding the tripping contacts open during the external fault is so large that upon release (as the fault is removed by the action of other devices), the moving contact leaps off of the stationary contact with such force that it travels to the trip position. This is, of course, intolerable.

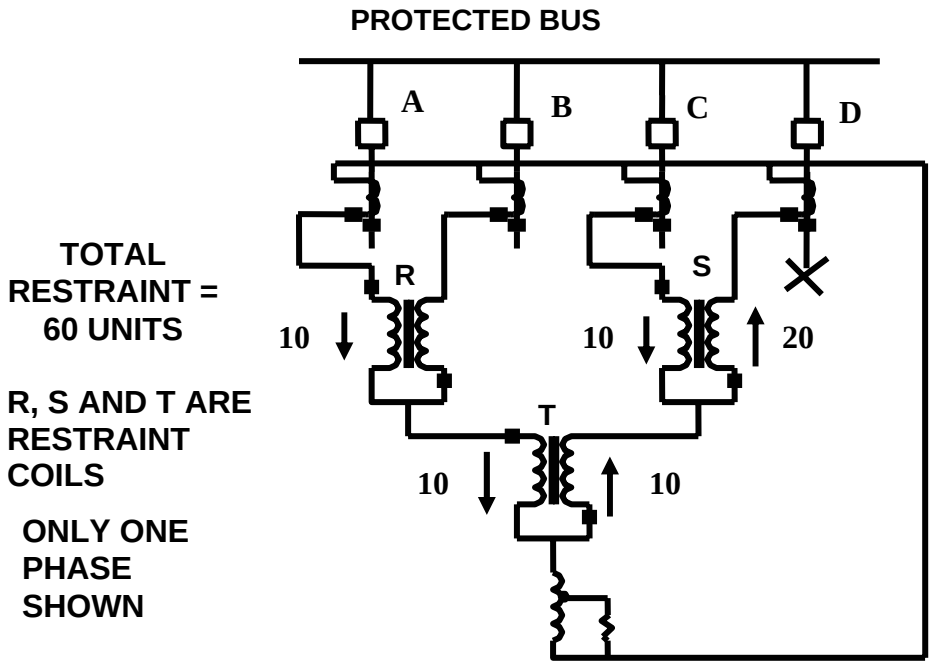


Figure 8 Multiple Restraint Example (Sources A&C)

Though this is an imprecise judgement because of the variations between relays, it is felt that a total equivalent ampere value for restraint for an external fault should not exceed 300 amperes. Beyond this, the connections of figure 9 should be chosen. Note that two additional circuits are accommodated with this connection, but this is a minor consideration.

With the same fault currents available, it is seen that considerably less restraint torque is produced when the connection of figure 9 is used. This connection is only necessary when the external fault current is considerably higher than that chosen for the example.

Having examined the conditions associated with this example for an external fault, the internal fault may now be compared for the two connections. The same total contribution of 20 amperes (secondary) to the internal fault is assumed.

The results are quite similar for the two connections in this particular case. At the low current levels chosen here, the choice of connections would be that of figure 7 because of the substantial, but not excessive, restraint that would be provided for this external fault.

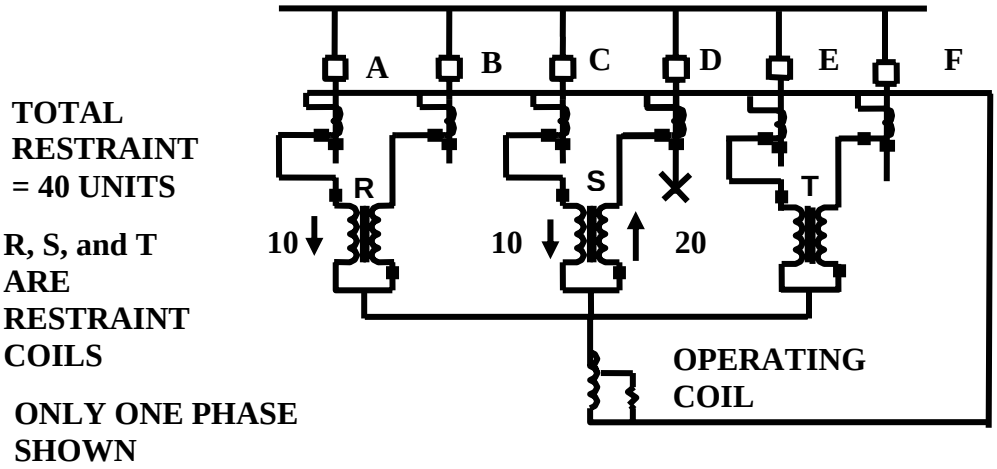


Figure 9 External Fault Multiple Restraint Example (Sources on A&C)

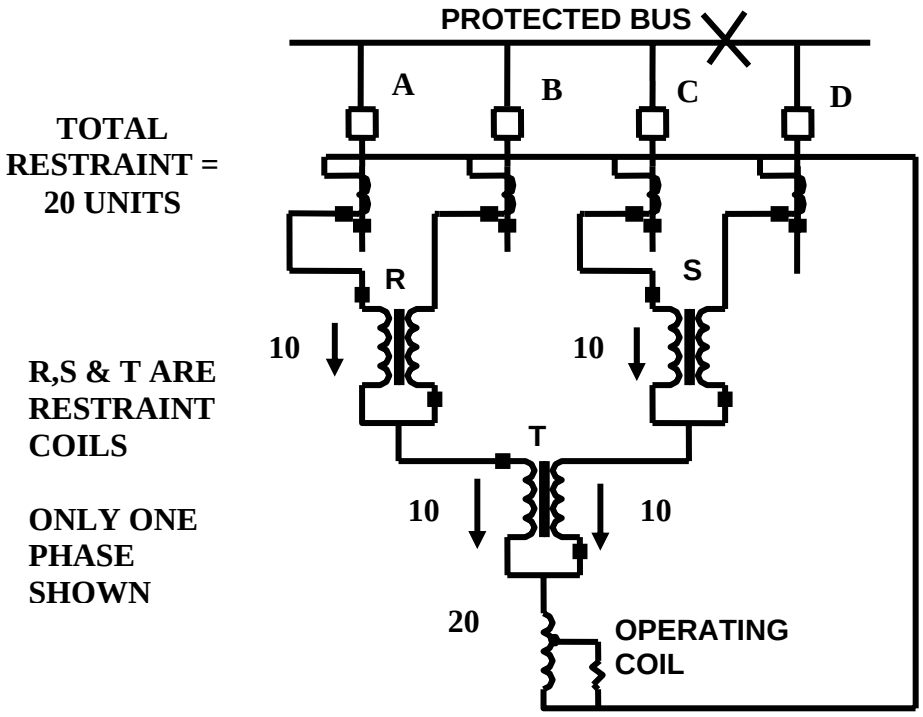


Figure 10 Internal Fault Multiple Restraint (Sources A&C)

If the fault current contribution from circuit A in figure 8 were 80 amperes and from circuit C were 20 amperes (in secondary amperes, of course), the total restraint for this external fault would be the equivalent of 360 amperes in one restraint coil. This is excessive, and this connection should not be used because of the possibility of a false trip due to rebound. Rather, the connection of figure 11 should be used. This is referred to as the," 6 circuit connection."

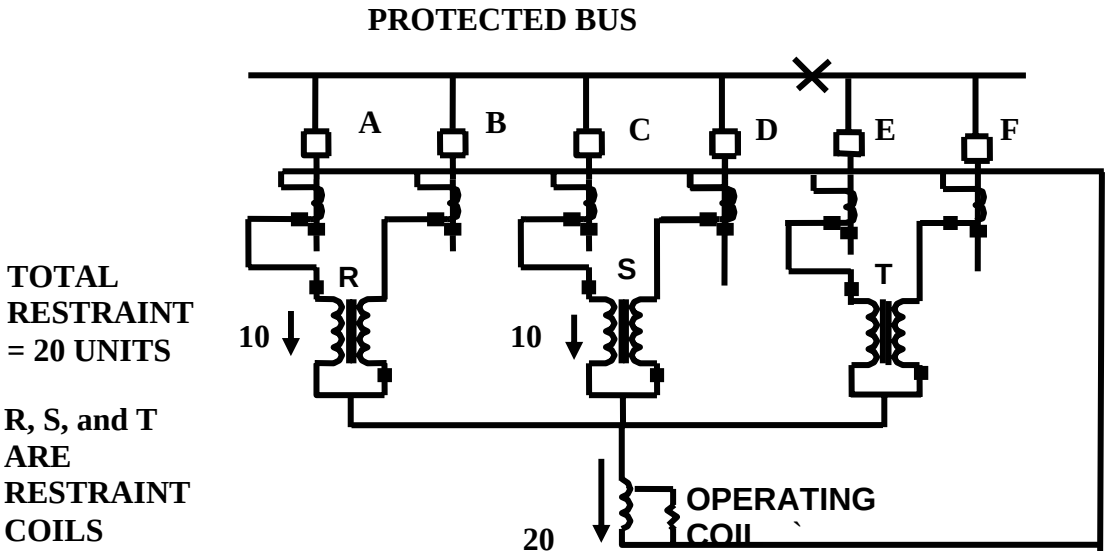


Figure 11 Internal Fault (Sources A&C)

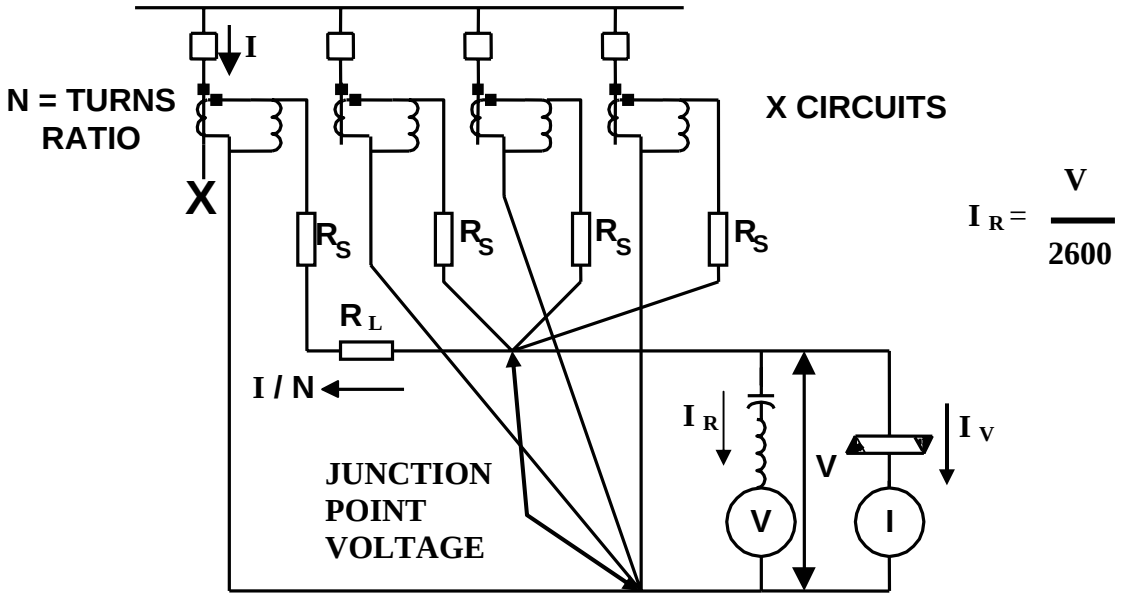
Using the connection of figure 11, with 80 amperes from A and 20 amperes from C, an external fault on circuit D produces only 100 amperes of restraint (compared to 360 using the connection of figure 8), allowing comfortable restraining energy for an external fault and reasonable speed for an internal fault.

HIGH IMPEDANCE DIFFERENTIAL

The high impedance bus differential is one of the most flexible differential schemes in use. It is easily expandable to accommodate new circuit additions to a substation. The scheme consists of the simple paralleling at a junction point of the current transformers associated with each of the circuits connected to the bus. A setting is chosen that exceeds the maximum voltage that can appear at the junction point for an external fault. That voltage is influenced by the external fault current and the loop impedance including the faulted circuit current transformer and the lead impedance from the junction point to the ct. The name of the relay comes from the fact that the impedance of the relay is chosen to be very high (2600 ohms, in one case). Figure 12 describes this relay.

The strategy for this relay assumes complete saturation (no output) from the current transformer associated with the faulted circuit for this external fault. The voltage unit (V) is adjusted so it

will not operate for a voltage equal to the maximum secondary current for the external fault times the sum of the lead resistance (R_L) and the ct secondary resistance (R_S).



EXTERNAL FAULT

$V > (I / N)(R_L + R_S)$ **(FOR SECURITY)**

INTERNAL FAULT

$I_{MIN} = (XI_E + I_R + I_V) N$ **(SENSITIVITY)**

Figure 12 High Impedance Differential

R_L can often be estimated from the knowledge that a bushing type 2500/ 5 ampere ct will typically have a secondary resistance of 1.0 ohm. The number of turns on the secondary of a ct, and thus the secondary resistance, varies with the ratio. The secondary resistance of a 1200/ 5 ct could be estimated to be 1200 / 2500 (1) = 0.48 ohms. The estimated value should never be used when more accurate information can be obtained.

While the rule of thumb to **never** supply other devices from the same ct's that are used for the differential function is a good one, it is only a fair warning, and not a brick wall advocacy. Other devices simply add to the R_L impedance and thereby decrease the sensitivity of the system to internal faults. Too little current does not appear to be a problem generally, so this should not be an impediment to the use of this scheme.

Another taboo unnecessarily restricts the user to identical ct's that make up the differential scheme. The rule is a perfectly good one and adherence to it will produce results that provide the greatest margins. However by giving careful consideration to the actual ct ratios and analyzing the maximum end-winding voltage that can be generated due to autotransformer effect, a variety

of ct choices can be allowed. The lowest achievable sensitivity is not always a mandate for bus protection.

For internal faults, the voltage at the junction point must be high enough to operate the voltage unit. In addition to the current delivered to the relay, this voltage produces current in the varistor (included to protect the relay against excessive voltage) as well as in all of the ct's in the differential system (magnetizing current). The current in the varistor can be ignored because it is too small in a modern relay to be significant. A representative setting of this relay is around 75 volts. The exciting current for a C100 ct is approximately 0.2 ampere or less at 75 volts. From this example, it can be seen that this relaying scheme can be quite sensitive.

Note that there is an instantaneous trip unit in series with the varistor. Thus if the voltage appearing at the junction point for an internal fault is high enough to cause the varistor to "conduct", the instantaneous unit will operate. The current transformers have a voltage limiting quality about them. There is a secondary voltage at which the current transformers will saturate. The maximum voltage that can appear across the junction points will be limited to the saturation level of the ct having the lowest relaying accuracy rating of all of those in the group.

The level at which a modern varistor designed for this service will "conduct" is approximately 800 volts rms. With ct's having a relaying accuracy class less than C800, the instantaneous element may have little use (other than to provide a seal when the varistor is shorted by the lockout relay).

Differential Comparator

The ingenious differential principle used in this scheme initially utilized a set of diodes to collect all of the currents flowing to the bus (in secondary terms, of course) and another set to collect all of the currents flowing away from the bus. This was done on an instantaneous basis, thereby allowing an instantaneous assessment of whether or not an internal fault existed.
If the comparison indicated that the sum of the currents coming into the bus exceeded that of those leaving the bus, there was obviously a path for current flow that was not accounted for in the differential system. Three millisecond energization of the trip coils of the circuit breakers associated with the bus were common. Figure 13 describes the circuitry for this relay.

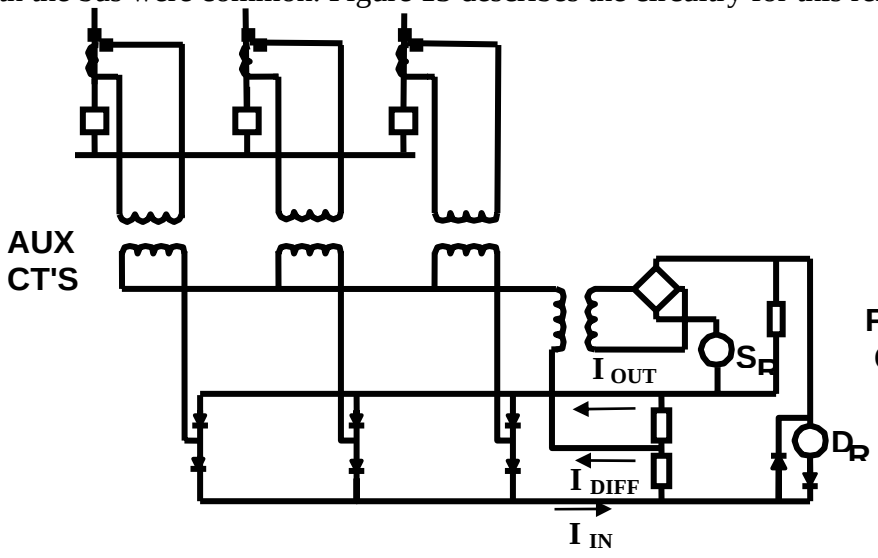


Figure 13 Differential Comparator

Microprocessor relays are perfectly capable of identifying current magnitude and direction at high speed without the diodes, but a few samples of the current must be obtained. The relay is, then, ultra high speed, but not as it's analog equivalent, instantaneous. A variety of input ct ratios can be accommodated as simple setting inputs to this relay, and the scaling for internal comparison is done numerically. Such a concept incorporates in this scheme extreme flexibility and excellent performance.

Partial Differential

The partial differential scheme is much like a complete differential scheme except that all of the circuits are not included in the summation. Figure 14 describes this arrangement.

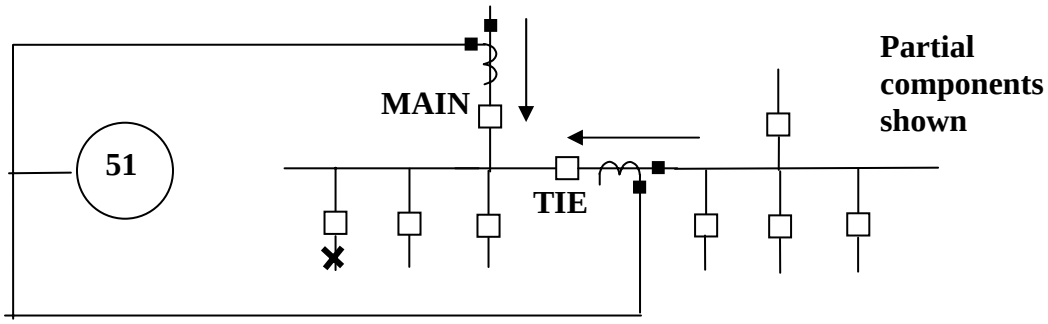


Figure 14 Partial Differential

Note that the relaying is shown only for the left-hand bus. A similar complement of ct's and relays are required for the right-hand bus. The partial differential relays must be coordinated with the feeder relaying on its bus. This scheme is inherently slow and insensitive, but it may be effective for some distribution substation applications.

Blocking Scheme

A far superior scheme to the partial differential arrangement is the blocking scheme. It requires more apparatus or software but is easily achievable. Looking at figure 14, it can be seen that feedback from each of the feeder relaying systems to the associated source breaker relaying allows the main (and tie) breaker relaying to identify immediately the need for high-speed tripping or coordinated (slow) tripping. A simple instantaneous overcurrent function in each of the feeder circuit relays reports to the main (and tie) breaker relaying that a fault exists beyond the feeder position. If no such report is made, and the main breaker relaying identifies the presence of overcurrent, it is clearly a bus fault and immediate tripping of the source breakers can be executed.

COMPARISON TABLE

	COST	EASE OF USE	SENSITIVITY	DEPENDABILITY	SECURITY	FLEXIBILIT	SPEED
SIMPLE OVERCURRENT	LOW	GOOD	POOR	GOOD	GOOD	GOOD	POOR
MULTIPLE RESTRAINT	MED	POOR	BEST	GOOD	GOOD	POOR	GOOD
HIGH IMPEDANCE	MED	GOOD	GOOD	GOOD	BEST	GOOD	FAST
DIFFERENTIAL COMPARATOR	HIGH	BEST	GOOD	GOOD	BEST	BEST	BEST
PARTIAL DIFFERENTIAL	LOW	GOOD	POOR	GOOD	GOOD	GOOD	POOR
BLOCKING	MED	GOOD	POOR	GOOD	GOOD	GOOD	FAST

CONCLUSIONS

All of the bus differential schemes described here have experienced excellent service over the years. All have their strengths and weaknesses. All of them are dependent on a proper evaluation of their behavior in the presence of current transformer error. External faults are key determinants, with some schemes allowing total ct saturation, and others being less accommodating. Operating speed may or may not be influenced by the nature of the scheme.

In general, the application rules that are being used in the industry are entirely satisfactory, but this paper shows that a proper evaluation of those things that influence the reliability of the system may allow some departure from these hard and fast rules. Current transformers can be shared by other elements with the bus differential relays, Security and sensitivity may be

influenced by this, but analysis such as that described in this paper, may show that there are margins well beyond those that must exist for a safe and reliable installation.
In most cases, sensitivity is not a limitation, though it is always an aspiration. Bus faults tend to produce too much fault current rather than too little. Security is generally a more imposing constraint than dependability. However overemphasis on security may itself lead to unique insecurity, as described with respect to the multiple restraint relay.

For bus differential relaying, no misoperation can be tolerated. Therefore, considerable focus should be directed to the application of a scheme to any bus. Low cost, high speed, low burden, utmost sensitivity, maximum restraint -- no single characteristic alone should be allowed to dictate the nature of the relaying system. Rather, the needs of the complete application should lead to the proper choice of relaying types and their settings.

Reference

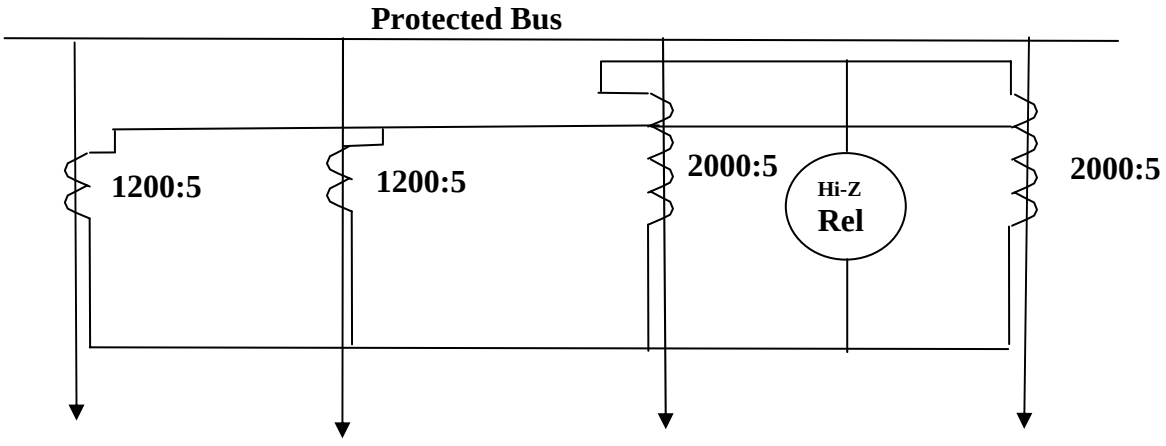
"Current Transformers and Relays for High-Speed Differential Protection with Particular reference to offset Transient Currents" by E.C.Wentz and W.K.Sonnemann, AIEE Transactions August 1940, Vol59, pages 481-488

APPENDIX

USE OF NON-IDENTICAL CURRENT TRANSFORMERS

History and experience tell us that all of the current transformers used in a bus differential relaying scheme must be identical. Though this is the preferred and conservative approach, it overstates the need. Indeed, some bus relaying schemes incorporate provision for accommodating current transformers having widely differing characteristics and ratios. The high-impedance bus differential scheme is not one of those.

This appendix attempts to show that the high-impedance bus differential relay can be used in certain applications where unlike ct's exist. Consider the example below. Two of the ct’s have a ratio of 1200:5 and two have a ratio of 2000:5 with a tap for 1200:5.



This connection provides balance for any external load or fault condition. The autotransformer effect that increases the voltage across the end points of the current transformer is taken care of by the connection of the relay and its protective varistor across the full winding of the largest ratio ct. Considerable care must be taken in selecting a setting for the relay. It must be set above the maximum voltage to which it may be subjected for any external fault case.

Another variation of this mix of ct's places the relay across the full 1200:5 winding. The 2000:5 taps are left unconnected (open circuited). Dependence is then placed on a careful evaluation of the maximum voltage that can appear across the full 2000:5 windings for an internal fault. The ct insulation and all connected leads and apparatus must support this voltage without damage.

Other solutions exist using high quality auxiliary ct's. Each case must be thoroughly analyzed with full recognition given to the influence of the resistance of the auxiliary ct itself and to the possible boost in voltage that it may introduce.

H.J.Li (retired ABB) has produced an excellent engineering memo, EM 81-001A (available from ABB, Coral Springs), analyzing these and other possible connections, concluding that considerable flexibility in the mixture of ct's is a realistic approach where adaptation to existing ct's is necessary.

Biographical Sketch

Walter A. Elmore was born in Bartlett, Tennessee, served in the Army Air Corps as a navigator during World War II, and graduated from the University of Tennessee with a BSEE in 1949. He was in Substation Design at Memphis Light Gas & Water Division until he joined Westinghouse in 1951 as a District Engineer in Seattle, Washington. He transferred to the Relay-Instrument Division in Newark, New Jersey in 1964, where he became Manager of the Consulting Engineering Section. He held that position, following a 1989 merger with ABB, until 1992 in Coral Springs, Florida. From 1992 until 1996, when he retired, he held the position of Consulting Engineer. He continues to work as a consulting engineer for ABB. In August 1996, he had the great honor of having the ABB manufacturing plant in Coral Springs, Florida dedicated to him.

He is past chairman of the IEEE / PES Technical Council, and past chairman of the IEEE / PES Power System Relaying Committee. He is a Life Fellow of the IEEE, and was presented the IEEE Gold Medal for Engineering Excellence in 1989. He was accepted as a member of The National Academy of Engineering in 1998.

He has presented over 100 technical papers, is one of the authors of the Year 2000" Standard Handbook for Electrical Engineers," and is the editor and co-author of two books: "Protective Relaying Theory and Applications" and " Pilot Protective Relaying." In April 1997, he received the Texas A&M "Most Prolific Author" Award.

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