Impact of Sampled Analog Values and Clocking on Line current differential element

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Abstract

With the increasing installation of digital substations utilizing IEC61850 process bus technology, operating the protection and control elements on sampled analog values (SAVs) is becoming more practical. This paper is aimed at understanding the impact of using SAVs to operate protection and control elements specifically for line current differential element even in hybrid cases where one end is conventional analog values acquisition and other end is a SAV acquisition. In conventional relays the analog signals from CTs and VTs to the relay travel at the speed close to that of light, i.e., almost instantaneously. As a result, the current and voltage measurements are naturally time aligned at the time of analog to digital (A/D) conversion at all line terminals. As such, the synchronization of relays at two or more terminals, which remains the most crucial aspect of the successful operation of 87L element, is inherent and guaranteed.

However, the SAVs travel over an Ethernet network which has inherent jitter and delay (which could be variable) associated with it. For successful operation of any protection element, it needs to be ensured that all the current and/or voltage samples that it uses are time-aligned to each other. In case of 87L element the compensation for the network delay is critical. Improper delay compensation would result in erroneous differential current.

This paper discusses the physical layout of the SAV system, the mechanism of alignment of the SAVs from various streams, applying compensation of network delay to SAVs. This paper also captures unique capabilities of SAV-based systems. Thereafter, this paper presents the various topologies of SAV-based 87L system that are implemented in the field along with the assumptions and considerations of each topology. Additionally, few theoretical topologies for SAV-based 87L are also discussed. The various enabling and limiting factor such topologies are also captured in this paper. Field examples of the application and performance of the line current differential element for both hybrid and SAV-to-SAV systems are given, with SAV and clocking impairments scenarios.

Index Terms

Digital Substation, GPS, IEC-61850, IRIG-B, Line current differential, Ping-pong, Sample Analog Values, Time Alignment

I. Introduction

In conventional relays, the output of instrument transformers are wired directly into the relay via copper wires. As analog signals travel through copper wires with speed almost equal to the light, the measurements are available at relay terminals almost instantaneously as the instrument transformers sense the primary signals. In conventional domain, therefore, the only crucial aspect for reliable operation of line current element (87L) element is the synchronization of the relays at each terminal to the other relays, which is done via well-know 'Ping-pong' method. Figure 1 shows a 2-terminal conventional 87L system. The ping-pong algorithm ensures that the Relay-A and Relay-B timestamps match each other closely. When Relay-A samples the current and voltage measurements, it applies its local timestamps to the samples and send the timestamped samples to the Relay-B. The Relay-B receives the samples and since, the timestamps of Relay-A and Relay-B closely match each other because of synchronization through ping-pong algorithm, the Relay-B is able to properly align the received samples to its own samples. Thus, 87L element can be operated reliably.

However, the substation infrastructure is slowly moving from conventional to digital domain. This requires replacing wired connections between substation equipment with fiber connections, using IEC 61850 protocol for data exchange between different substation entities. In digital domain, the instrument transformers are wired into an equipment called Merging Unit (MU), which samples the measured analog signals and sends the sampled analog values (SAVs) over an Ethernet network (see Figure 2). The SAVs arrive at the relay terminals over an Ethernet network where they are used for protection. These samples arrive with some time delay and this time delay could also be varying (jitter), unlike in

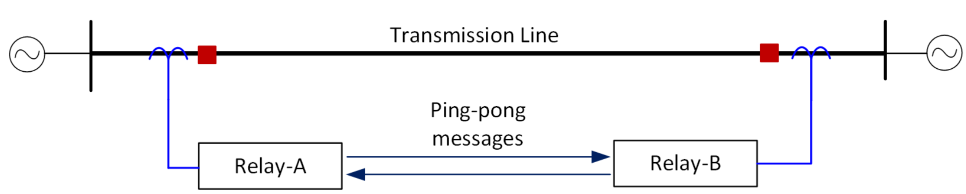

Figure 1: Conventional 87L system

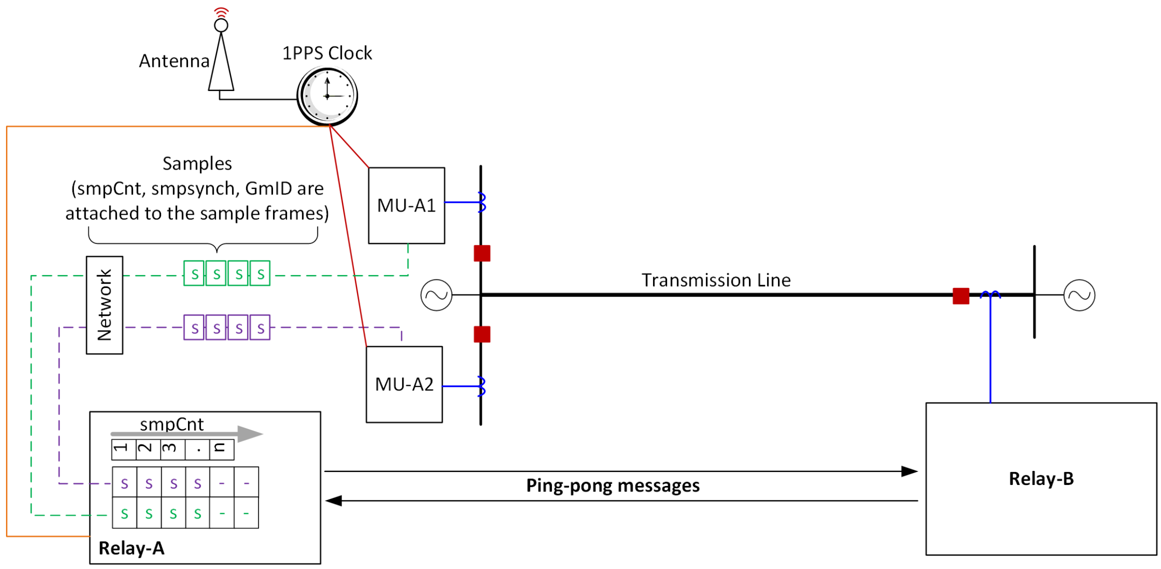

Figure 2: Schematic topology of an SAV system and 87L

conventional domain where the measurements are available at relay terminals ‘instantaneously’. From 87L perspective, the time delay between sampling at MU and arrival of the samples at the relay terminals plays significant role in synchronizing the measurements from different terminals. Ignoring this time delay will result imperfect synchronization of 87L relays and would result in ‘fictitious’ differential current. If the relays drift enough, it could lead to mal-operation of 87L element. Fortunately, these challenges can be overcome by using the architecture of IEC-61850 and by properly setting the time synchronization settings of the relay, as discussed in this paper. Note that the digital domain is referred to as sampled analog value (SAV) domain in this paper.

II. Time alignment and network delay compensation of SAVs for 87L application

In order to understand the time synchronization requirements for 87L element, it is important to know the significance of the following terms. The schematic diagram of Figure 2 can be used to better understand the significance of the terms. It shows 2MUs (MU-A1 and MU-A2) subscribed by Relay-A. The MUs and the Relay-A are connected to 1PPS Clock which inturn is connected to a GPS antenna. The MUs are sending the sampled value frames over a network to the Relay-A.

- **Variant Code**: It is MU nameplate which provides the information about the MU in a human readable format [1]. The template is: Ff SsIiUu;
  where
  f is the digital output sample rate expressed in samples per second, i.e., the sampling frequency of the MU;
  s is the number of ASDUs (sample frames) contained in a sampled value message;
  i is the number of current quantities contained in each ASDU;
  u is the number of voltage quantities contained in each ASDU.
  As an example, the variant code $F4800S1I4U4$ means that the MU under consideration has sampling rate of 4800samples per second (Hz); each message from this MU contains 1 frame of samples; each frame has 4 current and 4 voltage channels.
- **SmpSynch**: MUs are normally synchronized to the external time reference (clock) through PTP or IRIG-B. SmpSynch attribute holds the information about the state of the external clock. SmpSynch can attain the value of 2, 1, and 0. In the example of Figure 2, as long as MUs are synchronized to the 1PPS clock and 1PPS clock is connected to GPS Antenna (or synchronized to other global time source), the MU-A1 and MU-A2 will send the SmpSynch attribute set to ‘2’, indicating that MU’s are synchronized to global source. If the 1PPS Clock loses the antenna then it becomes a local clock source; in this case MU-A1 and MU-A2 will send SmpSynch attribute set to ‘1’, indicating that MUs are synchronized to a local time source. If the MUs lose the connection to the 1PPS Clock altogether then the MU-A1 and MU-A2 will send the SmpSynch attribute set to ‘0’, indicating that MU’s are not synchronized to any time source.
- **SmpCnt**: This is an attribute of the frame of samples which represents the the sample number from the start of the second. Whenever a pulse per second (PPS) is received by the MU from the external clock indicating the starting of a new second, the SmpCnt attribute of the next out going frame is set to 0. The SmpCnt for the next frame is 1 and so on till the end of the second when SmpCnt attains the value 4799. Rollover is allowed by the standard **IEC 61850-9-2**

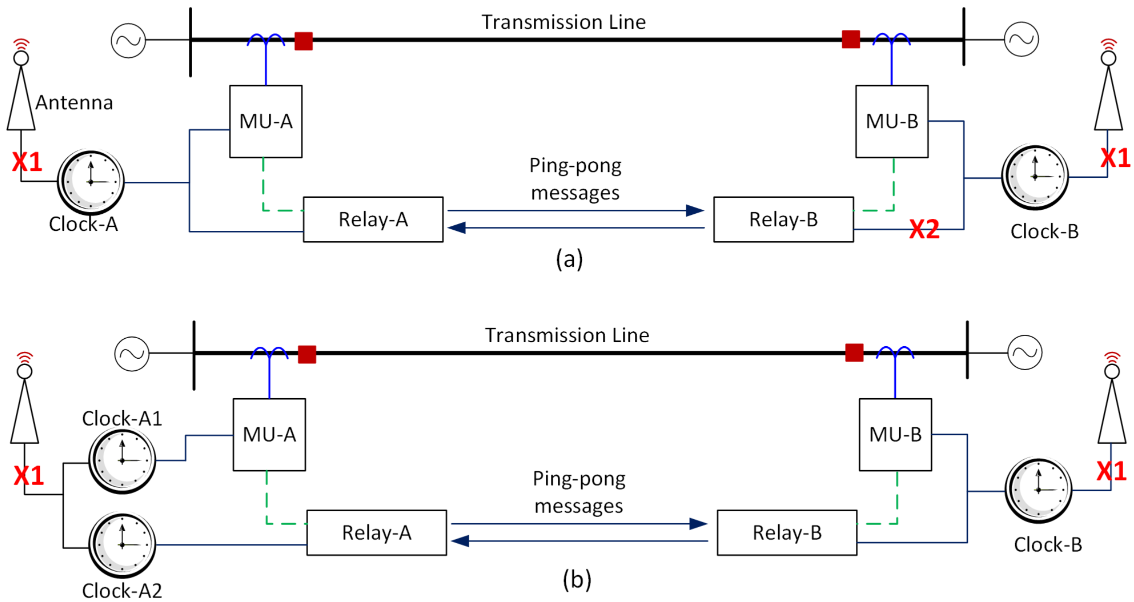

Figure 3: SAV-based 87-L relays at both ends of transmission line: (a) only one clock in the system at each terminal; (b) two clocks on Terminal-A of the transmission line.

Ed 2.1. In Figure 2, the 1PPS clock on the rising edge of a new second will send out a pulse indicating a new second. As soon as the MUs receive the pulse, the MU-A1 and MU-A2 will reset their SmpCnt counter to Zero, simultaneously, thus ensuring that the sampling in MU-A1 and MU-A2 remains in sync. Inside the relay the samples from MU-A1 and MU-A2 are arranged according to their Smpcnt counter. This ensures that the samples from both MUs are aligned correctly. Note that the SmpCnt does not take into account the network delay, rather it just represents the counter value when the sample was taken at the MU since the start of the second. Essentially, SmpCnt acts as a timestamp within a given second. This allows the correct translation of timing information of the samples from the MU into the timestamps of the 87L relay, as discussed later in this paper.

- **SynchSrcID/GmIdentity**: This attribute contains the Grandmaster Identity (GMID) of the clock source to which clock a particular MU is synchronized to. For the example in Figure 2, SynchSrcID fields sent BY MU-A1 and MU-A2 will contain the GMID of the synchronizing clock labeled as 1PPS. The importance of this field lies in the fact that in case of a loss of global time source, this field will indicate that to which particular local clock a particular MU is synchronized. This information will help in determining whether to keep 87L operational or not when a system loses global time reference as shown later in Section II-B. Note that it is assumed that time synchronization of MU and the relay is done via PTP because if the synchronization is done via IRIG-B then this field remains empty.

Figure 3 shows a transmission line protected by 87L element based on SAVs at both terminals. In Figure 3 (a), MU-A and Relay-A are synchronized to Clock-A, MU-B and Relay-B are synchronized to Clock-B. Both Clocks i.e., Clock A and Clock-B are synchronized to a global time reference (IRIG-B, GPS etc). Relay-A and Relay-B are synchronized to each other using Ping-pong algorithm. In Figure 3 (b), there are 2 clocks on Terminal-A with MU-A synchronized to Clock-A1, while Relay-A is synchronized to Clock-A2. For the sake of simplicity of analysis, the following values are fixed at:

- the sampling frequency of MU-A and MU-B is 4800Hz;
- the total delay for a sample from the sampling instance at MU-A to reaching the terminals of Relay-A is equivalent to 3 sample counts (=0.625ms) while for MU-B to Relay-B delay is 13 sample counts (=2.708ms). Note that the relays are not ‘aware' of these delays.
- the resolution of the timestamps that Relay-A and B are exchanging over ping-pong algorithm matches the resolution of the MUs (i.e., the relay timestamps vary from 0 to 4799);

These assumptions do not limit the analysis in anyway. Other values could also be used, but the analysis remain the same. Now let us examine the use cases under various contingencies.

A. No Contingency

In this case, there is no contingency in the synchronizing source network (see Figure 3 (a)), i.e., Clock-A and Clock-B are synchronized with a global time reference; both relays and MUs are synchronized to their respective clocks. The global synchronization of both clocks mean that Clock-A and B will receive their pulse per second (PPS) pulses at the same time instance. Table I shows the key events with the passing of time (with the flow of time from top to bottom) when there is no contingency in the SAV-based 87L system. Both MU's and relays receive the PPS simultaneously. The timestamps of Relay-A and Relay-B when 1PPS was received read 134. Both relays mark Timestamp-134 as when the PPS was received. The MU's make the SmpCnt of the next samples '0'. Now to showcase the proper alignment of samples for 87L, the sample with SmpCnt =12 has been selected in this paper. Any other sample number (0 to 4799) could also be selected, the analysis remains the same.

The samples with SmpCnt=12 are sampled By MU-A and MU-B when the timestamps of the Relay-A and B are 146 (=134+12). The sample SmpCnt=12 from MU-A will arrive at Relay A with a delay of 3 samples, i.e., when the Timestamp at relay is 149 (=146+3). Even though the sample is received at the Relay-A when relay timestamp is 149, however, Relay A can still apply correct timestamp of 146 to the sample because Relay-A 'knows' that PPS occured when its timestamp was 134. Therefore, the sample with SmpCnt=12 must have been taken at the Timestamp-146 (=134+12). Similarly, the sample with Smpcnt=12 from MU-B will arrive at Relay-B with a delay of 13 samples, when the timestamp of Relay-B is 159 (=146+13). Since, Relay-B has marked the Timestamp-134 when the PPS was received, it can apply the correct timestamp 146 (=134+12) of by using SmpCnt value of 12. Thus, it can be seen that even though the samples with the same SmpCnt were received by the relays at different time instances, the relays were still able to apply the correct timestamps.

The analysis presented here also applies to the system of Figure 3 (b) when 2 different clocks, Clock-A1 and Clock-A2 exist on Terminal-A and both clocks have global time reference. Since both clocks have a common reference (which is also global), both clocks are synchronized to each other and can be treated as one clock.

Table I: Operation of SAV-based 87L with no contingency

Time	PPS		SmpCnt MU		TimeStamp		Remarks
	Clock 1	Clock 2	MU-A	MU-B	Relay-A	Relay-B	
↓			4798	4798	132	132	The relays are synchronized through PingPong; will have identical or near identical Timestamps
			4799	4799	133	133	
	Yes	Yes	0	0	134	134	PPS is received by both relays and MUs. MUs reset the SmpCnt to 0. Each relay marks the Timestamp-134 when PPS occurred.
			1	1	135	135	
			—	—	—	—	
			12	12	146	146	The samples with SmpCnt=12 is sampled at both MUs, at the same instance. These samples have not arrived at the Relays yet.
			—	—	—	—	
			15	15	149	149	The sample with SmpCnt=12 from MU-A arrives at Relay-A at Timestamp-149 (3 sample count delay). For Relay-A, the PPS occurred at Timestamp-134, the SmpCnt=12 implies that it was sampled at at Relay-A's Timetsamp-**146** (=134 + 12).
			—	—	—	—	
			25	25	159	159	The sample with SmpCnt=12 from MU-B arrives at Relay-B at Timestamp 159 (13 sample count delay). For Relay-B, the PPS occurred at Timestamp 134, the SmpCnt=12 implies that it was sampled at Relay-B's Timetsamp-**146** (=134 + 12).

B. Global time reference lost at one or all ends

Assume that both terminals lose antenna represented by contingency 'X1' in Figures 3 (a) and (b). As explained below the impact of the loss of global time reference will be different in the topology of Figure 3 (a) vs. Figure 3 (b).

1) All devices at a terminal are synchronized to the same local clock: In Figure 3 (a), the Clock-A and Clock-B have lost GPS/antenna (denoted by contingency 'X1'). However, the Clock-A and Clock-B are still providing the time reference albeit a local reference, i.e., MU-A and Relay-A are still synchronized to Clock-A, while MU-B and Relay-B are synchronized to Clock-B. Assume, the drift between Clock-A and Clock-B is 1 sample count, with Clock-A leading by 1. This means the samples with SmpCnt=12 from MU-A and SmpCnt=11 from MU-B will correspond to the same time instance.

In Table II, MU-A and Relay-A receive 1PPS when Relay-A Timestamp reads 134, while MU-B and Relay-B receive 1PPS when Relay-B Timestamp reads 135. Relay-A marks Timestamp-134, while Relay-B marks Timestamp-135 when it received its 1PPS. The samples with SmpCnt=12 from MU-A and SmpCnt=11 from MU-B are sampled when the Timestamps at both relays read 146. The sample with SmpCnt=12 from MU-A, arrives at Relay-A terminals at Timestamp-149 with a delay of 3 samples. Relay-A has marked Timestamp-134 when it received its 1PPS, the SmpCnt=12 implies that sample was taken at Timestamp-146 (=134+12). On the end, the sample with SmpCnt=11 from MU-B arrives at Relay-B terminals at Timestamp-159 with a delay of 13 samples. Since, Relay-B has marked Timestamp-135 when it received its 1PPS, the SmpCnt=11 implies that the sample was taken at Timestamp146 (=135+11). It can be seen that even though different SmpCnt value was assigned to the samples taken at the same instance, the samples were still aligned properly. Thus, the

87L can be kept operational as long as all the devices (MU(s) and Relay) at any given terminal are all synchronized to the same time reference. This time references can be a local or global reference.

Table II: Operation of SAV-based 87L with local time reference at one or all ends with 1 clock per terminal: Contingency 'X1' in Figure 3 (a)

Time	PPS		SmpCnt MU		TimeStamp		Remarks
	Clock 1	Clock 2	MU-A	MU-B	Relay-A	Relay-B	
↓			4798	4797	132	132	The relays are synchronized through PingPong; will have identical or near identical Timestamps
			4799	4798	133	133	
	Yes		0	4799	134	134	PPS is received by MU-A and Relay-A. MU-A resets the SmpCnt to 0. Relay-A marks the Timestamp-134 when PPS occurred.
		Yes	1	0	135	135	PPS is received by MU-B and Relay-B. MU-B resets the SmpCnt to 0. Relay-B marks the Timestamp-135 when PPS occurred.
			—	—	—	—	
			12	11	146	146	The sample with SmpCnt=12 is sampled at MU-A while sample with SmpCnt=11 is sampled at MU-B. Note that samples SmpCnt=12 at MU-A and SmpCnt=11 at MU-B correspond to the same time instance. These samples have not arrived at the Relays yet.
			—	—	—	—	
			15	14	149	149	The sample with SmpCnt=12 from MU-A arrives at Relay-A at Timestamp 149 (3 sample count delay). For Relay-A, the PPS occurred at Timestamp-134, the SmpCnt=12 implies that it was sampled at at Relay-A's Timetsamp-**146** (=134 + 12).
			—	—	—	—	
			25	24	159	159	The sample with SmpCnt=11 from MU-B arrives at Relay-B at Timestamp 159 (13 sample count delay). For Relay-B, the PPS occurred at Timestamp-135, the SmpCnt=11 implies that it was sampled at Relay-B's Timetsamp-**146** (=135 + 11).

2) All devices at the terminal are ***not*** *synchronized to the same local clock:* In Figure 3 (b), the Clock-A1, Clock-A2 and Clock-B have lost GPS/antenna (denoted by contingency 'X1'). At Terminal-B, the Relay-B and MU-B are synchronized to the same local clock, therefore the timestamping of samples will be correct at Terminal-B as explained in the above example. However, at Terminal-A, the MU-A is synchronized to Clock-A1 while Relay-A is synchronized to Clock-A2. Since, the Clock-A1 and Clock-A2 do ot have any common reference, the accuracy of timestamping of the samples will deteriorate as Clock-A1 and Clock-A2 drift mutually. To analyze this case assume that the drift between Clock-A1 and Clock-A2 is equivalent to 5 samples with Clock-A1 Leading.

In this example as shown in Table III, MU-A receives 1PPS when Relay-A Timestamp reads 134, while Relay-A receive 1PPS when Relay-A Timestamp reads 139. Relay-A marks Timestamp-139 when it received its 1PPS. The sample with SmpCnt=12 from MU-A is sampled when the Timestamp at Relay-A reads 146. This sample from MU-A arrives at Relay-A terminals at Timestamp-149 with a delay of 3 samples. Since, Relay-A has marked Timestamp-139 when it received its 1PPS, the SmpCnt=12 implies that sample was taken at Timestamp-151 (=139+12), which is clearly wrong. It can thus be observed that drift of 5 samples between Clock-A1 and Clock-A2 manifests as 5 sample error in timestamping of the samples (wrong timestamp of 151 is applied instead of 146). This error will result in a fictitious differential current. Therefore, for the cases when the relay and the corresponding merging unit are synchronized to different clocks, and the global (common) time reference is lost then 87L should be blocked.

Table III: Operation of SAV-based 87L with local time reference at one or all ends with multiple clocks per terminal: Contingency 'X1' in Figure 3 (b)

Time	PPS		SmpCnt MU	TimeStamp	Remarks
	Clock-A1	Clock-A2	MU-A	Relay-A	
↓			4798	132	The relays are synchronized through PingPong; will have identical or near identical Timestamps
			4799	133	
	Yes		0	134	PPS is received by MU-A and resets the SmpCnt to 0. Relay-A does not receive PPS yet.
			—	—	
		Yes	5	139	PPS is received by Relay-A. Relay-A marks the Timestamp-139 when PPS occurred.
			—	—	
			12	146	The sample with SmpCnt=12 is sampled at MU-A. The samples have not arrived at the Relays yet.
			—	—	
			15	149	The sample with SmpCnt=12 from MU-A arrives at Relay-A at Timestamp-149 (3 sample count delay). For Relay-A, the PPS occurred at Timestamp-139, the SmpCnt=12 implies that it was sampled at at Relay-A's Timetsamp-**151** (=139 + 12). Drift between Clock-A1 and Clock-A2 causes the Relay-A to apply wrong timestamp to the samples. 87L should be **blocked**

C. No time reference is available to at least 1 Relay or MU

In this scenario, both MUs and Relay-A are synchronized to global time reference while Relay B is not synchronized to any time source, represented by contingency 'X2' in Figure 3 (a). The analysis of this case will also be applicable if Relay-B is synchronized to a local source while both MUs and Relay-A are still synchronized to a global source. Bottom line is that this case is applicable whenever all the devices at one given terminal are not synchronized mutually to a common timing source.

The Table IV shows chronology of events for this case, where both MUs and Relay-A receive the 1PPS when timestamps of Relay-A and Relay-B read Timestamp-134. Both MUs reset the SmpCnt to 0; Relay-A marks the Timestamp-134 when 1PPS occurred. Note that Relay-B does not receive 1PPS, so it cannot mark Timestamp-134 as when 1PPS occurred. Since both MUs are synced to the same global source, the samples with Smpcnt=12 are taken at the same time instance. The sample with SmpCnt=12 from MU-A, arrives at Relay-A terminals at Timestamp 149 with a delay of 3 samples. Relay-A has marked Timestamp-134 when it received its 1PPS, the SmpCnt=12 implies that sample was taken at Timestamp-146 (=134+12). The sample with SmpCnt=12 from MU-B, arrives at Relay-B terminals at Timestamp 159 with a delay of 13 samples. However, the Relay-B did not recieve the 1PPS signal and it does not 'know' that delay for a sample to arrive from MU-B to its terminal is 13 samples. Therefore, Relay-B cannot reliably apply the correct timestamp to the sample. If Relay-B assumes that there is no delay in the network, it will apply Timestamp-159 to the sample, thus introducing an error equivalent to 13 samples (=Timestamp-B - Timestamp-A=159-146) in the sample alignment. This error will result in a fictitious differential current. Therefore, for such cases 87L should be blocked.

Table IV: No time reference is available to at least 1 Relay or MU: Contingency 'X2' in Figure 3 (a)

Time	PPS		SmpCnt MU		TimeStamp		Remarks
	Clock 1	Clock 2	MU-A	MU-B	Relay-A	Relay-B	
↓			4798	4798	132	132	The relays are synchronized through PingPong; will have identical or near identical Timestamps
			4799	4799	133	133	
	Yes	Yes	0	0	134	134	PPS is received by both MUs and Relay-A. MUs reset the SmpCnt to 0. Relay-A marks the Timestamp-134 when PPS occurred. The Relay-B **does not** receive 1PPS.
			1	1	135	135	
			—	—	—	—	
			12	12	146	146	The samples with SmpCnt=12 is sampled at both MUs, at the same instance. These samples have not arrived at the Relays yet.
			—	—	—	—	
			15	15	149	149	The sample with SmpCnt=12 from MU-A arrives at Relay-A at Timestamp-149 (3 sample count delay). For Relay-A, the PPS occurred at Timestamp-134, the SmpCnt=12 implies that it was sampled at at Relay-A's Timetsamp-**146** (=134 + 12).
			—	—	—	—	
			25	25	159	159	The sample with SmpCnt=12 from MU-B arrives at Relay-B at Timestamp-159 (13 sample count delay). As Relay-B does not have 1PPS reference, it cannot correctly account for 13 samples delay. 87L should be **blocked**.

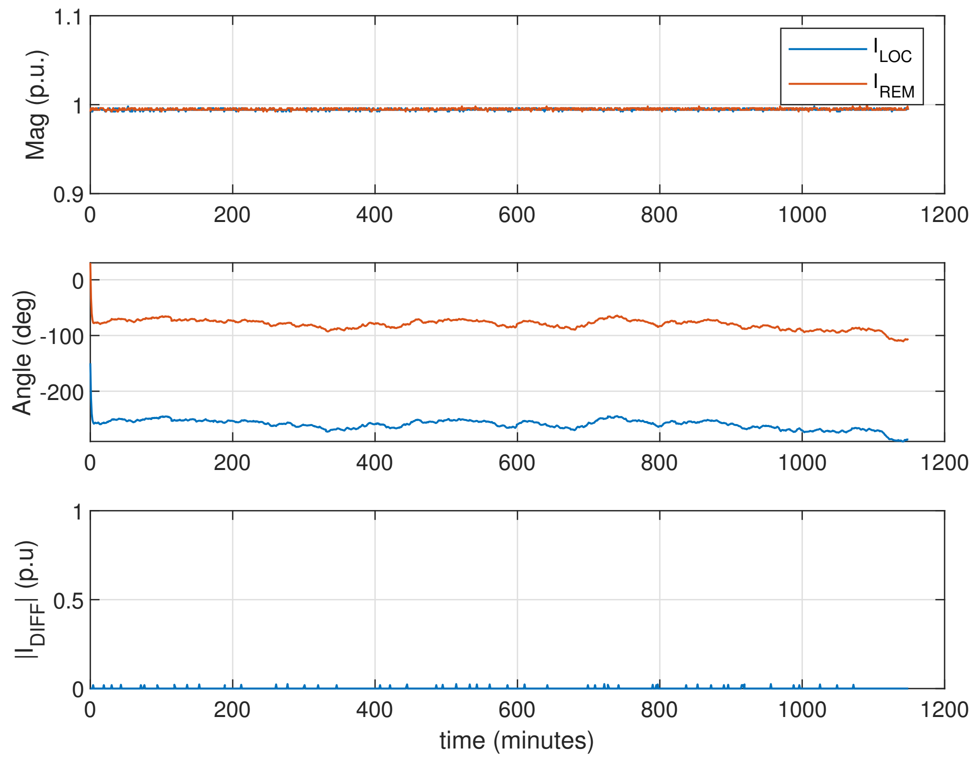

Figure 4: Relay-A and MU-A synced to the same local clock: Current phasors and Differential current in Phase-A

III. Test Results

The previous section presented the analytical evaluation of the various clock related contingencies in SAV-based 87L system. In this section, the test results using actual 87L relays are presented. A no fault condition is simulated by injecting a 1 p.u. current which enters the one terminal and leaves through the other terminal implying a ZERO differential current. The test cases were allowed to run for up to approximately 20 hours.

The first case is represented by the contingency 'X1' in Figure 3 (a), i.e., the clocks at both ends of the transmission line have lost the global time reference but Relay-A & MU-A and Relay-B & MU-B are synchronized to the same local clocks at their respective terminals. The results are shown in Figure 4. It can be seen that the magnitudes and the angles of the local and remote phase-A currents remain stable throughout. The magnitudes of the local and remote currents are almost identical with each measuring 1p.u. while the angles of the the local and remote currents are approximately 180^o apart. Thus, leading to near ZERO differential current throughout. It proves that as long as Relay and its corresponding MU(s) are synchronized to a common local clock at all ends, the 87L can be safely operated, even when global time reference is lost at all terminals.

The second case is represented by contingency 'X1' in Figure 3 (b), i.e., the clocks at both ends of the transmission line have lost global time reference; Relay-B & MU-B are synchronized to the same local clock while Relay-A & MU-A are synchronized to different local clocks. The results are shown in Figure 5. It can be observed that the magnitudes of the local and remote currents remain identical to each other but the phasor angles of the local and remote currents start drifting from each other gradually. This angle shift is due to the drift between the Clocks-A1 and A2. At the beginning of the test the angles of the local and remote currents are approximately 180^o apart, leading to almost ZERO differential current. As the test progressed, the phasor angles start drifting from each other and as a result 'fictitious' differential current appears. By about 20 hours, the angles difference between the local and remote currents is approximately 150^o, resulting in 'fictitious' differential current close to 0.5p.u.. It shows that in the absence of a global time reference, if the relay and its corresponding MUs are not synchronized to a common local clock then 87L could potentially be operated securely for few minutes to hours depending upon the accuracy of clock crystals. Ultimately, 87L will not remain secure and should be blocked.

IV. Existing topologies of 87L element based on SAV and Results

In this section, the different topolgies of SAV-based 87L element are discussed along with the results under various contingencies. It is assumed that communication path for the ping pong algorithm are symmetrical, i.e., the time taken by a message to go from Terminal-A to Terminal-B is same as the time taken by the message to travel from Terminal-B to

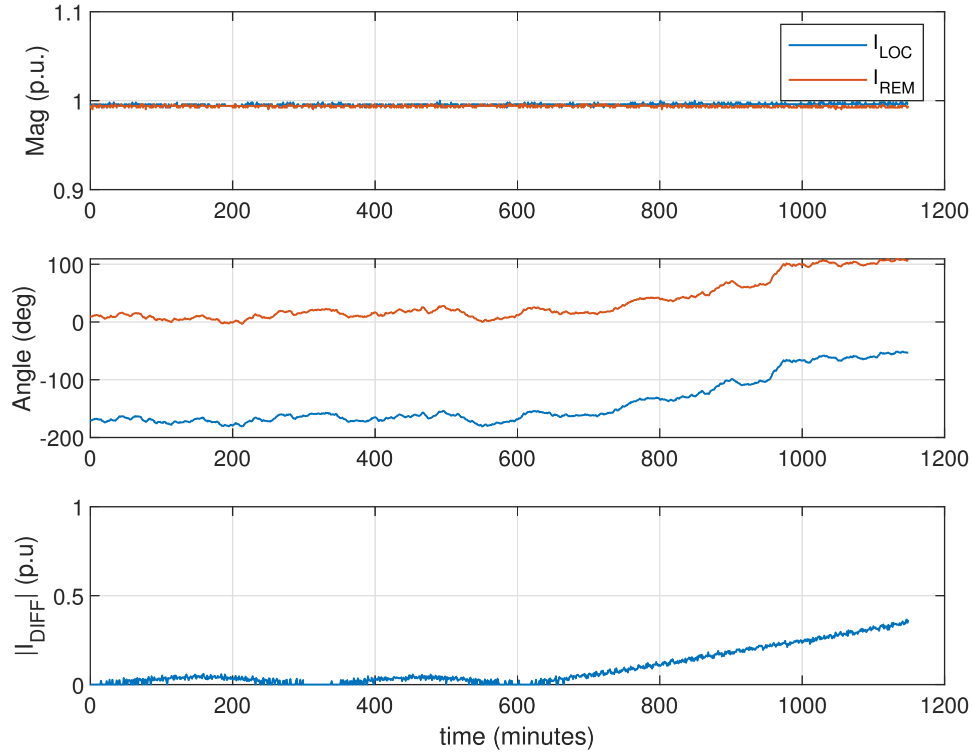

Figure 5: Relay-A and MU-A synced to the different Local clocks: Current phasors and Differential current in Phase-A

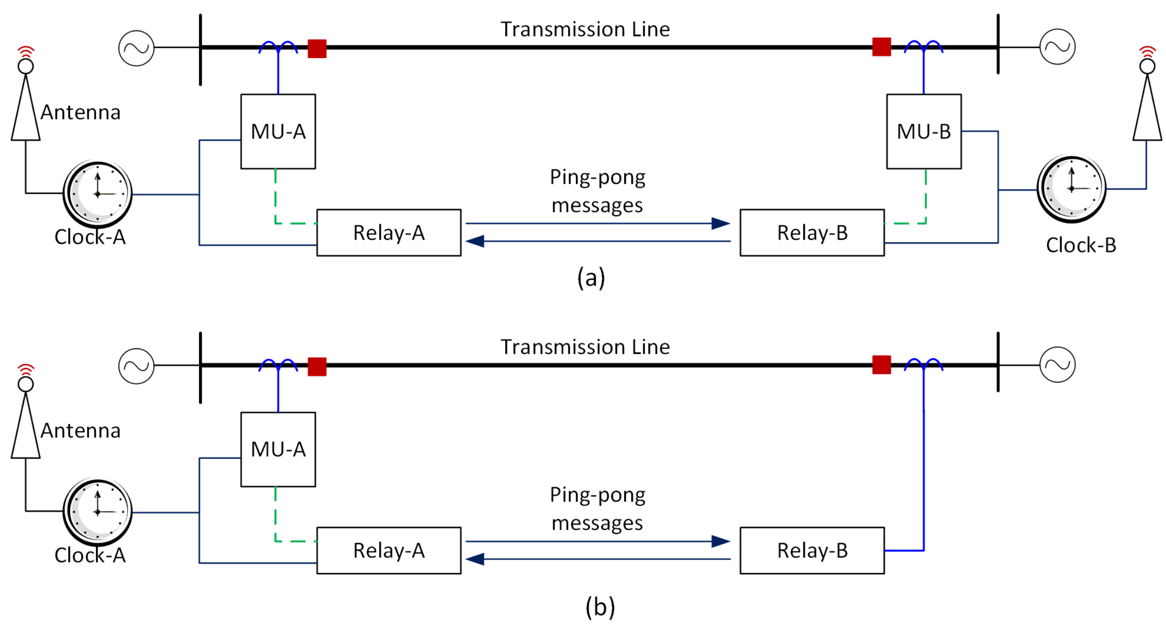

Figure 6: Existing topologies SAV-based 87L system: (a) SAV-SAV 87L System; (b) SAV-Hardwired 87L System

Terminal-A. If the communication path between Relay-A and B is not symmetrical, then having global time source is a must.

A. SAV-SAV 87L System

This topology of SAV-based 87L system is the one which is discussed in detail in Section II and is shown in Figure 6(a). In this system, the relay at both terminals (all terminals for multiple terminal application) obtain their samples through SAVs. Both relays and MUs are synchronized to an external clock which is is in turn synchronized to a global time source. Following are the few scenarios based on the availability of the clock.

1) All terminals synchronized to Global clock: In this case, there is no contingency. 87L is secure and remains operational.

2) One or more terminals synchronized to Local Clock (GMIDs of MU and Relay match at all terminals): In this case, one or more terminals lose the global time reference, however, the relay and MU(s) at any affected terminal are synchronized to the same local clock. Therefore, the GmID of the relay and MU(s) at that affected terminal will match each other. For this scenario, 87L is secure and remains fully operational as discussed in Section II-B1.

3) One or more terminals synchronized to Local Clock (Mismatch of of MU and Relay GMIDs at least at one of the terminals): In this case, one or more terminals lose the global time reference, and the relay and MU(s) at at least one affected terminal(s) are synchronized to the different local clocks. Therefore, the GmID of the relay and MU(s) at that affected terminal will **not** match each other. 87L is not secure and it should be blocked as discussed in Section II-B2.

Another variation of this case, is that one or both of the devices (relay or MU) are not synchronized to any time source. For example, if Relay-B is not synchronized but the MU is synchronized to local clock (their GMIDs would not match) OR if MU-B is not synchronized to any clock, (its incoming SmpSynch attribute will become '0'), OR if both Relay-B and MU-B are not synchronized; the common factor in all these scenarios is that the Relay-B and MU-B are not synchronized to the same clock, therefore 87L element is not secure and must be blocked. This scenario is discussed in Section II-C

B. SAV-Hardwired 87L System

In this system relay at one of the terminals line obtains samples through SAVs (Relay-A) while the relay at the other terminal (Relay-B) obtains analog signals directly from CT/VTs through hardwired copper wire connections Figure 6(b). Various cases possible in this topology are as below:

1) Global clock available at Terminal-A: In this case, the Relay-A and MU-A are both synchronized to an external clock which in turn is synchronized to the global time reference. The 87L is secure and remains fully operational.

2) Local clock at Terminal-A (GMIDs of Relay-A and MU-A match): In this case, terminal-A loses the global time reference. The Relay-A and MU-A are synchronized to the same clock as indicated by the fact that GMID of the clock to which the Relay-A is synchronized matches the GMID of the clock to which the MU-A is synchronized. The 87L is secure and remains fully operational.

3) Local clock at Terminal-A (Mismatch of GMIDs of Relay-A and MU-A): As in the previous case, Terminal-A loses the global time reference. However, the Relay-A and MU-A are synchronized to the different clocks as the GMID of the clock to which Relay-A is synchronized is different from the GMID of the clock to which MU-A is synchronized. Another variation of this case, is that one or both of the devices (Relay-A and/or MU-A) are not synchronized to any time source. If Relay-A is not synchronized but the MU-A is synchronized to local clock, then their GMIDs would not match. If MU-A is not synchronized to any clock, its incoming SmpSynch attribute will become '0'. The common denominator is all these cases is that Relay-A and MU-A are not synchronized to the same clock, therefore 87L element is not secure and must be blocked.

V. Future possible topologies of 87L relays

Sending the SAVs over a network have opened up avenue for new possible topologies of 87L system. Few topologies are discussed below briefly, the feasibility of which can be explored in future:

A. One relay and multiple MUs

In legacy 87L applications, the relays were located at each terminal of the transmission line. Each relay would perform signal acquisition, communicate the received current and/or voltage measurements and run 87L calculations. Each relay acted as master as long as each relay could communicate to all its peers. When due to network problem a relay could only send but not receive the current/voltage measurements from the other end, it would run in slave mode. That is the relay is primarily doing signal acquisition and then communicating the signals. The relay which receives the measured signals from all other relays, runs in master mode and runs the 87L calculation.

Now with the emergence of the MUs, the relays at the all terminals can be replaced with MU's which will sample the current/voltage signals and then forward the measured signals to the only relay present in the 87L system which will perform the 87L calculations as shown in Figure 7 (a). The key requirements for the successful would be that all the MUs will need to be synchronized to the same time source (preferably a global one) and in case of a tripping, the trip signal will have to be conveyed to the each terminal.

B. Operating SAV-based 87L without depending upon Clocks

In this scheme, each relay while synchronized to other relays via ping-pong method, also becomes the PTP grandmaster clock, i.e., the synchronizing source at its terminal, thus, synchronizing the subscribed MUs as shown in Figure 7(b). This scheme can be used as the main scheme or as a back-up scheme as a result of the failure of clock(s). Note that in all previous topologies the MUs are sending the samples only which the relays consumed. However, for this topology to work each relay will very likely required to exchange time stamps with the its corresponding MU(s) to synchronize and correctly timestamp the samples.

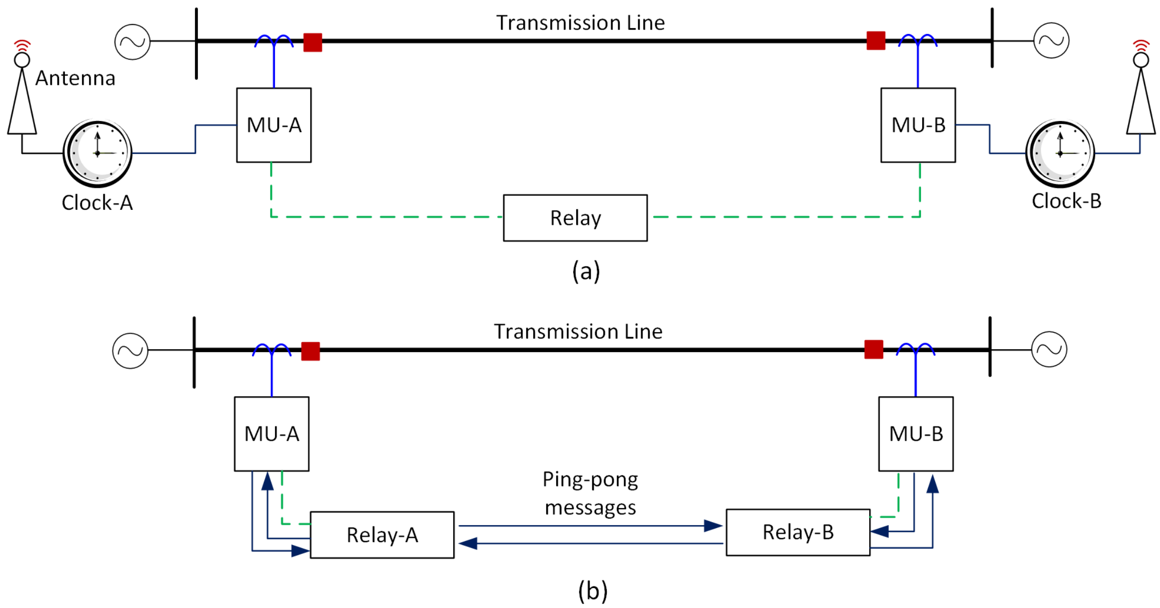

Figure 7: Possible topologies of SAV-based 87L system: (a) One relay with only MUs located at each terminal; (b) SAV-based system without any external clock

VI. Conclusion

In this paper, firstly the concept of synchronization of measurements from different terminal in legacy 87L relays is revisited, and it is shown that in SAV-domain the network delay needs to be properly accounted for to keep 87L secure. Thereafter, the attributes and terms of IEC-61850 such as *Variant Code, SmpSynch, SmpCnt, SynchSrcID/GmIdentity* which are related to the synchronization and time alignment of the SAVs were discussed. Thereafter, the analytical evaluation of different clock related contingencies in SAV-based 87L system and their potential impact on 87L element was presented. The key point derived from the analysis was that 87L can be kept securely operational only: 1-if all the MUs and the relays are synchronized to a global time reference; OR if all the MUs and the relays at any given terminal are synchronized to same local time reference. On the other hand, if at least one device (MU or Relay) at any given terminal is synchronized to a different local time source as compared to other devices OR that device is not synchronized at all, the measurements will not be aligned correctly; thus resulting in 'fictitious' differential current, and for such cases 87L element should be blocked. The analysis was further supported by the testing results produced using real relays, MUs and Clocks. Thereafter, the existing topologies of SAV-based 87L systems that are deployed in the field currently were discussed briefly. Lastly, the possible topologies of SAV-based 87L system that could be investigated and implemented in future were also introduced.

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