

Protection Centralization of a Direct Connect Static Var Compensator

Zachary Campbell, Principal Engineer, American Electric Power

Introduction:

American Electric Power (AEP) owns the nation's largest electricity transmission system, operating a more than 40,000-mile network that includes more 765-kilovolt extra-high voltage transmission lines than all other U.S. transmission systems combined, more than 223,000 miles of distribution lines, and producing approximately 30,000 megawatts, including more than 5,300 megawatts of renewable energy [1]. AEP also operates and maintains approximately 30 Flexible Alternating Current Transmission System (FACTS) and High Voltage Direct Current (HVDC) sites. This paper focuses on a FACTS site with a Static Var Compensator (SVC). SVC technology is well explained elsewhere[2] and will only briefly be discussed here. An SVC will often be found to be made up of bus-work, coupling transformers, Thyristor Controlled Reactors (TCR), Thyristor Switched Capacitors (TSC), and harmonic filter banks. This equipment can be found alongside ancillary secondary systems that are required to operate this equipment like cooling, valve, control, and protection systems. Though not all this equipment is required for every SVC manufactured, a subset of these components will be found at any SVC. The SVC of study in this work is made up of 69kV bus-work, a single TCR branch, and three harmonic filter banks (single tuned at the 5th, 7th, and 15th harmonic). A simplified single line diagram of the SVC can be found in Fig. 1. As can be seen in Fig. 1, the harmonic filter banks offer a capacitive range of the SVC of 50MVar and the TCR, in conjunction with the harmonic filter banks, offers an inductive range of 40MVar.

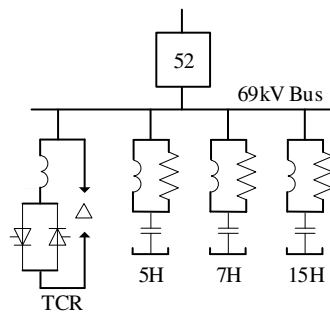


Fig. 1 - AEP Directly Connected SVC Facility Simplified One-Line Diagram

Motivation:

In 2024, this SVC is being refurbished to replace the original control, protection, and cooling control systems. The SVC was originally installed in 2006 and the refurbishment work is being motivated by replacement programs targeting hardware with operating systems no longer supported by OEMS as well as control and protection system hardware that has been deprecated by the original manufacturer. By strategically replacing the SVCs secondary systems to bring them into compliance with AEPs current operating practices, it is thought that the useful life of the SVC will be extended well into the future. Furthermore, this SVC is a duplicate of

four other facilities on the AEP footprint and the engineering work done to accomplish this refurbishment can be taken advantage of at each of the others in order to extend the life of each.

The traditional approach to this replacement project by AEP engineers would have been to install a set of redundant relays (two each) for each of the SVCs primary protection zones: three harmonic filter banks, the 69kV bus, and the TCR branch. This traditional approach would have resulted in five replacement panels with ten new relays. The existing control building in which the original relaying was installed did not have the space to handle this many panels or relays. These limitations required that the replacement protection system fit all the replacement componentry into the same physical space as the original. Additionally, consolidating protection systems into more dense and capable hardware benefits AEP customers by reducing protection system hardware costs. After considering the number of current transformers and voltage transformers that the existing protection used for protection purposes, it was observed that one set of protection relays (one redundant pair), could potentially, measure all the instrument transformers that were originally present for protection purposes. This observation led protection engineers to pursue an approach to consolidate and centralize all the protection of the existing SVC into one pair of redundant relaying.

Existing protection:

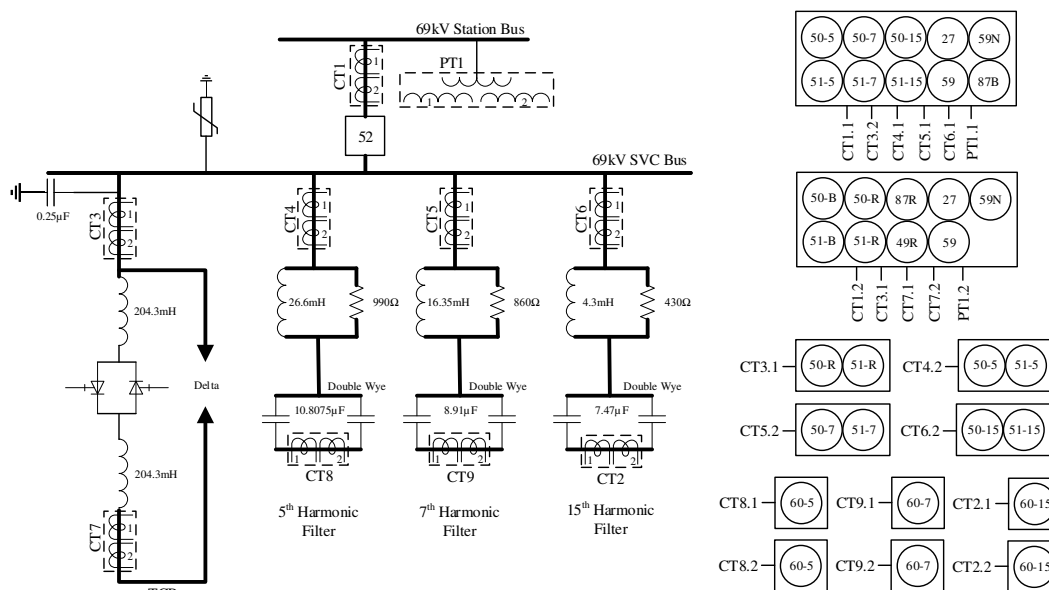


Fig. 2 – Existing AEP Directly Connected SVC Facility Protection Block Diagram

In the pursuit of determining what protection functions needed to be included in the pair of redundant relaying the engineering team needed to determine what protection functions were currently in use at the facility. Fig. 2 shows a single line diagram of the facility with the legacy protection functions measuring instrumentation and hardware shown. This diagram illustrates that the original protection design implemented two three phase differentials at the facility. The first was a bus differential function which wrapped the main breaker and each of the SVC branches up to the location of a set of three free-standing CTs within each SVC branch: the three

harmonic filter banks and the TCR branch. The second was a typical TCR branch differential, with phase zones that begin at the TCR branch wye connections and end within the delta, and whose zone configuration can be seen in Fig. 3. Each SVC branch current had redundant instantaneous and inverse time overcurrent functions except for the SVC main circuit breaker whose overcurrent functions were non-redundant. Fig. 2 also shows that the SVC previously had redundant phase under and over-voltage functions as well as redundant calculated residual overvoltage functions. The TCR branch was also protected with a non-redundant thermal overload element. The double-wye harmonic filter banks also deployed fully redundant unbalance elements, each on their own hardware. As can be seen in Fig. 2, all the initial SVC protection hardware was deployed across twelve protective relays. These twelve relays were housed in two panels which were fully populated because of so much hardware being deployed within them.

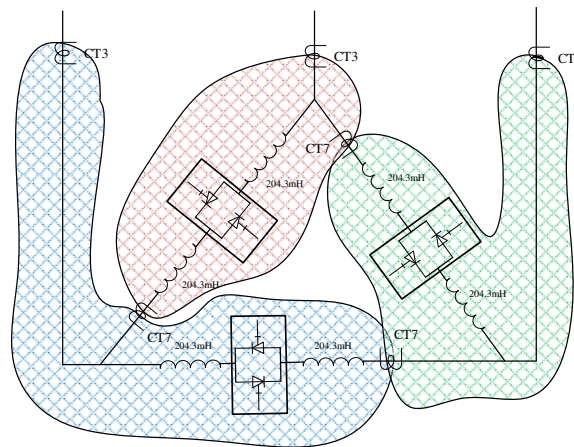
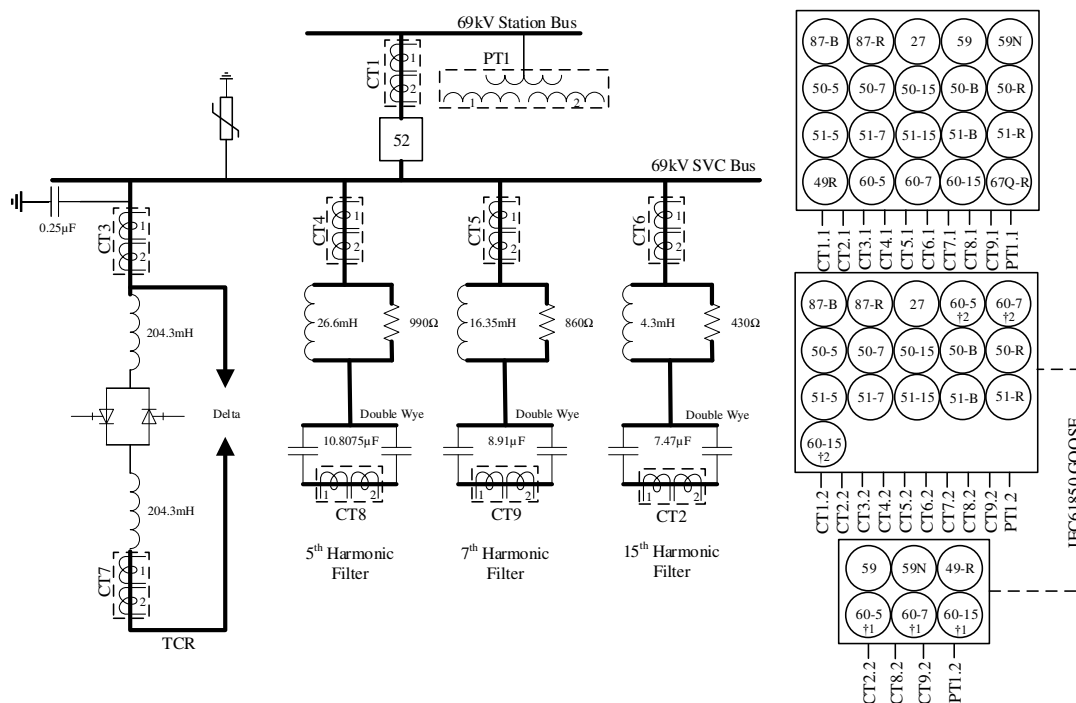


Fig. 3 – TCR Branch Conventional Differential Zone Configuration

Centralization:

Once all the protection functions initially present at the facility were understood and accounted for, AEP engineers began identifying which modern protective relaying platforms could not only measure all the existing instrument transformers but deploy all the existing protection functions on these newer relaying platforms. It can be observed in Fig. 2 that the existing CT instrument transformers total twenty-one and there is one set of three phase potential transformers measuring 69kV bus voltage. As a modern approach to protective relaying hardware platform selection, AEP deploys two different manufacturers hardware so-as to avoid common mode failure concerns. The team identified two commonly used protective relays that could measure twenty-one current transformers and one set of three phase voltages. These relays are commonly deployed at AEP as bus differential relays. The next main task was to ensure that the selected hardware platforms could perform all the previously deployed protection element tasks. The goal here was to have all protection functions deployed previously be present on both newly selected, dual-redundant, protection hardware. This would mean that the two three-phase current differential elements, previously deployed across two different protection system hardware, would be consolidated into the new hardware. The selected hardware is capable of this because of some additional software enabled protection functions made through selection

options made during the ordering process of the hardware. The number of instantaneous and inverse-time overcurrent elements totaled fifteen, which both selected relays had the capability to perform by default. Each of the selected relays was also capable, by default, of performing undervoltage functions. Only one of the two selected relays could provide overvoltage functions. Neither of the selected relays could perform capacitor unbalance or thermal overload functions without modification. Furthermore, air-core reactor protection that could be used for TCR branch turn-to-turn fault detection using a negative sequence directional overcurrent element is not present in either of the selected relays.



In studying the harmonic filter bank unbalance current elements that were needed to be customized for the project, it was noticed that one of the harmonic filter banks was not built like

the others. The capacitor section of all three harmonic filter banks were built in the topology of a double-wye, ungrounded capacitor bank. In this configuration, a CT can be installed to measure the current across the star point of both individual wye connections of the capacitor sections. Current measured across this position is zero (or near zero) when the two wye connected capacitor banks that make up the double-wye have no failed elements and are well balanced. This method of protection is favored because the method is immune to external fault conditions. This capacitor bank configuration is traditionally made up of two equally sized, wye-connected capacitors [4]. What is different at the facility of interest is that one of the banks is not equally sized on either side of the double-wye sections; the left and right legs of the bank are not the same. A single-phase isometric drawing of this bank is shown in Fig. 5. As a result of this, there would be unequal current magnitude developed for the failure of capacitor elements on either side of the asymmetric double wye legs. Conventionally, the method of element failure detection uses the same current magnitude level comparators to determine levels upon which to generate alarming and tripping conditions. When using traditional current magnitude only based detection functions to protect against overvoltage conditions and element failures in these capacitor banks, the protection engineer must set the alarm and trip thresholds to the lowest value condition for which an alarm or trip condition is required, even if another circumstance would not require the action. This precaution ensures that the protection system responds to potential issues early enough to prevent damage to the bank components. An alternative approach involves considering both the magnitude and the angle of the current. By combining these two parameters, the protection engineer can more precisely identify problems within the bank and determine the appropriate actions needed for different conditions. To set up the protection to perform this protection task, the current flowing across the double-wye bridge of the mentioned asymmetric harmonic filter bank must be analyzed.

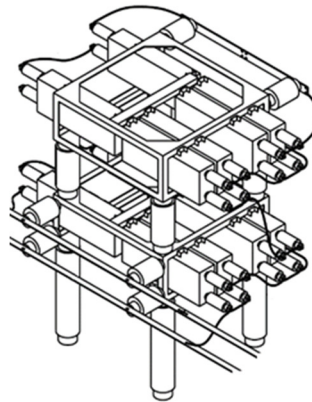


Fig. 5 – Isometric View of Asymmetric Double-Wye Capacitor Bank Section

Asymmetric Double-Wye Unbalance Element:

The following circuit, shown in Fig. 6, acts as a basis for the evaluation of all the double-wye harmonic filter banks at the facility of interest. The following analysis assumes that the resistors and inductors in the filter bank are equal and that the capacitor unit types at the facility are internally fused. The capacitances of each left and right leg of the three-phase section of the

capacitor bank (CLA, CRA, CLB, CRB, CLC, CRC) are each made up of an arbitrary number of parallel capacitances, either PL or PR, and an arbitrary number of series capacitances, SL or SR.

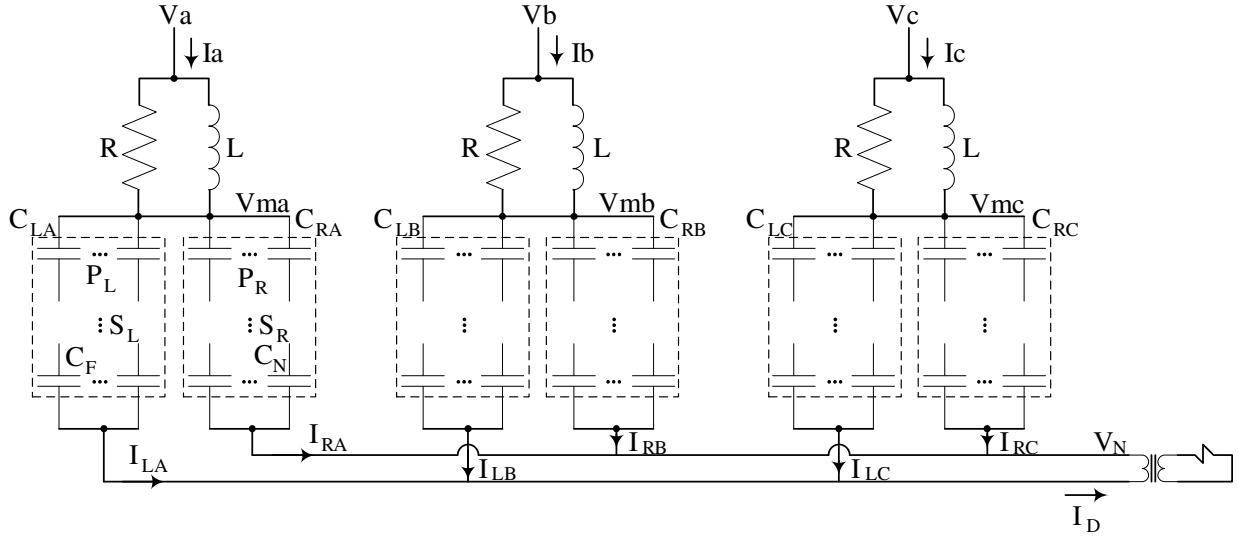


Fig. 6 – Three Phase Schematic of AEP Asymmetric Double-Wye Harmonic Filter Bank

Evaluation of the current summation at the star point of double-wye cap section of the bank will yield the following relationship, Eq. 1, where V_A , V_B , V_C , and V_N are the three phase voltages of the system as well as neutral and Z_A , Z_B , and Z_C are the three phase impedances.

$$\frac{V_A - V_N}{Z_A} + \frac{V_B - V_N}{Z_B} + \frac{V_C - V_N}{Z_C} = 0 \quad \text{Eq. 1}$$

Each of the three phase impedances of Eq. 1 can be written as follows.

$$Z_A = Z_{RL} + Z_{CA} = \frac{j\omega RL}{j\omega L + R} + \frac{1}{j\omega(C_{LA} + C_{RA})}, \quad Z_B = Z_{RL} + Z_{CB} = \frac{j\omega RL}{j\omega L + R} + \frac{1}{j\omega(C_{LB} + C_{RB})}, \quad \text{and}$$

$$Z_C = Z_{RL} + Z_{CC} = \frac{j\omega RL}{j\omega L + R} + \frac{1}{j\omega(C_{LC} + C_{RC})} \quad \text{where } C_{LA} \text{ is the capacitance of the entire phase A left leg, } C_{RA} \text{ is the capacitance of the entire phase A right leg, } C_{LB} \text{ is the capacitance of the entire phase B left leg, } C_{RB} \text{ is the capacitance of the entire phase B right leg, } C_{LC} \text{ is the capacitance of the entire phase C left leg, and } C_{RC} \text{ is the capacitance of the entire phase C right leg.}$$

Using the definitions above, Eq. 1 can be rewritten to form the following.

$$\frac{V_A}{Z_A} + \frac{V_B}{Z_B} + \frac{V_C}{Z_C} = V_N \left(\frac{1}{Z_A} + \frac{1}{Z_B} + \frac{1}{Z_C} \right) = V_N \left(\frac{Z_B Z_C + Z_A Z_C + Z_A Z_B}{Z_A Z_B Z_C} \right)$$

And solving for V_N yields:

$$V_N = V_A \left(\frac{Z_B Z_C}{Z_B Z_C + Z_A Z_C + Z_A Z_B} \right) + V_B \left(\frac{Z_A Z_C}{Z_B Z_C + Z_A Z_C + Z_A Z_B} \right) + V_C \left(\frac{Z_A Z_B}{Z_B Z_C + Z_A Z_C + Z_A Z_B} \right)$$

If $x = \frac{1}{Z_B Z_C + Z_A Z_C + Z_A Z_B}$, then:

$$V_N = V_A Z_B Z_C x + V_B Z_A Z_C x + V_C Z_A Z_B x \quad \text{Eq. 2}$$

By observation of Fig. 6, it can be observed that:

$$\frac{V_A - V_N}{Z_A} = I_A \text{ and } \frac{V_B - V_N}{Z_B} = I_B \text{ and } \frac{V_C - V_N}{Z_C} = I_C$$

Which can be rearranged to form the following:

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_A} & 0 & 0 \\ 0 & \frac{1}{Z_B} & 0 \\ 0 & 0 & \frac{1}{Z_C} \end{bmatrix} \begin{bmatrix} V_A - V_N \\ V_B - V_N \\ V_C - V_N \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_A} & 0 & 0 \\ 0 & \frac{1}{Z_B} & 0 \\ 0 & 0 & \frac{1}{Z_C} \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} - \begin{bmatrix} \frac{1}{Z_A} & 0 & 0 \\ 0 & \frac{1}{Z_B} & 0 \\ 0 & 0 & \frac{1}{Z_C} \end{bmatrix} \begin{bmatrix} V_N \\ V_N \\ V_N \end{bmatrix} \quad \text{Eq. 3}$$

$$\text{Eq. 2 can be represented as } \begin{bmatrix} V_N \\ V_N \\ V_N \end{bmatrix} = x \begin{bmatrix} Z_B Z_C & Z_A Z_C & Z_A Z_B \\ Z_B Z_C & Z_A Z_C & Z_A Z_B \\ Z_B Z_C & Z_A Z_C & Z_A Z_B \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad \text{Eq. 4}$$

Eq. 4 can be substituted into Eq. 3 to yield the following:

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_A} & 0 & 0 \\ 0 & \frac{1}{Z_B} & 0 \\ 0 & 0 & \frac{1}{Z_C} \end{bmatrix} \begin{bmatrix} V_A - V_N \\ V_B - V_N \\ V_C - V_N \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_A} & 0 & 0 \\ 0 & \frac{1}{Z_B} & 0 \\ 0 & 0 & \frac{1}{Z_C} \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} - x \begin{bmatrix} \frac{1}{Z_A} & 0 & 0 \\ 0 & \frac{1}{Z_B} & 0 \\ 0 & 0 & \frac{1}{Z_C} \end{bmatrix} \begin{bmatrix} Z_B Z_C & Z_A Z_C & Z_A Z_B \\ Z_B Z_C & Z_A Z_C & Z_A Z_B \\ Z_B Z_C & Z_A Z_C & Z_A Z_B \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}$$

$$\text{Which can be simplified to } \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_A}(1 - xZ_B Z_C) & xZ_C & xZ_B \\ xZ_C & \frac{1}{Z_B}(1 - xZ_A Z_C) & xZ_A \\ xZ_B & xZ_A & \frac{1}{Z_C}(1 - xZ_A Z_B) \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad \text{Eq. 5}$$

An additional set of relationships can be established from the circuit of Fig. 6. These relationships are:

$$\frac{V_A - V_{MA}}{Z_{RL}} = I_A \text{ and } \frac{V_B - V_{MB}}{Z_{RL}} = I_B \text{ and } \frac{V_C - V_{MC}}{Z_{RL}} = I_C$$

Which can be rearranged into matrix form as:

$$\begin{bmatrix} V_{MA} \\ V_{MB} \\ V_{MC} \end{bmatrix} = \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} - Z_{RL} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad \text{Eq. 6}$$

Substituting Equation 5 into Equation 6 allows the following relationships to develop:

$$\begin{bmatrix} V_{MA} \\ V_{MB} \\ V_{MC} \end{bmatrix} = \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} - Z_{RL} \begin{bmatrix} \frac{1}{Z_A}(1 - xZ_B Z_C) & xZ_C & xZ_B \\ xZ_C & \frac{1}{Z_B}(1 - xZ_A Z_C) & xZ_A \\ xZ_B & xZ_A & \frac{1}{Z_C}(1 - xZ_A Z_B) \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}$$

Which can be re-written as:

$$\begin{bmatrix} V_{MA} \\ V_{MB} \\ V_{MC} \end{bmatrix} = \begin{bmatrix} 1 - Z_{RL} \left(\frac{1}{Z_A} \right) (1 - xZ_BZ_C) & xZ_CZ_{RL} & xZ_BZ_{RL} \\ xZ_CZ_{RL} & 1 - Z_{RL} \left(\frac{1}{Z_B} \right) (1 - xZ_AZ_C) & xZ_AZ_{RL} \\ xZ_BZ_{RL} & xZ_AZ_{RL} & 1 - Z_{RL} \left(\frac{1}{Z_C} \right) (1 - xZ_AZ_B) \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad \text{Eq. 7}$$

Because $I_D = I_{LA} + I_{LB} + I_{LC}$, it must also be true that $I_D = \frac{V_{MA}-V_N}{Z_{CLA}} + \frac{V_{MB}-V_N}{Z_{CLB}} + \frac{V_{MC}-V_N}{Z_{CLC}}$

$$\text{The above can be re-written as } I_D = \left[\frac{1}{Z_{CLA}}, \frac{1}{Z_{CLB}}, \frac{1}{Z_{CLC}} \right] \begin{bmatrix} V_{MA} \\ V_{MB} \\ V_{MC} \end{bmatrix} - \left[\frac{1}{Z_{CLA}}, \frac{1}{Z_{CLB}}, \frac{1}{Z_{CLC}} \right] \begin{bmatrix} V_N \\ V_N \\ V_N \end{bmatrix} \quad \text{Eq. 8}$$

Substituting Eq. 7 and 4 into Eq. 8 yields:

$$I_D = \begin{bmatrix} \frac{1}{Z_{CLA}} \\ \frac{1}{Z_{CLB}} \\ \frac{1}{Z_{CLC}} \end{bmatrix}^T \begin{bmatrix} 1 - Z_{RL} \left(\frac{1}{Z_A} \right) (1 - xZ_BZ_C) & xZ_CZ_{RL} & xZ_BZ_{RL} \\ xZ_CZ_{RL} & 1 - Z_{RL} \left(\frac{1}{Z_B} \right) (1 - xZ_AZ_C) & xZ_AZ_{RL} \\ xZ_BZ_{RL} & xZ_AZ_{RL} & 1 - Z_{RL} \left(\frac{1}{Z_C} \right) (1 - xZ_AZ_B) \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} - \begin{bmatrix} \frac{1}{Z_{CLA}} \\ \frac{1}{Z_{CLB}} \\ \frac{1}{Z_{CLC}} \end{bmatrix}^T x \begin{bmatrix} Z_BZ_C & Z_AZ_C & Z_AZ_B \\ Z_BZ_C & Z_AZ_C & Z_AZ_B \\ Z_BZ_C & Z_AZ_C & Z_AZ_B \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}$$

Simplifying the above leads to the following:

$$I_D = \begin{bmatrix} \frac{1}{Z_{CLA}} \\ \frac{1}{Z_{CLB}} \\ \frac{1}{Z_{CLC}} \end{bmatrix}^T \begin{bmatrix} 1 - Z_{RL} \left(\frac{1}{Z_A} \right) (1 - xZ_BZ_C) - xZ_BZ_C & xZ_CZ_{RL} - xZ_AZ_C & xZ_BZ_{RL} - xZ_AZ_B \\ xZ_CZ_{RL} - xZ_BZ_C & 1 - Z_{RL} \left(\frac{1}{Z_B} \right) (1 - xZ_AZ_C) - xZ_AZ_C & xZ_AZ_{RL} - xZ_AZ_B \\ xZ_BZ_{RL} - xZ_BZ_C & xZ_AZ_{RL} - xZ_AZ_C & 1 - Z_{RL} \left(\frac{1}{Z_C} \right) (1 - xZ_AZ_B) - xZ_AZ_B \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad \text{Eq. 9}$$

Eq. 9 provides a framework for analyzing the current magnitude and phase angle in the previously discussed bank configuration topology. It shows that the current in the double-wye bridge depends solely on power system voltage and the impedances of the harmonic filter bank. For the analysis, we will assume that the power system provides balanced positive-sequence three-phase voltages and focus only on changes in the capacitor bank configuration. This approach allows us to plot the phasor of the bridge current (I_D) for different capacitor bank configurations as failures in parallel capacitor elements, for an internally fused capacitor unit, within a single capacitor unit, accumulate. Using the component values of Table 1, Fig. 7 was generated to illustrate the bridge current phasors as an increasing number of element failures occurs, within the labeled bank leg, under the labeled configurations. The legend labels in Fig. 7 denoting L or R prior to either A, B, or C refer to which side of the double-wye bank (left or right of the polarity marking of Fig. 6 circuit) and within which phase (A, B, or C) the failures are occurring. All plots shown in Fig. 7 have phasor magnitude and angles that start at the origin and extend outward as the number of element failures increases.

Table 1: Asymmetric Double-Wye Harmonic Filter Bank Component Values

Tuning Section Resistance	Tuning Section Inductance	Capacitor Unit Element Capacitance	Capacitor Unit Internal Series Elements	Capacitor Unit Internal Parallel Elements
990 Ω	27 mH	7.205 μF	6	12

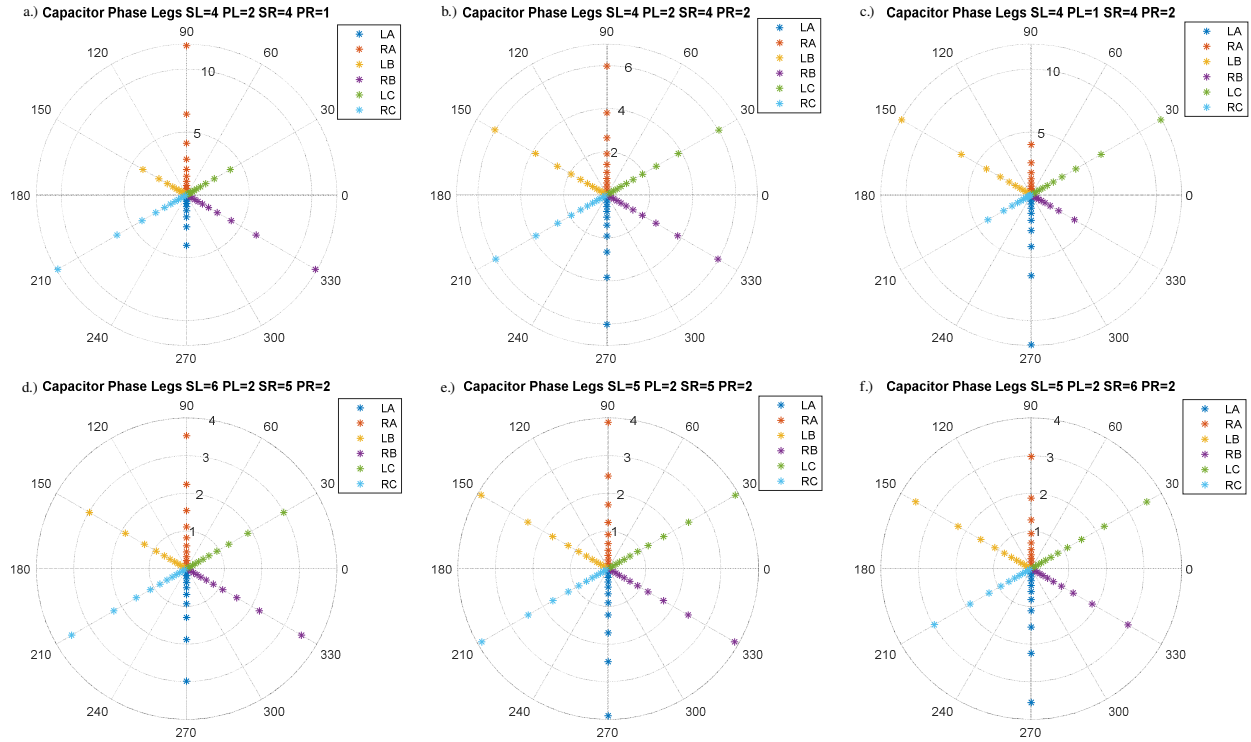


Fig. 7 – Bridge Current Phasors Under Increasing Parallel Element Failures

The typical symmetric double-wye capacitor bank bridge current phasor would appear like that seen in Fig. 7 plot b or e. These plots show that when there are an equal number of parallel and series capacitor units on either side of the double-wye bank, the magnitude of the bridge current is identical to when the same number of parallel element capacitor unit failures occur regardless of the phase or leg of the bank in which the failures have occurred. In all the phasor plots of Fig. 7, it can be observed that when the bridge CT is set up with shown polarity, the phasor angles of the bridge current remain the same during all the same scenario parallel leg failures for all the bank configurations shown. Plots a through c of Fig. 7 show that when there is an equal number of series capacitor unit element failures within the legs of the bank, those which have a greater number of parallel capacitor sections will result in a smaller magnitude of current as compared to when the opposing leg parallel element failures occur. Similarly, plots d through f show that when the banks are made up of equal numbers of parallel sections on either side of the bank, the side with the smaller number of series units will result in a greater magnitude of current during parallel element failures. In all the cases shown, the magnitude of the current in the all the left legs are the same and the magnitude of the current in all the right legs are the same for the same parallel element failures.

Once an understanding of the bridge current phasor trajectories under element failure conditions has been developed, an understanding of the voltage applied to the most stressed capacitor elements can be developed for these conditions. The circuit of Fig. 8 can be evaluated to find the voltage remaining on capacitor elements from the result of the failure of an arbitrary number of elements within a parallel group of a capacitor unit. It is this scenario that results in the greatest stress to individual capacitor unit elements. In this circuit, capacitor C_F represents

the capacitor with some number of elements out of operation, in a parallel group, due to internally fused elements becoming open-circuited. Capacitor C_N , represents the capacitance of a normal capacitor unit.

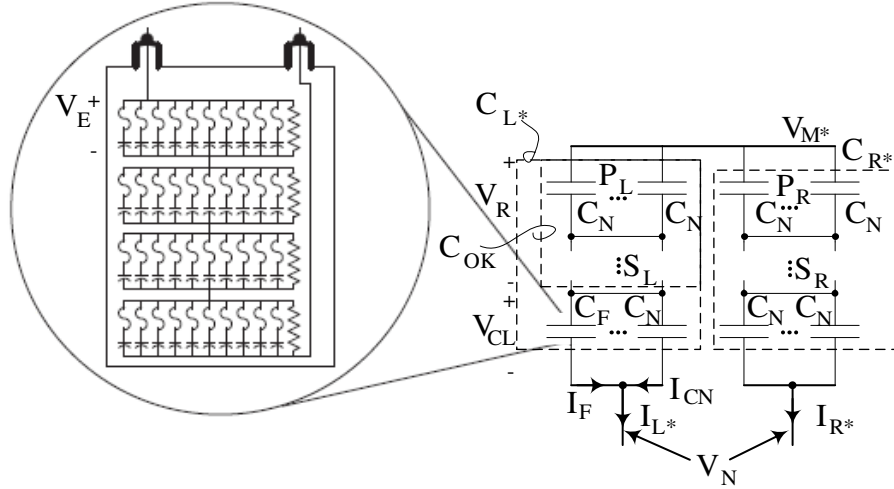


Fig. 8 – Capacitor Section of Asymmetric Double-Wye Harmonic Filter Bank

Evaluating the circuit of Fig. 8, the equation can be developed.

$$V_{M*} = V_R + V_{CL} + V_N \text{ rearranged, this is: } V_{CL} = V_{M*} - V_R - V_N \text{ Eq. 10}$$

And by evaluation of Fig. 8 circuit:

$$I_{L*} = I_F + I_{CN} \text{ Eq. 11}$$

$$\text{Where } I_{CN} = \frac{V_{CL}}{Z_{C_N}} \text{ Eq. 12} \quad \text{also } I_{CN} = V_{CL} j \omega C_N$$

Substituting Eq. 12 into 11 and rearranging terms yields the following:

$$I_F = I_{L*} - I_{CN} = I_{L*} - \frac{V_{CL}}{Z_{C_N}} \text{ Eq. 13}$$

$$\text{Substituting Eq. 10 into Eq. 13 generates } I_F = I_{L*} - \frac{V_{M*} - V_R - V_N}{Z_{C_N}}$$

Where, if the impedance of the healthy section of the bank, labeled as C_{OK} , is $Z_{C_{OK}}$, then

$$V_R = Z_{C_{OK}} I_{L*}. \text{ Which means } I_F = I_{L*} - \frac{V_{M*} - Z_{C_{OK}} I_{L*} - V_N}{Z_{C_N}}$$

Now that the failed unit current is determined, we can determine how much voltage remains across an individual element (V_E) by dividing the current across the number of remaining elements ($P_C - n$), where n is the number of element failures, and multiplying by an individual elements impedance ($1/j\omega C_E$).

$$V_E = \frac{\left(\frac{I_{L*} - \frac{V_{M*} - Z_{COK} I_{L*} - V_N}{Z_{CN}}}{(P_C - n)j\omega C_E} \right) \text{ and, for failures within the right leg, } V_E = \frac{\left(\frac{I_{R*} - \frac{V_{M*} - Z_{COK} I_{R*} - V_N}{Z_{CN}}}{(P_C - n)j\omega C_E} \right)$$

In the above the * designation denotes phase, and the value of V_{M*} can be determined from Eq. 7 and V_N from Eq. 4. If there are no parallel units in the bottom parallel section of the capacitor bank, $I_F = I_{L*}$ and, if the failure occurs within the right leg, $I_F = I_{R*}$. This means that $V_E = \frac{I_{L*}}{(P_C - n)j\omega C_E}$ and, if the failure occurs within the right leg, $V_E = \frac{I_{R*}}{(P_C - n)j\omega C_E}$.

The remaining element voltage (V_E' in PU of the capacitor unit) can be seen for the same element failure conditions seen in Fig. 7 a through f result in the same remaining element voltage plot a through f of Fig. 9. Plots a through c of Fig. 9 show that when there is an equal number of series capacitor units on either side of the bank the side which houses the smaller number of parallel segments will result in having a higher level of remaining element voltage than the side which has more parallel segments. Plots d through f of Fig. 9 show that when there is an equal number of parallel segments the side of the bank the side which houses a smaller number of series units will result in having a higher level of remaining element voltage than the side which houses more series units. As can be seen in plots d and e, the leg of the capacitor bank which has fewer series capacitors undergoes a more rapid increase in remaining element voltage as the number of elements failures increases. The likelihood of a capacitor bank built (or harmonic filter bank) being built like this would be low given the dissimilar behavior of the voltage applied to either side of the capacitor legs under normal conditions.

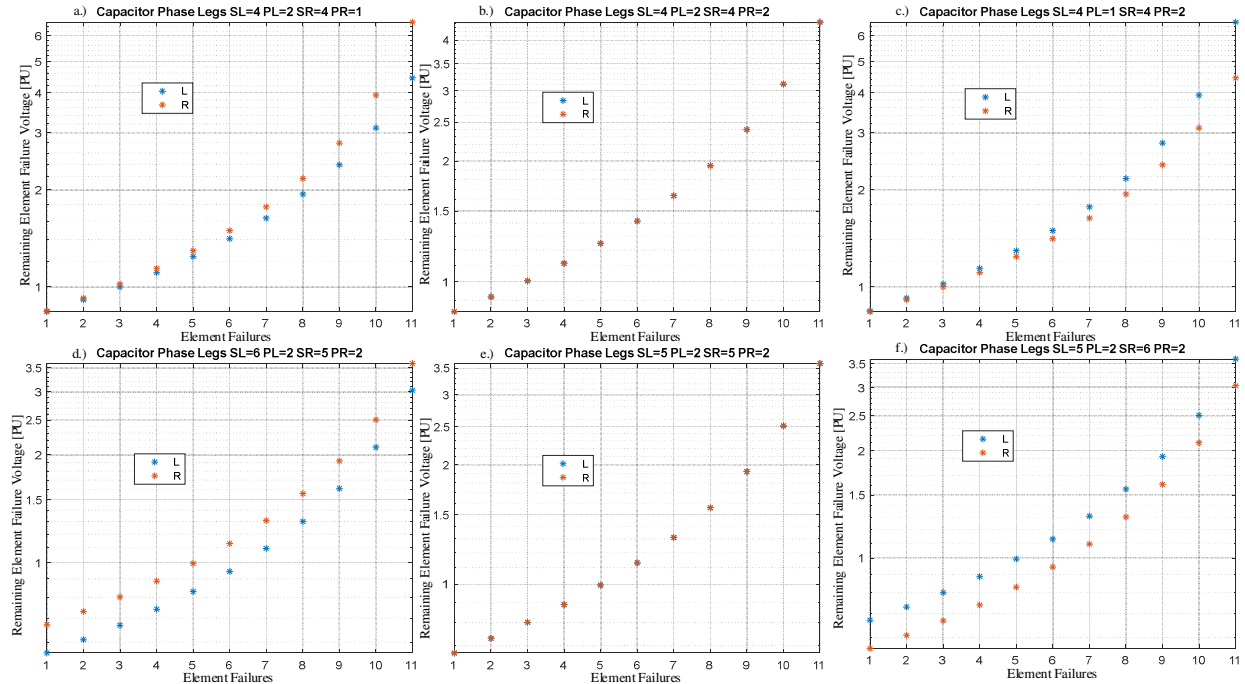


Fig. 9 – Most Stressed Element Per-Unit Voltage Under Increasing Element Failures

With the insights provided from Fig. 7 and Fig. 9 a few key concepts can be highlighted. It should be clear that when an asymmetric double-wye capacitor bank (or asymmetric double-

wye harmonic filter bank) undergoes increasing parallel element failures that the voltage stress across remaining elements within the same parallel segment is not the same as those that happen on the opposing side of the bank, and the magnitude of the current across the bridge is also different. These differences must be accounted for to ensure voltage stress of capacitor unit elements is not exceeded under increasing element failure conditions. However, if each of the phases are built with the same asymmetric construction (equal left leg construction and equal right leg construction), the same bridge current magnitude will exist for similar number of element failures for each half (left or right) for the same parallel element failure conditions. The case that has been studied and represents the asymmetric capacitor bank section used at the facility under study in this paper is the case in Fig. 7 plot a and Fig. 9 plot a (SL=4, PL=2, SR=4, PR=1). This case and the observations made so far lead to the development of a double-wye capacitor unbalance element with the operating region characteristic as that shown in Fig. 10. As this figure shows, the angle of the bridge current informs the operating characteristic as to which leg (left or right) the failure of any capacitor element may have failed. Due to the asymmetric nature of the bank, the magnitude of the current pickup element is different from one half of the bank to the next. Each phase and leg region characteristic is 60 degrees wide and has an alarm level pickup, and a slow trip level pickup to meet the needs of the voltage stress level differences that exist as a result of the asymmetry built into the banks.

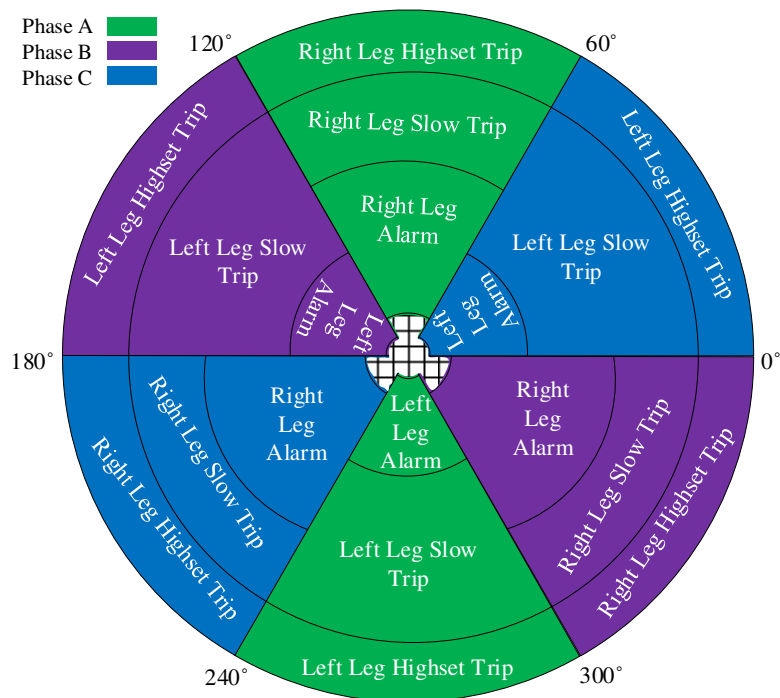


Fig. 10 – Asymmetric Double-Wye Capacitor Unbalance Element Characteristic

The Fig. 10 characteristic provides for alarm region operation, slow trip region operation, and a fast trip ('highset') region of operation. The threshold level comparison settings for the alarm level are based on historical operating procedure and are set to detect for a single element failure. The settings for the trip threshold level are based on C37.99 guidance stating that no more than 110% (1.1PU) of the rated RMS voltage or no more than 135% of nominal RMS

current should be applied to capacitors (or their elements) allowed to persist in operation [3]. Accumulated failures across parallel elements within a single capacitor unit are the assumed failure mode for this element. There is a very short time trip level characteristic that is meant to detect for rack fault conditions and has the same pickup level across all phases and legs. Others have produced similar operating characteristics with unbalance elements but not different pickup levels based on location within the bank [5].

Results:

Once the newly formed protection element was fully developed it was programmed into the selected relaying platforms using customizable logical programming. The unbalance element, like other sensitive unbalance elements, requires calibration (or compensation) of the unbalance element to zero out the inevitable, non-zero bridge current phasor that occurs as a result of not perfectly balancing the capacitances of the capacitor units of the capacitor banks. To accomplish this, each element was implemented with unbalance compensation so-as to zero-out the natural non-zero bridge current phasor after initial energization of the banks. RTDS testing was then performed to ensure proper operation of the element. Fig. 11 plot a and b demonstrates RTDS cases where a single internal fuse failure condition in both the left and right leg of the same phase of the 5th harmonic filter bank at the facility of interest occurs. As the figure shows, there is a nearly two-fold difference in the magnitude of the bridge current that occurs for a single element failure. The angles of the bridge currents for these failures illustrate the expected 180° phase difference between the conditions and both lie within the phase A regions as shown in the Fig. 10 element characteristic. The digital channels shown at the top of the plot illustrates the internal element recognition of when the alarm level conditions become adequate to begin timing before issuing an alarm.

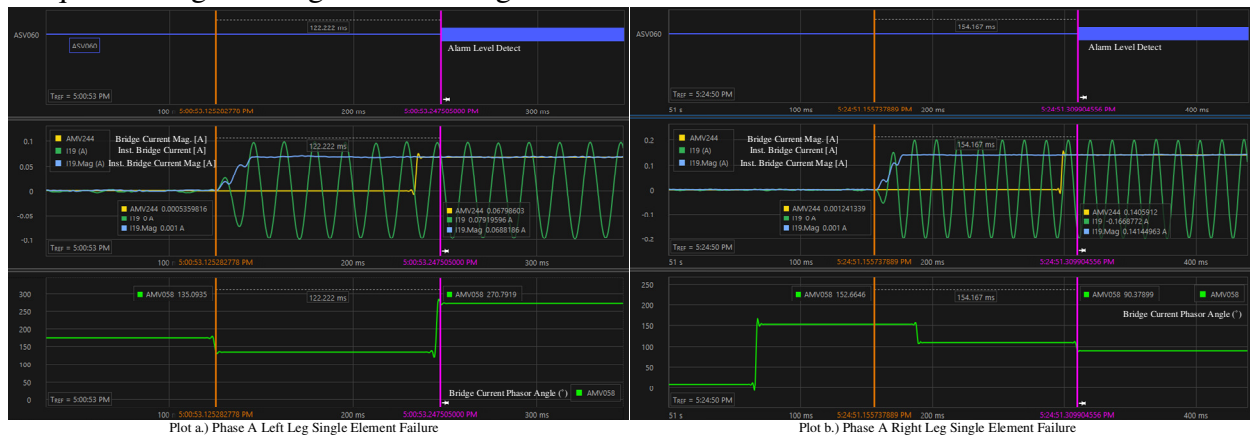


Fig. 11 – Phase A Left and Right Leg Single Capacitor Element Failure

Discussion:

Though the asymmetric double-wye unbalance was fully programmed and implemented in the customizable logic of the relaying platforms, there were several other protection elements mentioned that were also not available as a default protection element onboard the bus differential relaying platforms used. These elements included the thermal elements, the negative

sequence directional overcurrent element, and one voltage element. The limitations mentioned throughout this paper in the centralization and consolidation of the protection elements into the two dual-redundant protective relays led to several insights. First, when attempting to consolidate many protection functions, the availability of customizable logic and mathematical operators on analog quantities within relaying platforms can help to fill the gaps that exist between what default protection elements exist and what is needed in an application. In the example provided in this paper, the logical capability of one relay did not exist and required a secondary device to provide the missing functions; in the second relay nearly ninety percent of logical capability was occupied. Second, the current and voltage input density of a relay informs the capacity of any consolidation effort to facilitate the protection tasks required. In the case of the project details discussed here, had there been a need to monitor an additional set of three phase potentials or currents, the relays selected would not have been able to accommodate the need. When developing consolidated protection applications, preference necessarily should be given to the relays with the highest number of current and voltage inputs. Lastly, the signal processing functions of nearly all relays are built around the fundamental frequency of the power system in which they are deployed. However, there are some non-conventional protection applications where the use of non-fundamental frequency current or voltage analog quantities could be useful. In the case of the harmonic filter banks shown in this paper, if there had been a CT connected and used on the resistor leg of the banks, the current that flows in this leg is mostly, if not entirely and normally, the harmonic frequency of the tuning harmonic of the filter. Users would need to exhibit care to ensure that the protection elements deployed can measure these currents without filtering out pertinent information.

Conclusions:

Modern protection system hardware offers engineers the opportunity to consolidate numerous protection elements into significantly fewer hardware resources than traditionally used. This approach benefits utility customers by reducing both hardware and footprint costs. The consolidation strategy has been demonstrated with a directly connected SVC and could similarly be applied to a directly connected STATCOM. The development and analysis of a protection element designed to detect unbalance conditions in an asymmetric double-wye harmonic filter bank have been presented. Key insights from these consolidated protection efforts include the importance of relays with customizable programming, an abundance of current and voltage inputs, and versatile analog quantities. These characteristics are essential for relaying platforms used in the consolidation and centralization of protection systems.

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Biography:

Zachary Campbell received his Bachelor of Science degree from the University of Akron in 2008, and his Master of Science degree from The Ohio State University in 2012. He has been an engineer at American Electric Power (AEP) for thirteen years, working in various capacities within protective relaying departments including field services and engineering. He also worked for Hitachi ASTEMO (formerly American Showa R&D) for three years. Zak is a senior member of IEEE and is a registered professional engineer in the state of Ohio. zpcampbell@aep.com